Computer Aided Design and Simulation for Comparative Performance Analysis of Nanoscale SOI and GaAs-On-Insulator MOSFETs

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***Abstract*—** From the beginning of the electronics era, the fundamental goals of device research are achieving high speed, low power and ultra-dense integration. During many decades those goals have been successfully achieved through scaling down the silicon based MOS devices. But due to certain operational and technical challenges has made father scaling almost impossible so the further miniaturization. In order to continue farther device advancement, recently some alternative device technology has been evolved like Silicon-on-Insulator (SOI) technology. Although SOI MOSFET exhibit excellent performance to enhance the parameters without further reductions in operating voltage, future scaling may not be feasible. This factor has drowned the attention of research community around the world towards III–V compound semiconductors. It has been predicted in very recent time that modifying SOI structure with III-V compound material will produce III-V compound semiconductor-On-Insulator structure which is expected to show superior performances over its originating structure. Under present analysis, SOI MOSFET and III-V compound (GaAs)-On-Insulator MOSFET are fabricated and their threshold voltage performance has been comparatively analyzed with SILVACO T-CAD process simulator, 'ATHENA', and device simulator, 'ATLAS', respectively. It has been found GaAs-On-Insulator (GAOI) has lower threshold voltage compared to SOI and thus shows better current deliverability when analyzed with oxide thickness and channel length variation.

***Keywords*-** *Nanoscale MOS, SCEs, SOI MOS, III-V Compound MOS, TCAD Simulation*

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I. INTRODUCTION

Driven by tremendous advances in fabrication technology, the semiconductor industry has followed Moore's law by shrinking transistor dimensions continuously for the last 40 years [1]. The big challenge going forward is that continued scaling of planar, silicon, CMOS transistors will be more and more difficult because of both fundamental limitations and practical constrains as the transistor dimensions approach sub nanometers [2]. In common the fundamental limitations imposed by device physics at ultra low dimension are summarized as 'Short Channel Effects (SECs)' and transistor performance is gating vastly affected at 100nm and bellow [3].

So, further improvements in transistor speed and performance may have to come from non-conventional structures with new channel materials [4]. Among the non-conventional MOS structures investigated recently, Silicon-On-Insulator (SOI) structure, has received much attention of the researchers due to some of its inherent advantages [5]. The SOI structure offers many advantages, in particular, higher speed, high radiation tolerance, lower parasitic capacitance, lower short channel effects, better current deliverability, and manufacturing compatibility with the existing technology [6]. Along with such alternative device architectures, some new device materials have been proposed very recently [7]. Among recently proposed materials, the III-V compound semiconductor materials based transistors stand out as promising candidates for future logic applications because their less effective masses lead to high electron mobility and high on-currents [8]. If, those advantages are effectively translated into device performance, it is expected to have superior device performance at lower voltage and thus further voltage scaling will be feasible [8]. So, replacing the silicon channel of SOI MOSFET, with III-V compound semiconductor material is expected to produce better device with improved performance compared to both SOI MOS and simple III-V MOS structures.

Since, along with the experimental exposure, the application of simulation tools for the development of new processes and novel device structures has become a worthwhile and an alternative to the experimental route [9]. For such newly proposed and less investigated structure, III-V compound semiconductor-On-Insulator MOSFET, adopting TCAD simulation tool, will not only help to execute virtual fabricate of such device trough process simulation and it will be also useful to analyze its performance through device simulation.

Till now there are few reports of such III-V compound on insulator MOS structure and those are especially dedicated to different fabrication issues [10]. Performance analysis of such structure especially with respect to general SOI structure is important to understand its potential in future CMOS VLSI era. So, under present analysis a normal SOI MOS and GaAs-On-Insulator (GAOI) MOS structures have been fabricated with TCAD simulator SILVACO process simulator ATHENA. Then with device simulator ATLAS, comparative threshold voltage performance has been investigated for both the structures while gate oxide thickness and channel length have been considered as variables.

II. PROCESS & DEVICE SIMULATION

Partially depleted n-channel SOI MOSFET and GaAs MOSFET have been fabricated and their performance are simulated with SILVACO TCAD tools, ATHENA and

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ATLAS respectively [8]. Under present analysis an initial structure is considered to have the silicon substrate, SiO_2 buried layer and the silicon thin film as channel for SOI and silicon substrate, SiO_2 buried layer and GaAs thin film as channel material for GAOI MOSFET. Once the initial structure has been defined, the standard n-type MOS fabrication process has been applied to fabricate rest of the structure such as oxidation, materials deposition, diffusion, and etching etc. Some of the parameters of the fabricated structures are given in the following table.

TABLE I
STRUCTURAL PARAMETERS CONSIDERED FOR SIMULATION

PARAMETERS	VALUE
CHANNEL THICKNESS	100 NM
CHANNEL DOPING (BORON)	1×10^{15} CM^{-3}
BURIED LAYER THICKNESS	400 NM
SUBSTRATE THICKNESS	500 NM
SUBSTRATE DOPING (BORON)	1×10^{14} CM^{-3}
S/D DOPING (ARSENIC)	0.5×10^{16} CM^{-3}
POLLY SI DOPING (ARSENIC)	1×10^{19} CM^{-3}

Fallowing process simulation device simulation has been carried out in ATLAS and threshold voltage value has been extracted with the gate oxide thickness and channel length variations. In device simulation model self heating effect, quantum mechanical effects etc. are incorporated to improve the accuracy of the simulation [8]. Extra interface roughness effect at the gate oxide and channel interface for GAOI structure has been encountered with the excess interface trap charge density compared to SOI structure [8].

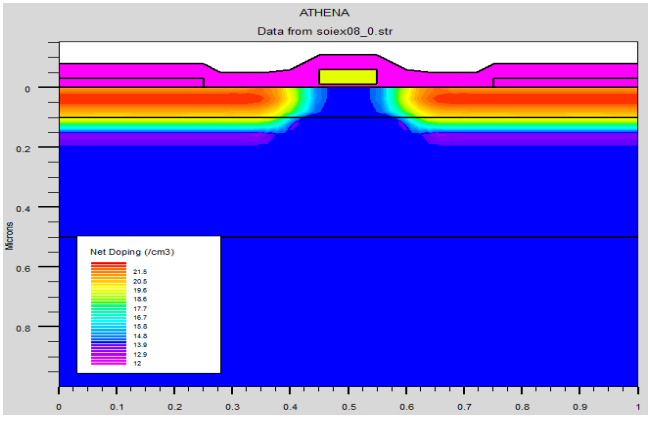

Figure 1 ATHENA simulated SOI structure and for GAOI the channel Silicon material has been replaced with GaAs

III. RESULTS & DISCUSSIONS

Under the present work threshold voltage has been simulated for SOI MOSFET and GAAS MOSFET with various oxide thickness and channel length and the comparison graph has been plotted.

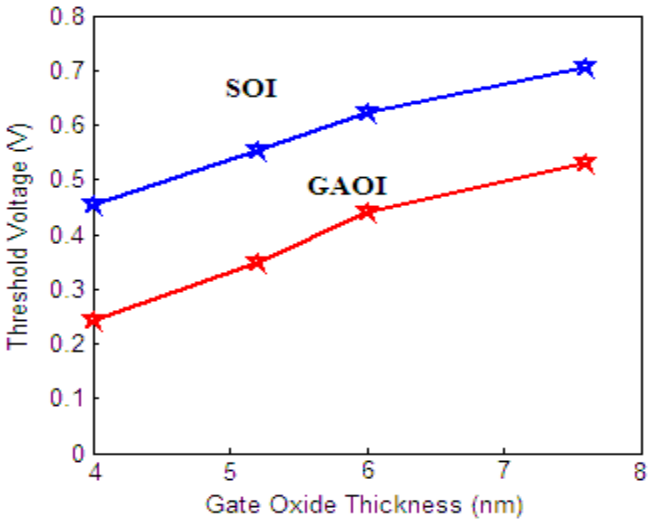

Fig.ure 2 Threshold voltage with gate oxide thickness for a channel length 90nm

The variations of threshold voltage with gate oxide thickness have been plotted (in Fig. 2.) for different SOI and GAOI structures. As expected, threshold voltage has increased with increasing gate oxide thickness and that is due to less gate voltage control over channel potential.

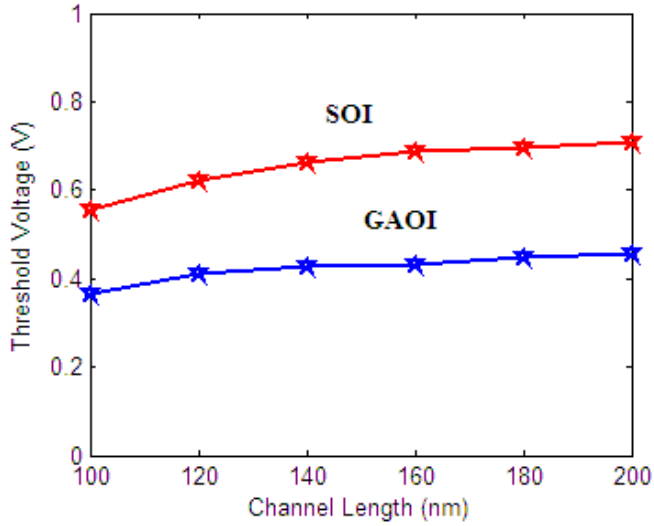

Figure. 3 Threshold voltage variation with channel length for gate oxide thickness 5nm

Similarly, in Fig. 3., the threshold voltage variations with different channel lengths have been plotted. It is clear from the Fig. 3. the decreasing channel length will roll down the threshold voltage due to enhanced so called Short Channel Effects.

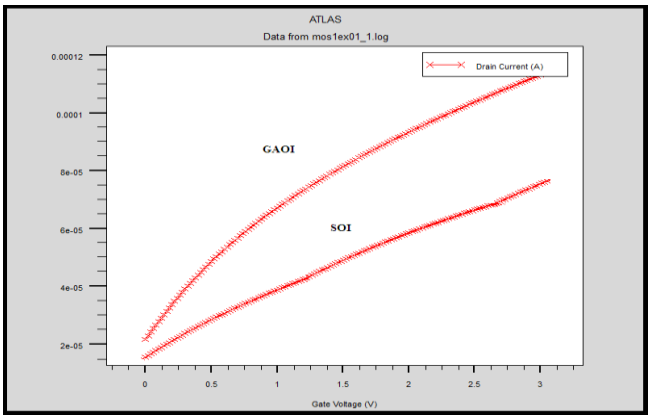

Figure. 4 Drain current with gate voltage for gate oxide Thickness 5nm and channel length 90nm

Both the structures show similar threshold voltage roll off but lower threshold voltage and higher electron mobility initiate higher current in GAOI structure as shown in Fig. 4.

IV. CONCLUSION

Through present analysis Nanoscale SOI and GAOI MOSFET structure has been fabrication through process simulation and device simulation has been performed to analyze its threshold performance with gate oxide thickness and channel length. Present analysis shows that GAOI structure provides better current voltage performance compared to simple SOI structure. This scenario is initiated with reduced threshold voltage as well as higher carrier mobility in GaAs material and it has been confirmed with the present simulation study. Lower threshold voltage not only initiate higher current, it also provides option for further voltage scaling. Although, lower threshold voltage can enhance some negative effect like higher leakage current but that can be restricted with modified structure with different material. The present analysis shows that GAOI MOSFET technology is able to offer devices with voltage scalability and enhanced performance. Over SOI, GAOI, structures provides scope for further miniaturization of devices for the next generation CMOS VLSI.

REFERENCES

[1] The International Technology Roadmap for Semiconductor, Emerging Research Devices (2009).

[2] Sanjoy Deb, N.Basanta Singh, Nurul Islam, and S.K.Sarkar, "Work Function Engineering with Linearly Graded Binary Metal Alloy Gate Electrode for Short Channel SOI MOSFET", IEEE Transactions on Nano Technology, Vol. 11 (3), pp. 472-478, 2012.

[3] Sanjoy Deb, Saptarsi Ghosh, N Basanta Singh, A K De and Subir Kumar Sarkar, "Two dimensional Analytical Model Based Comparative Threshold Performance Analysis of SOI-SON MOSFET", Journal of Semiconductor, IOP, Vol. 32 (10) 2011.

[4] M. Jagadesh Kumar and Anurag Chaudhry, "Two-Dimensional Analytical Modeling of Fully Depleted DMG SOI MOSFET and Evidence for Diminished SCEs", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 51, NO. 4, APRIL 2004

[5] Wenjie Lu et. al., A Test Structure to Characterize Nano-Scale Ohmic Contacts in III–V MOSFETs, IEEE ELECTRON DEVICE LETTERS, VOL. 35, NO. 2, pp. 178-180, FEBRUARY 2014

[6] Qian Xie et. al., Comprehensive Analysis of Short-Channel Effects in Ultrathin SOI MOSFETs, IEEE Transactions on Electron Devices, Volume:60 , Issue: 6, pp. 1814 – 1819, June 2013

[7] J. C. Lin, S. Y. Yu, and S. E. Mohney, "Characterization of lowresistance ohmic contacts to n- and p-type InGaAs," J. Appl. Phys., vol. 114, pp. 044504-1–044504-8, Jul. 2013.

[8] Nanometer-scale electronics with III–V compound semiconductors,Jesus A. Del Alamo, 17 NOVEMBER 2011 VOL 479| NATURE | 317.

[9] ATHENA, ATLAS Users Manual, SILVACO International, www.**silvaco**.com

[10] Junghyo Nah et.al., III−V Complementary Metal−Oxide−Semiconductor Electronics on Silicon Substrates, Nano Lett. 2012, 12, pp. 3592−3595.