Power Optimization of Linear Feedback Shift Register (LFSR) for Low Power BIST: A Review

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Abstract— This paper provides a comparison between different types of Linear Feedback Shift Register which are built by using fast binary counter, or using a hierarchical Manchester carry chain, and a counter built using a low time linear feedback shift register. The comparison is focused on speed, power and area consumption. We demonstrate the use of LFSR as an alternative to conventional binary event counters. In order to use an LFSR as a counter, an efficient algorithm for decoding the pseudo-random bit patterns of the LFSR counter to a known binary count is also discussed. The hypotheses that LFSR counters leads to reduced area and higher speed were validated after discussing simulation and measurement results.

Keywords- *LFSR, Low Power, Optimization, BIST, Test Patterns*

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I. INTRODUCTION

An LFSR is a finite state machine that goes through n cycles before repeating the sequence. It is structurally a shift register with specific tap taken out and XOR-ed with nth flip-flop and fed back to itself. It can be represented either as a binary polynomial, P(x), or transition matrix (T). The transition matrix decides the next state of the LFSR depending on its current state [1].

Built-in Self- Test (BIST) and BIST based analysis emerged as promising solutions to VLSI testing. BIST is a DFT method that aims to detect faulty components in a system incorporating the test logic on the chip. BIST is well known for its many benefits such as improved testability, testing at low speed and the need for costly external automatic test equipment (ATE). In BIST, a shift register with linear feedback (LFSR) generates the pseudo-random patterns to test the main input or scan chains and multiple entries firm entry (MISR) record the responses of the evidence received compact primary production or the output of the scan chains . The test vectors applied to a circuit under test to the nominal operating frequency often cause more average and / or maximum power dissipation in normal mode. The reason is that the randomness of patterns generated by the LFSR, the correlation between the reduction and pseudo-random patterns in each model as well. This, in turn, can lead to more power dissipation and switching in test mode[2].

The Global System for Mobile communications use different encryption algorithms. But the information must be secure so nobody could interfere during communication as a secret spy named listeners. To protect our information, the cryptography used. However, to send information from the mobile station to the base station, which is the air interface avoiding serious security between communicating party's threat. Initial value of the LFSR is called the seed for the operation of LFSR is the values of deterministic flow generated by LFSR are completely determined by their current or previous state. However, the feedback function choice LFSR can produce a sequence of bits which appears random and long cycle [6].

BIST simplifies and reduces the overall cost of test generation through the internal configuration and the output of the analyzer also speeds up the process. It has a BIST unit test generation and control hardware to sequence the desired pattern of the circuit under test (CUT). The role of test pattern generation is usually done by a shift register with linear feedback circuit (LFSR). This is a pseudo -random sequence in which this structure is a simple shift register. The main factors that determine the quality of a generator model are the fault coverage (fc) and test time. Test runtime is quantified by the number of units (n). This depends on the characteristic polynomial that describes the selected LFSR and initial state (seed) responsible for their records.[3]

II. REVIEW ON LFSR ARCHITECTURE

A. Low Power LFSR

LFSR is characterized by the polynomial by its characteristics polynomial and inverse of characteristics polynomial is generated polynomial.

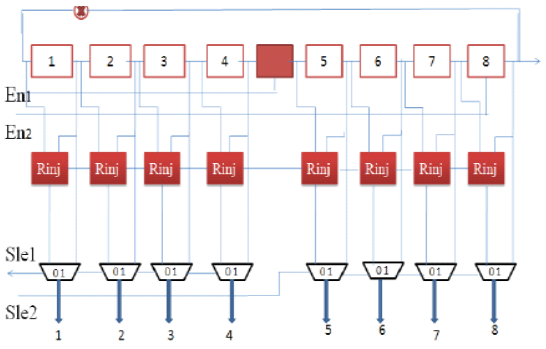

Figure 1: Low Power LFSR

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This approach the 3 intermediate test vectors are generated between every two successive vectors (say TI, T2). The total number of signal transition occurs between these 5 vectors are equivalent to the number of transition occurs between the 2 vectors. Hence the power consumption is reduced. Additional circuit is used for few logic gates in order to generate 3 intermediate vectors [4].

The 3 intermediate vectors (Ta, Tb, Tc) are achieved by modifying conventional flip-flops outputs and low power outputs. The first level of hierarchy from top to down includes logic circuit design for propagation either the present or next state of flip-flop to second level of hierarchy. Second level of hierarchy is implementing Multiplexed (MUX) function i.e. selecting two states to propagate to output as shown in flow [4]. Second level of hierarchy is implementing Multiplexed (MUX) function i.e. selecting two states to propagate to output as shown in figure 1.

B. LFSR Based On Proposed Random Key Generator

We have here four LFSR that we will use as random key generator to provide the map that implements the information hiding. The Figure 2 shows the main component of this generator.

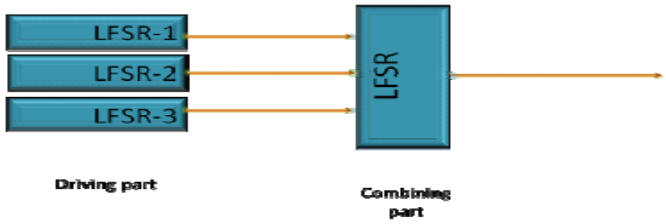

Figure 2: Components of LFSR based on proposed random key generator

The random key generator consists of two parts: the driving part and the combining part. The driving part consists of three LFSR's of length 29, 30, 31 stages for each. The tapping stages are (31, 3), (30, 23), (29, 27), each of these feedback functions produce a maximal period. These registers are initialized using a special procedure and are very important for the circuit. The combining part consists of a single LFSR of length8 stages with a feedback function defined by the tapping (8, 5, 3).[5]

C. Hierarchical Manchester Carry Chain Counter

As the name suggests, the high-speed counter in this work uses a hierarchical Manchester carry chain for carry propagation. This carry chain propagates the previous carry signal if the input signal Ai is high, and kills it otherwise. All the transmission gates (TGs) shown in Figure 3 below have high signal strength in order to reduce the propagation delay in the carry path. The pull-down n-MOS transistors have less value of Wn while inverters have W /Wn value to on the lower side. There are DFFs, XOR gates and a tri-state buffer (not shown) at each output. The counter has input carry Co at logic high, so that a count of one is added at every clock cycle. The carry to the next hierarchal level will be high if and only if all the bits (Ao: A3) are high. A 4-input AND gate - with graded sizing of n-MOS transistors in order to reduce the propagation delay is utilized to generate the carry skip signals [6].

This carry skip circuit is built into each 4-bit counter used in the longer counters. The 8-bit counter consists of two 4-bit counters with a second level of hierarchy in the form of a 2-bit Manchester carries chain. The 16-bit counter is built with four4-bit counters and a second level of hierarchy in the form of a 4-bit Manchester carry chain. The more complex 32-bit counter consists of four 8-bit counters linked by a third level of hierarchy in the form of a 4-bit Manchester carry chain. When necessary, inverting buffers were added to the carry chain so as to increase the operating frequency. The complete binary counter chip consists of four counters of length 4, 8, 16, and 32 bits. A decoder is used to enable the Outputs of only one counter at a time.

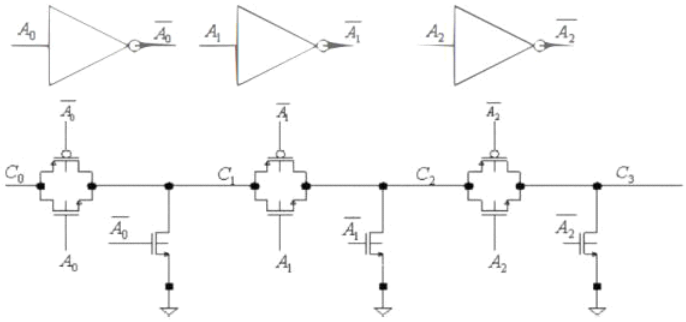

Figure 3: Hierarchical Carry Chain Counter

D. Low-Transition LFSR for BIST-Based Applications

Random pattern generators such as LFSR usually generate very low correlated patterns. *Sn* is the number of bits in the test patterns which is equal to either the number of PIs or length of scan chain in the circuit under test. If *Ti* is used for combinational circuits, then it is applied to PIs. If *Ti* is a pattern generated to be used in sequential circuits, it is applied to the scan-in pin (SI) of a scan chain in the circuit.

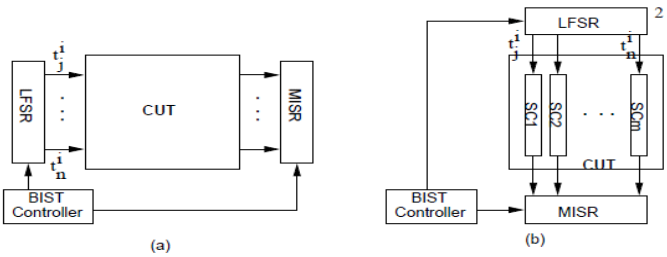

Figure 4: Combinational and Sequential Circuits

For this purpose, we have designed a new random pattern generator that reduces the total number of transitions among the adjacent bits in each random pattern (horizontal dimension) and transitions between two consecutive random

patterns (vertical dimension) as well. In other words, the new low transition random pattern generator increases the correlation between and within patterns and can be used for any circuit kind, i.e. Combinational or sequential [7].

Assume that $T_{i-1}$and T_i are two consecutive patterns and the number of bit changes (transitions) between two consecutive patterns high. Therefore, if low correlated patterns are applied to PIs of combinational circuits (Figure 4), they generate high number of transitions at the PIs which in turn results in huge number of switching activities in circuit under test. Assume that pattern T_i is shifted into the scan chain and the number of transitions among the adjacent bits going into the scan chain is high. [8]

III. CONCLUSION

After comparing different LFSR counters, it is found that multi counter is faster than the conventional binary counter. The discussion also show that as the length of the counter increases, the maximum operating frequency of the conventional counter decreases. On the other hand, increasing the length has negligible effect on the LFSR counter. Its maximum operating frequency remains almost constant at 6.7MHz for a power supply of 1.1 V, independent of N. Several possible reasons for this disparity are supply noise, clock jitter, parasitic capacitances in the layout that is not accounted for during simulation, and normal process variations in threshold voltage and mobility. Additionally, LFSR counters occupy significantly less area compared to the conventional binary counter, due to the simplicity in the LFSR logic. On the other hand, simulation results showed 54% higher power for a 16-bit LFSR counter and 71 % higher power for a 32-bit LFSR counter, compared to their binary counterparts.

IV. REFRENCES

[1] Guang Zeng, Wenbao Han, and Kaicheng He, High Efficiency Feedback Shift Register, International Journal of Engineering and Innovative Technology (IJEIT) Volume 1, Issue 4, January 2013.

[2] Sunil Kumar Muttoo, Ismael Abdulsattar, a new stego-system based on LFSR generator, International Journal of Engineering and Innovative Technology (IJEIT) Volume 1, Issue 1, January 2012.

[3] R. Vara PrasadaRao, N. Anjaneya Varaprasad, G. Sudhakar Babu, C. Murali Mohan, Power optimization of Linear Feedback Shift Register (LFSR) for Low Power BIST implemented in HDL, International Journal of Modern Engineering Research (IJMER) Vol. 3, Issue. 3, May-June. 2013, pp-1523-1528.

[4] Nisha Haridas, Dr. M. Nirmala Devi, Modified Genetic Algorithm for Deciding LFSR Configuration, VLSI Research Group, Amrita University, Coimbat IJECTore, India IJECT Vol. 2, Issue 2, June 2011.

[5] Rosepreet Kaur, Nikesh Bajaj, Enhancement in Feedback Polynomials of LFSR used in A5/1 Stream Cipher, International Journal of Computer Applications (0975 – 8887) Volume 57– No.19, November 2012.

[6] Timothy Brian Brock, Linear Feedback Shift Registers in SAGE, May 16, 2006.

[7] Mohammad Tehranipoor, Mehrdad Nourani, Nisa Ahmed, Low-Transition LFSR for BIST-Based Applications, 2011.

[8] Avinash Ajane, Paul M. Furth, Eric E. Johnson, and Rashmi Lakkur Subramanyam, Comparison of Binary and LFSR Counters and Efficient LFSR Decoding Algorithm, 2013.