Layout Design and Implementation of Adiabatic based Low Power CPAL Ripple Carry Adder

Ms. Bhumika Narang
TCE Department
CMR Institute of Technology, Bangalore
er.bhumika23@gmail.com

***Abstract*— this paper presents schematic and layout designs for low power adiabatic Ripple Carry Adder which is implemented by proposed N-type & P-type Full Adder Cell. Adiabatic logic Design is the most efficient energy saving technique which provides very low power dissipation for VLSI circuits. In this paper the main emphasis on the most significant technique of adiabatic logic design that is Complementary Pass Transistor Logic. Simulation results shows that energy loss of digital VLSI circuits can be greatly reduced by using Complementary Pass Transistor Adiabatic Logic technique. All the circuits have been simulated on BSIM3V3 90nm technology on tanner EDA tool.**

***Keywords*- Adiabatic Logic Design; Low power; Full Adder; Power Delay Product(PDP).**

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I. INTRODUCTION

Motivation to reduce energy consumption of logic circuits comes from increasing difficulties in removing heat from high speed VLSI circuits. The importance of reducing power dissipation in digital systems is increasing as the range and complexity of applications in portable and embedded computing continues to increase. System-level issues such as battery life, weight, and size are directly affected by power dissipation [1]. A trend into reducing power dissipation of the digital systems only serves to improve the performance and capabilities of these systems.

The power dissipation is a critical concern in the design of VLSI circuits with increasing package density and working speed. Also the energy consumption of battery-driven systems is above all problem to be considered. Many low power design methods have been developed to reduce CMOS digital circuit's power consumption. However the adiabatic circuit is an attractive way to obtain extreme low power level which conventional CMOS digital circuit can't reach [2]. At present time, lots of digital systems are targeted at portable, battery-operated systems, so power dissipation is one of the primary design constraints.

To reduce the power dissipation, the circuit designer can minimize the switching events, decrease the node capacitance, reduce the voltage swing, or apply a combination of these methods. In all these cases, the energy drawn from the power supply is used only once before being dissipated. To increase the energy efficiency of the logic circuit, other measures can be introduced for recycling the energy drawn from the power supply [3]. A novel class of logic circuits called Adiabatic Logic offers the possibility of further reducing the energy dissipated during switching events, and the possibility of recycling or reusing, some of the energy drawn from the power supply.

II. ADIABATIC LOGIC DESIGN

Recently, a novel approach to reduce power dissipation in digital circuits was proposed, which is to be used and verified in many digital applications. The approach, called adiabatic logic design, utilizes clocked ac power to slowly charge the node capacitances and then partially recover the energy associated with that charge.

The term "adiabatic" is typically used to describe thermodynamic process that has no energy exchange with the environment, and therefore no energy loss in the form of heat [5]. Adiabatic digital circuits have the ability to recover energy once committed in computation and make it available for recycling. Due to the trend of increasing clock frequencies and transistor count, power demands new System-on-Chip designs will continue to grow. Adiabatic logic style has emerged as a promising approach to achieve ultra-low power without sacrificing noise immunity and driving ability.

Adiabatic circuits are low power circuits which use "reversible logic" to conserve energy. Adiabatic logic is a low–power circuit design approach where the signal energy stored on a capacitor may be recycled instead of dissipated as heat. Power dissipation can be avoided if the capacitor is slowly charged with a voltage ramp. It is possible to recover this charge back into the power source by discharging the capacitor to a down–ramping supply. Adiabatic principles, together with charge reuse by redistribution, can be utilized for power saving in interconnects [4].

Adiabatic logic is an attractive low power approach by utilizing AC voltage supplies (power clocks) to recycle the energy of circuits instead of being dissipated as heat. Adiabatic circuits are work on the principal of adiabatic charging and discharging by which energy is recycled from output nodes instead of discharging it to ground. Conventional CMOS circuits achieve a logic '1' or logic '0' by charging the load capacitor to supply voltage V_{dd} and discharging it to ground respectively. Thus every time a charge-discharge cycle occurs an amount of energy equal to CV^2 is dissipated. Unlike

the conventional CMOS circuits, in adiabatic circuits energy is recycled. Instead of discharging the capacitor to ground, the charge is discharged to the power supply [3]. Since the charge has to be discharged to supply, the supply in adiabatic circuits is a time varying one called the power clock. It has been observed that among the different waveforms for charging or discharging the load capacitor, a ramp is more efficient and as such trapezoidal power clocks have been used in many adiabatic circuit styles [8]. Many adiabatic logic circuits which dissipate less power than static CMOS logic circuits have been introduced as a promising approach in low power circuit design.

III. Proposed CPAL Full Adders

Transistor count of CPAL circuits are considerably less than the another techniques of Adiabatic Logic Design. CPAL circuits have more efficient energy transfer and recovery, because the non-adiabatic energy loss of output Loads has been completely eliminated by using complementary pass-transistor logic for evaluation and transmission gates for energy recovery. Complementary pass transistor logic concept reduces the complexity of circuit [6].

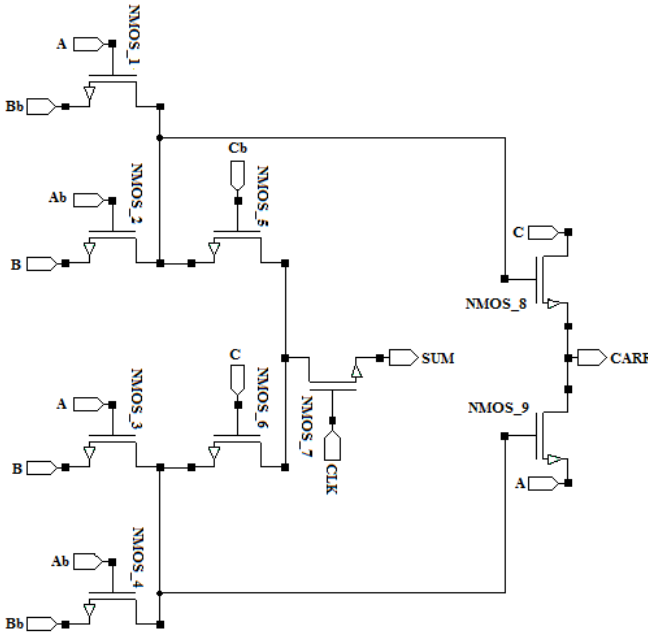

Figure 1. Proposed N-type CPAL Full Adder

CPAL technique uses purely NMOS or PMOS pass transistor network for the logic operations. All inputs are applied in complementary form i.e. every input signal and its inverse must be provided. CPAL circuits also produce complementary outputs which can be used further in subsequent CPAL stages. The CPAL circuit essentially consists of complementary inputs, an NMOS pass transistor logic network to generate complementary outputs. The elimination of PMOS transistors from the CPAL logic significantly reduces the parasitic capacitances associated with each node in the circuit. Thus the operation speed is typically higher compared to CMOS logics and also it reduces the overall noise immunity. On the other hand CPAL design style is highly modular i.e. a wide range of functions can be realized by using the same basic pass transistor structures [1].

Proposed design of N-type CPAL full adder is shown in fig. 1. The circuit uses only NMOS pass transistors. Power clock is given at the gate of transistor NMOS_7. Power clock is the essential required component of an adiabatic ciruit. To perceive about the working side of proposed circuit let us consider the input signal "101" is applied at input port A, B and C. By appling this input pattern transistor NMOS_1 turned on and other four transistors NMOS_2 to 4 remain in off mode. Bit '1' is available at source of transistor NMOS_5 and '0' bit is available at source of transistor NMOS_6. Since Input signal Cb is '0' thus no transition is occure to the output port sum through transistor NMOS_5 and '0' is transmit to transistor NMOS_7 via transistor NMOS_6. Hence output available at output port sum is '0', which is a correct output for the applied input bit stream. At the other side 1 is available at gate of transistor NMOS_8. That makes transistor NMOS_8 on and value form input port C is transferred to the output port carry that is '1', which is correct for a full adder logic block.

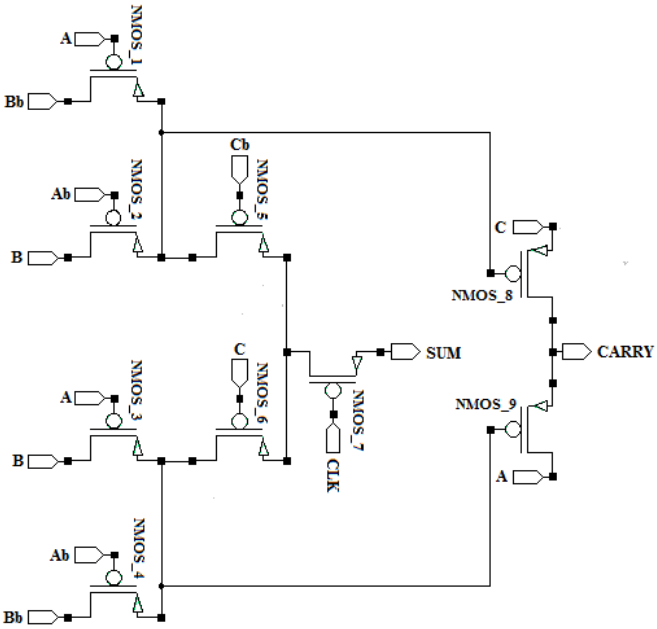

Figure 2. Proposed P-type CPAL Full Adder

Proposed design of P-type CPAL full adder is shown in fig. 2. The circuit uses only PMOS pass transistors. Here also power clock is given at the gate of transistor NMOS_7. In the case of PMOS transistor output is taken from the source terminal. The working principle of both proposed designs are approximatly same but the difference is found in the results. N-type CPAL full adder gives more efficient charge transfer and recovery from the output node.

IV. Proposed CPAL RCA

It is possible to create a logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs a C_{in}, which is the C_{out} of the previous adder. This kind of adder is a ripple carry adder, since each carry bit "ripples" to the next full adder. The first full adder may be replaced by a half adder. Here 4-bit ripple carry adder is implemented with the help of four full adder blocks. Fig. 3 and 4 shows the ripple carry

adder implemented with proposed PMOS and NMOS CPAL full adder design simultaneously for checking driving capability of proposed circuit.

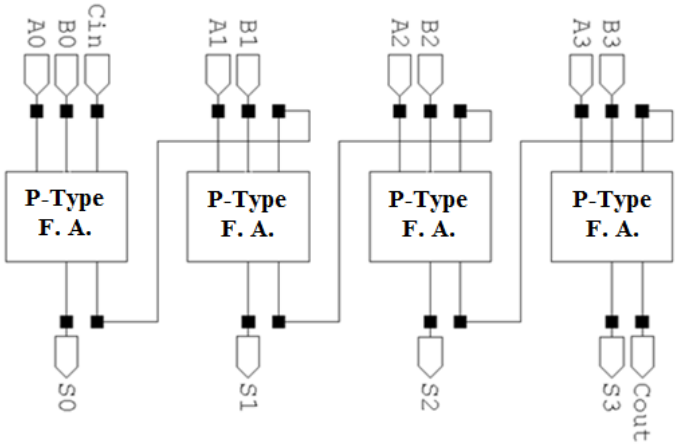

Figure 3. Proposed P-type CPAL Ripple Carry Adder

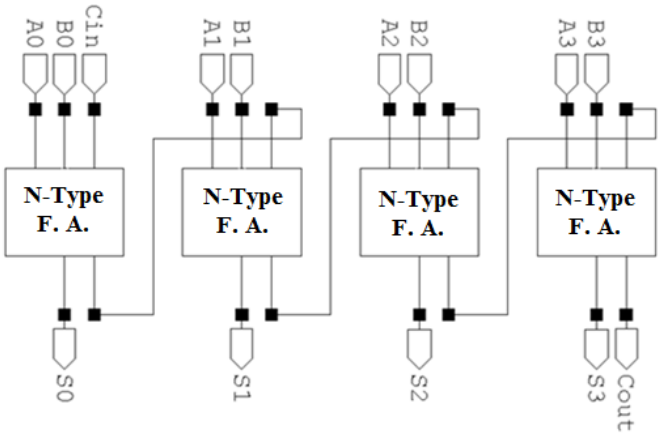

Figure 4. Proposed N-type CPAL Ripple Carry Adder

V. Layout Design of CPAL Full Adders and Ripple Carry Adder

Layouts of proposed P-Type and N-type and full adder are shown in Fig. 5 and 6 respectively. Again for checking the driving capability of proposed full adders layouts of P-type and N-type ripple carry adders are implemented by using Tanner EDA tool. These layouts of ripple carry adder are shown in Fig. 7 and 8 correspondingly.

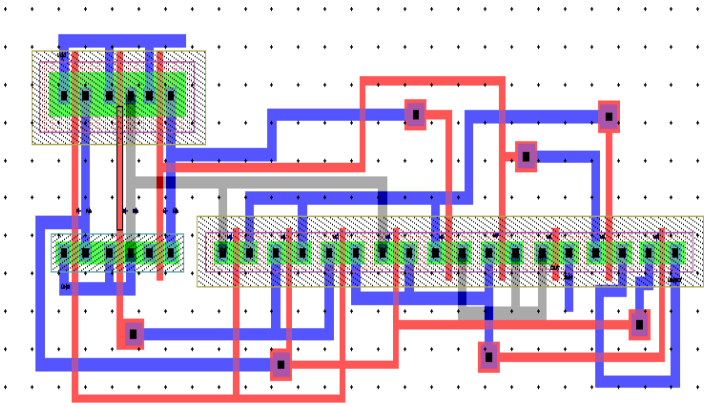

Figure 5. Layout of P-type CPAL Full Adder

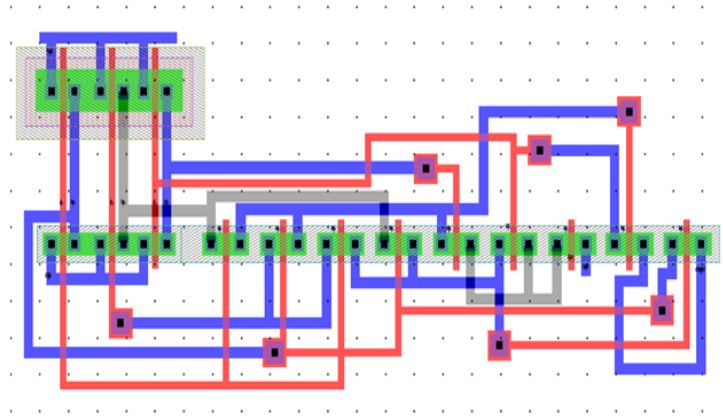

Figure 6. Layout of N-type CPAL Full Adder

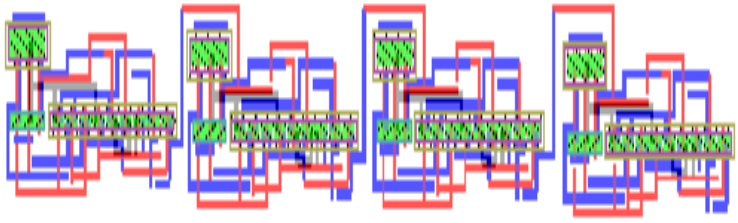

Figure 7. Layout of P-type CPAL Ripple Carry Adder

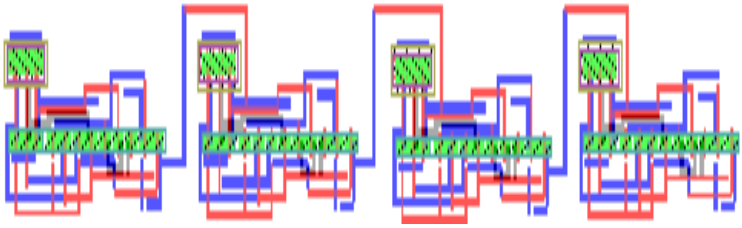

Figure 8. Layout of N-type CPAL Ripple Carry Adder

VI. Simulation Results

A. *Simulation Environment*

All the circuits have been simulated on BSIM3V3 90nm technology on tanner EDA tool. To establish an impartial testing environment each circuit have been tested on the same input patterns.

B. Simulation Comparison

Fig. 9 to 14 shows the comparison between PDP Vs power supply voltage, PDP Vs temperature and PDP Vs operating frequency for full adders and ripple carry adders. As it is reveals from the graphs that the proposed design of NMOS CPAL full adder shows more efficient results in compare to PMOS one and also have better driving capability as it gives proficient results in deliberation of ripple carry adder also. These graphs simply conclude that proposed design is better on various values of temperatures, power supply voltages and operating frequencies.

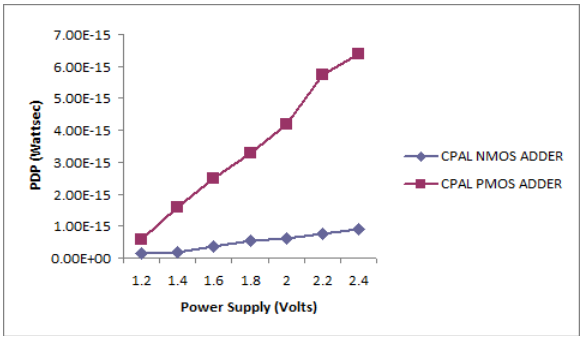

Figure 9. Comparison of PDP for the Adiabatic full adders at different supply voltages

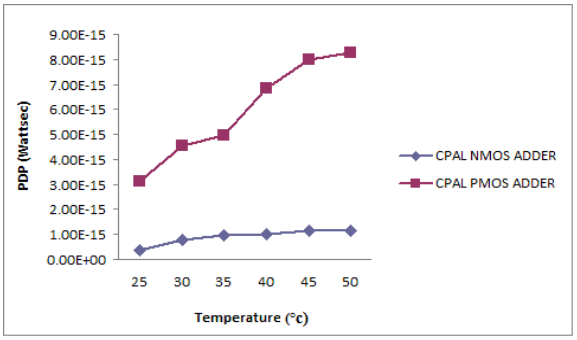

Figure 10. Comparison of PDP for the Adiabatic full adder at different values of temperatures

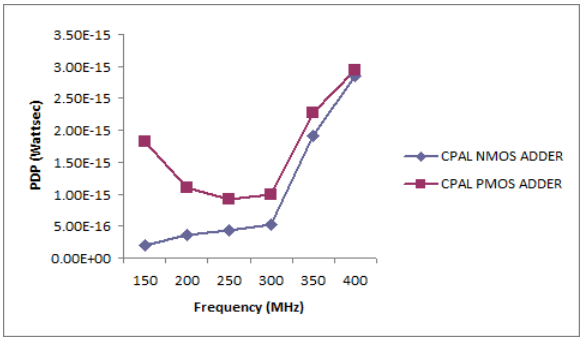

Figure 11. Comparison of PDP for the Adiabatic full adder at different operating frequencies

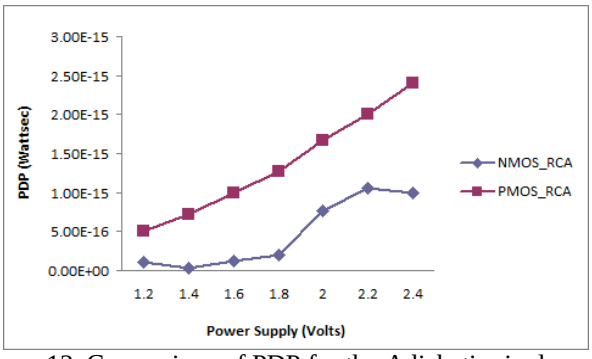

Figure 12. Comparison of PDP for the Adiabatic ripple carry adders at different supply voltages

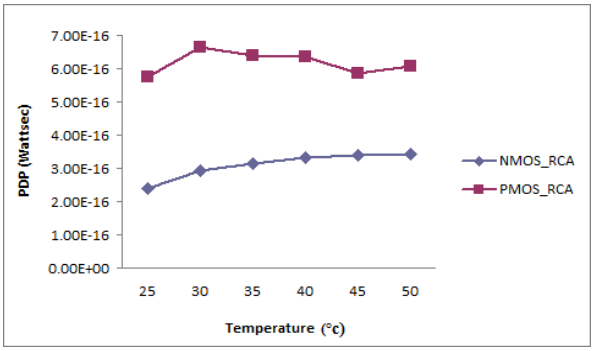

Figure 13. Comparison of PDP for the Adiabatic ripple carry adder at different values of temperatures

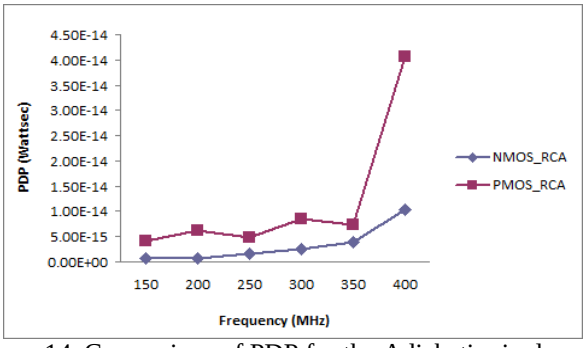

Figure 14. Comparison of PDP for the Adiabatic ripple carry adder at different operating frequencies

VII. CONCLUSION

Adiabatic circuits offers reduction in the power dissipation for the VLSI circuits. Adiabatic circuits adopt a gradually rising and falling power-clock, can result in a considerable energy saving. NMOS and PMOS full adder are proposed using CPAL techniques. Previous Research work defines that that the proposed NMOS and PMOS CPAL full adder behaves much better than another circuits reported in literature. In comparison of NMOS and PMOS full adder blocks we found NMOS full adder block is more efficient than PMOS full adder block. Proposed NMOS CPAL full adder shows 89% power reduction than the other CPAL full adder and 78% power reduction in compare to other full adder blocks. Also the 4-bit Ripple carry adder is implemented by using proposed NMOS and PMOS full adder circuits for checking the driving capability of circuit. N-type RCA shows promising results than 4-bit RCA designed by using P-type full adder which proves that N-type RCA has lower power consumption than P-type RCA. We can also use this proposed NMOS for implementing n-bit ripple carry adder, carry save adder, carry

generate adder, multipliers etc. Consequently, the proposed adiabatic NMOS full adder cell can be a viable option for efficient system design in low power logic applications.

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