Design of 16-Bit Quaternary adder using Various Encoding Techniques

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Abstract— Design of binary circuit is restricted by the necessity of the interconnection. A conceivable arrangement could be touched base at by utilizing a bigger arrangement of signs over the same chip region. Quaternary outlines are picking up significance from that point of view. In this paper we design two types of full adder based on quaternary logic is proposed which will reduced the parameter such as area, power, and delay. The feature of this full adder is based on one hot encoding technique and binary encoding technique. All the design is using 180nm CMOS techniques. Sum and carry blocks are handled in two separate square controlled by the code generator unit. Plan check will be done by tanner tools.

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I. INTRODUCTION

In binary digital circuit static power is directly related to the leakage power. In binary circuit number of interconnection is available to reduce that interconnection we can used quaternary adder. Quaternary circuit shows improvement in area, power and delay.[5]

Interconnection of area is determined by the number of interconnection and their length. Interconnection length is also determined by the complexity of interconnection.

The decimal number 255 in binary it will be 11111111 and in quaternary it is represented as 3333[1].To reduce the area, interconnection, power, transistor by using quaternary logic. There are four quaternary states 0, 1, 2 and 3 for which we can take parallel comparable as 00, 01, 10 and 11 [5]. They are called as total low, medium low, medium high and supreme high. In the event that the bits of paired representation trade their position and quaternary state stay unaffected then it is called as twofold symmetry if not called as halter kilter.[3]
This paper is organized as, section II full adder using one hot encoding. Section III Full adder using binary encoding, section IV Future scope and conclusion is in section V.

II. FULL ADDER USING ONE HOT ENCODING

The propose quaternary full Adder designed with one hot encoding technique. It consists of one hot decoder block, one hot decoder with carry block, sum and carry block. In one hot decoder at a time only one bit active. A and B are the two input of full adder circuit. Barrel Shifter is controlled by two inputs A and B. In quaternary input logic level of 0, 1, 2, and are represented by 0V, 1V, 2V and 3V.
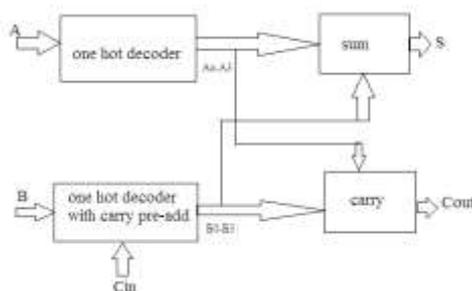

Figure 1: Block Diagram Of Quaternary Full Adder

One-Hot Encoder Block:-
In one hot encoding only one bit of the state vector is assert for any given state given state. All other state bits are zero. Thus if there are n state then n state flip-flops are required. As only one bit remains logic high and rest are logic low, it is called as one-hot encoding. And the input will generate A0-A3 four hot codes. Since there is a two inputs A and B.

Encoding For The Input B With Carry Pre-Addition:-
It depends on the one contribution of the yield lines will be high and all others will be low. The point by point hardware incorporates down strict circuits, twofold XOR doors alongside double inverters to get fitting one hot yield. Thus the snake to be composed is a full viper we ought to likewise deal with the convey info. Thus because of this convey pre expansion is done to the information B before the yield is shared amongst Sum and Carry generators.

Summer Block:-
Subsequently it is clear that from the table of a full adder the entirety part of the adder is only a movement of one info relying upon the other. To minimized the circuitry barrel shifter is used where 0V, 1V, 2V and 3V is the quaternary voltage level. In circuit diagram A0-A3, B0-B3 is the output of one hot encoding and sum block show in the circuit.

Carry Block:-
The carry generator block utilized is only a blend of inputs where one info line goes about as select line and chooses or rejects a different line taking into account whether the blend of info is meeting the prerequisites of producing convey yield. The convey pre-expansion activity which happens in the main part of the snake, dispenses with the convey part if data B is 3V and convey in is high thus an OR entryway is utilized to spare that convey what's more, drive it to complete in the carry block circuit.
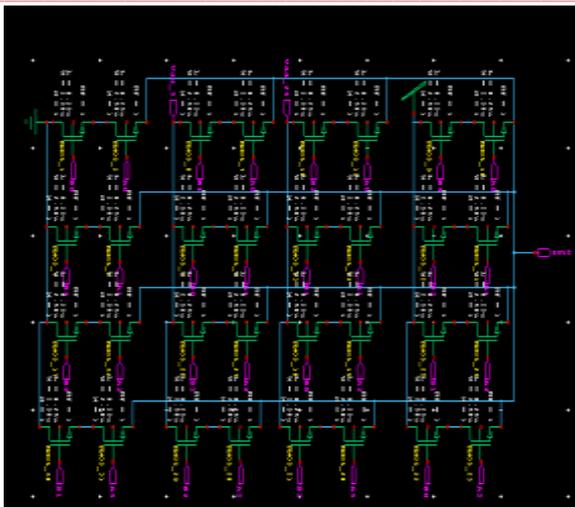
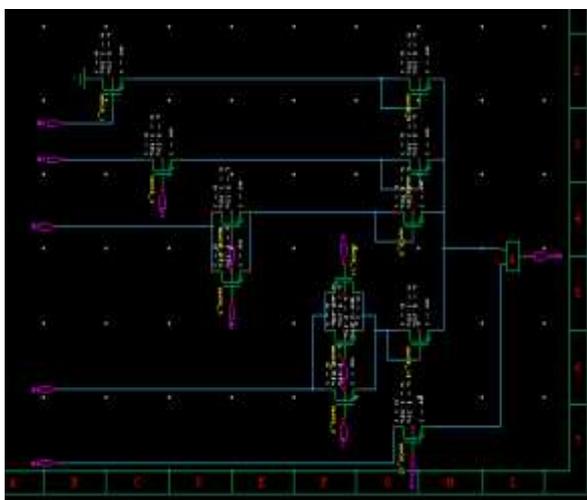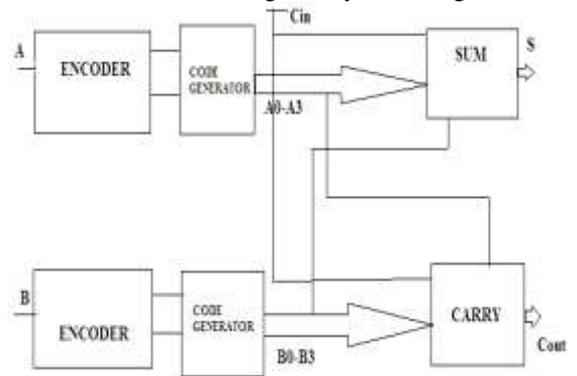Figure 2: Logic Circuit Of Sum Block

Figure 3: Logic Circuit Of Carry Block

Figure 5: Output Of Quaternary 16-Bit Adder

III Full Adder Using Binary Encoding:-

Encoder Block:-

In full adder using binary encoding there is a Encoder block the encoder block having input A and B yield is sustained to the code generator unit. Furthermore, this code generator unit produces codes which are used for the entirety and convey square to produce last estimation of entirety and convey. Code generator having output A0-A3 and B0-B3 and it is given to sum and carry block.

Code Generator:-

Code generation is the process by which a compiler's code generator converts some intermediate representation of source code into a form (e.g., machine code) that can be readily executed by a machine. Code generator block generate the output A0-A3 and B0-B3. And it is given to sum and carry.

Sum & Carry Block:-

In the full adder using unique encoding diagram the Sum and carry blocks are built with pass transistors. And this Pass transistor can be replaced by the transmission gates for proper logic levels. According to the levels of the input the quaternary voltage levels are switched towards output. The Codes A0, A1, A2, A3, B0, B1, B2 and B3 are generated by the code generator block which is used to control these pass transistors
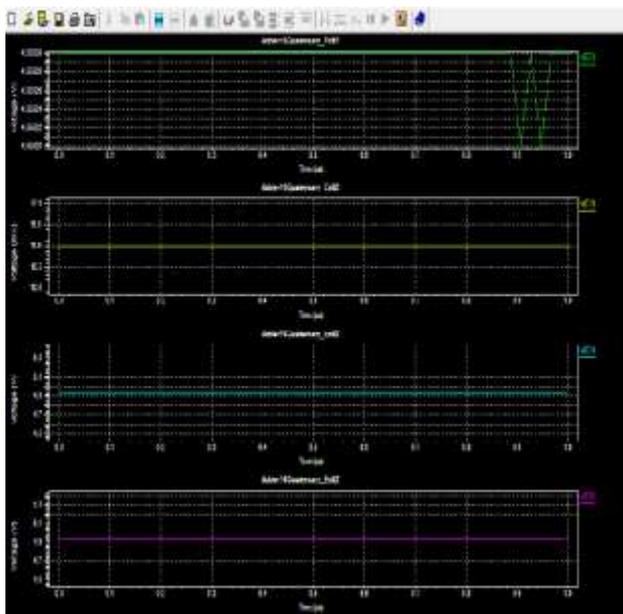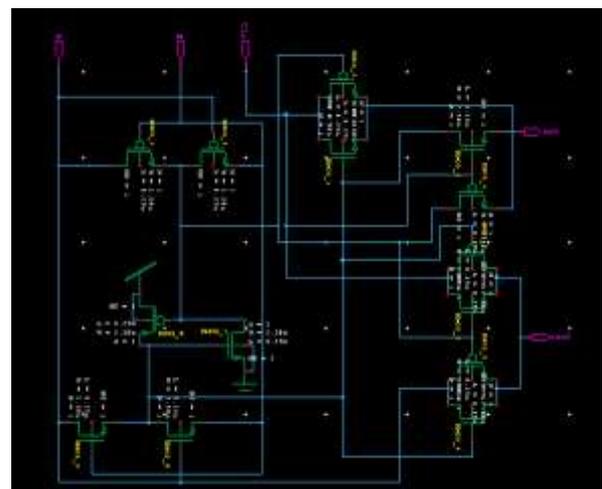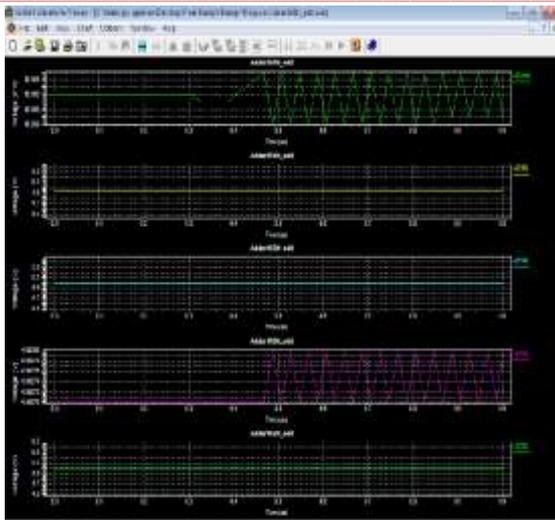

Figure 6: Logic Circuit Of Carry Block

Figure 7: Output Of Quaternary Binary Adder

Table I: COMPARISON

Author	Technology	Delay	Transistor Count	Average Power
Mr. t. R. Pardhi[1] 2014	180nm	1.4 ns	120	**394uw**
Hirokatsu Shirahama [4]2008	180nm	1.4 ns	**194**	**194uw**
Ricardo Cunha[7]2006	180nm	**2.24ns**	332	**181uw**
Proposed work	180nm	2.02ns	200	**210uw**

IV. FUTURE SCOPE

1) System will help to save the area because in quaternary it will design on a single chip that why area will be reduce.
2) It also used to reduce the transistor for design the circuit.
3) Circuit will also help to reduce the delay, Power consumption.

V. CONCLUSION

From latest research after studied various papers it is observed that work done on quaternary adder is very less. From literature review it is observed that they design and verify the single bit quaternary adder. In this paper, designing a 16-bit quaternary adder using various encoding techniques. In type I quaternary adder is required 200 transistors and 2.10 watt dissipates at 50nHz. In type II full adder circuit required 224 transistor and 2.91 watt dissipate at 50nHz. Simulation of the proposed circuit is carry out targeted for 180ns technology using tanner tool.

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