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Low Area, Low Power and High Bandwidth Operational Amplifier by 130nm CMOS Technology

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Abstract—A low power and high bandwidth CMOS Operational Amplifier has been designed in 130 nm CMOS Technology by Miller compensation technique and obtained a gain of 107 dB. A loop feedback is used to increase the bandwidth and results the final 3dB bandwidth 65 KHz and Unity gain bandwidth 2.3GHz. The proposed opamp providing 318 dB CMRR, 137 dB PSRR, 4.25 V/us Slew rate and 0.7 mW power dissipation. The overall design is simulated in 130nm digital CMOS technology in PSpice.

Keywords—*CMRR; PSRR; Operational Amplifier; high frequency*

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I. Introduction

Operational Amplifier (commonly called as Op-Amp) is the most common building blocks of many electronics systems. It is not only limited to analog system designingbut it is also used in mixed system. Op-Amp uses vastly different levels of complexity to comprehend functions ranging from dc bias generation to high speed filteringor amplification.[2-3] The single-stage amplifier having limitation of gain and bandwidth which is the main requirements and if increasing the stages it is difficult to maintain stability and power dissipations. Hence due to this reason commonly used two-stage Op-Amp so that this difficulty is can be revolved. The design of Op-Amps continues to pose a challenge as the transistors channel length and supply voltage scaled down with new generation of CMOS technology.To maintain the transistor in proper bias condition with low supply voltage is difficult. At different aspect ratios, there is a tradeoff among gain, speed, power and other performance parameters.**[**5**]**The proposed research work introduces to improve the critical parameters like DC gain, bandwidth while operating the low supply voltage.

As the transistor sizes shrink from micron to nanometer region in today's technology due to higher chip density demand so designer have to design the circuit withless area. As in the conventional Op-Amp to maintain the transistor in proper bias condition requires the bias circuitry which is designed with current source. To maintain the designed Op-amp stable is one of the challenging task, for maintaining this differentcompensation technique is used. Miller compensation is one approach to maintain stability which is used here. A capacitor requiredin this approach which maintains the pole locations for maintaining the stability. This approach also improves the bandwidth. Two mostimportant properties of analog circuitsare speed and accuracy however, optimizing this circuit for both aspects leads to contradictory demands. So finally high gain, low power and wide bandwidth two-stage Op-amp is presented in this paper.

II. Opamp Block Diagram

The block diagram of Op-amp consists differential amplifier input stages, gain stage and output buffer. These three stages plays important role in various aspects.

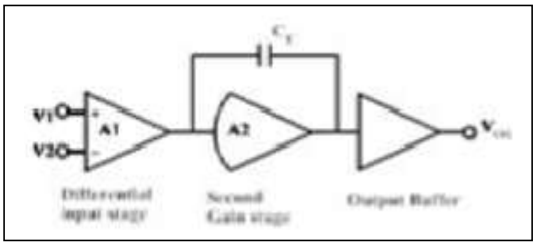

Fig. 1.Block diagram of Op-amp

The first stage of Op-amp is the differential amplifier which is also referred as "heart of Op-amp" having two inputs i.e. inverting and non-inverting. It provides differential output either voltage or current depending upon the input. This differential voltage or current is fed to the gain stage which act as the differential to single ended converter. This stage is in common source configuration. This stage has the important property of to increase the gain of first stage. The compensation capacitor is connected across second stage to improve stability. At last output buffer is used to reduce the output impedance of Op-amp.

III. Opamp design with Miller Compensation

The proposed Op-amp design is presented below in which miller capacitor is used. The differential amplifier includes transistors of M_1 to M_5 whereas transistor M_6 and M_7 presents the gain stage. Bias circuit is designed by using transistors M_8 and M_9 along with this miller capacitor which is connected across second stage is designed by using M_{10}. The most widely used compensation technique is miller compensation. This is also referred as pole splitting technique.A miller capacitor is used to split the poles, which causes the dominant pole move to lower frequency or nearest to the origin and thus providing ample stability.

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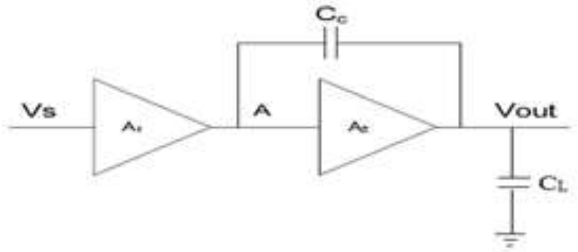

Fig. 2.Op-amp with miller capacitor

Above Figure shows the block diagram of a two-stage Op-amp employing Miller Compensationor Direct compensation technique. The Op-amp consists of an input differential pair stage having gain A_1. The second stage (output stage) is biased by the output of differential stage and driving a large capacitive load. This capacitor (C_C) is also known as bridging capacitor. Before the compensation, the poles of the two cascade stages are given as

$$P_1 = \frac{1}{R_1 C_1} \quad (1)$$

and

$$P_2 = \frac{1}{R_2 C_2} \quad (2)$$

where, R_k and C_k are the resistance and capacitances of this stages. In order to achieve dominant pole stabilization of the Op-amp, Miller compensation is used to perform pole splitting. A compensation capacitor is placed between the output of the whole amplifier to output of the first stage. After compensation the location of poles P_1 and P_2 is

$$P_1 = \frac{1}{R_1(C_1+(1+A_1)C_C)} \quad (3)$$

$$P_2 = \frac{1}{R_2(C_2+(1+\frac{1}{A1})C_C)} \quad (4)$$

After applying miller technique, capacitance seen in parallel in both side of second stage and location of poles before and after compensation is given below

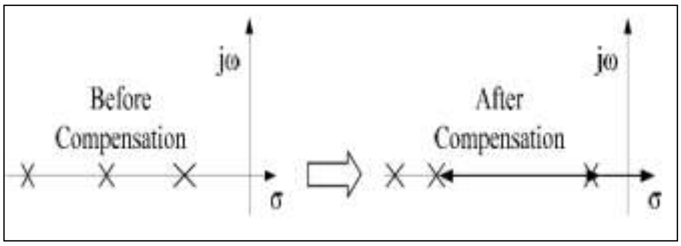

Fig. 3. Pole locations before and after compensation

Now the complete design of two-stage Op-amp is shown below in Fig. 4. The differential amplifier consist of current-Mirror configuration and differential input transistors pair. These differential input pair takes differential voltage and convert it into differential current. This differential current fed to the current-mirror configuration which act as a load for input stage and convert it into single ended current. The second stage consists of a common-source MOSFET convertingthe second-stage input voltage to current.

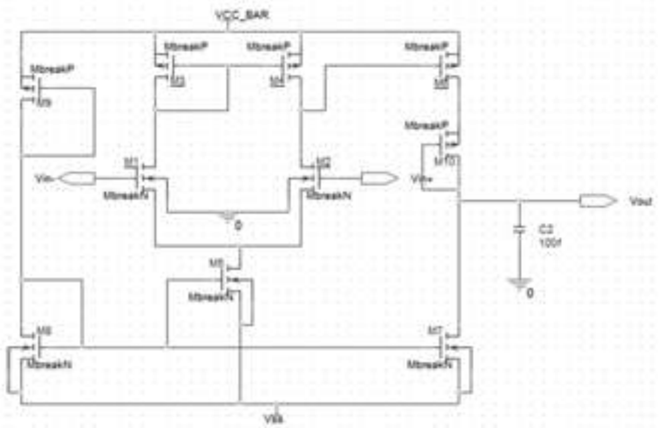

Fig. 4. Proposed Op-amp design

At last the transistor which converts the current to voltage at the output is loaded by a current-sink load; this stage is also nothing but the current-sink inverter. It is importantly to be noted that the current to voltage converter stage is referred as load stage and the voltage to current converter is referred as transconductance stage. The first stage is also to be important to increase the important parameters of Op-amp such as Input common mode range, slew rate and gain-bandwidthproduct. The current-mirror configuration designed by PMOS is to provide maximum input common-mode range similarly for gain-bandwidth product the input transistor pair is responsible. The gain-bandwidth (GBW) is maximizing by increasing the aspect ratio of input transistor. However another way to increase the GBW is toincrease the transconductance of first stage i.e. g_{m1}which is depended upon input current.

Mathematically it is represented as

g_{m1} = GBW× C_C (5)

The bottom transistor of first stage i.e. M_5 is to maintain the slew rate. Slew rate is mostly depended upon current I_5, which is given as

$$\text{Slew rate} = \frac{I_5}{C_C} \quad (6)$$

The second stage load is responsible for providing maximum output voltage swing. The overall gain of the Op-amp is given as the product of the first-stage and second-stage gain i.e.

$A_V = A_1 A_2$ (7)

where

$$A_1 = g_{m1} R_1 \quad (8)$$

and

$$A_2 = g_{m2} R_2 \quad (9)$$

where R_1 and R_2 is given as

$$R_1 = r_{ds2} || r_{ds4} \quad (10)$$

and

$$R_2 = r_{ds6} || r_{ds7} \quad (11)$$

IV. Op-Amp Design Issue

1). Theproposed Op-amp having Dual input unbalanced output differential amplifier who provides directly output to the second stage by using inverting and non-inverting input that’s the reason to choose this. There are no needs of calculationof gain for each stage.Power dissipation is one of the major tradeoffs for designing any analog circuit. Hence considering this parameter here worked at low supply voltage so there is no issue of power dissipation.

2). Due to the low area demand for high chip density the proposed Op-amp is design in low area compared to previous. This is to be done by using only transistors for overall design. As in the conventional Op-amp current source is used for proper biasing and miller capacitor which is connected from the output of differential amplifier to output of gain stage takes large die area. Here both of these componentsare replaced by the MOS transistors which take less area.

3). High bandwidth Op-amp is required for many applications. Hence this is to be taken account the Op-amp proposed is getting high bandwidth by employing negative feedback loop. However it decreases the gain but significantly improves the bandwidth.

4). Others parameters of Op-amp such as CMRR, PSRR, Slew rate, settling time is also efficient in this work. CMRR which is the ratio of differential mode gain to common mode gain is also high and PSRR describes the rejection capability of supply.

V. Simulation Result

Op-amp simulation is performed in PSpice EDA tool using 130nm digital CMOS technology. BSIMv3.0 is used as a model library. Comparative table on previous work is shown in TABLE I whereas TABLE II represents simulated results of this work. Frequency response of this Op-amp is also shown in fig. 4 where magnitude is in dB and frequency is in logarithmic plot.

TABLE I. Previous Work on Op-Amp

Parameter	[1]	[2]	[3]	[4]	[5]	[6]
Power Supply(V)	1.8	1.8	3	5	2.5	3.5
Gain (dB)	65	58.1	49	77	36.74	48
f_{-3dB} BW (MHz)	-	0.25	-	0.0013	7.33	-
UGB (MHz)	2300	205	2020	14	16.54	40
CMRR (dB)	96	-	39	80.9	133.6	-
PSRR (dB)	62	-	154	-	179.3	-
Slew rate (V/μs)	450	-	1.41	10.3	12.5	-
DC Offset (μW)	2%	-	-	-	-	-
Powerdiss. (mW)	25	-	0.039	-	0.804	-
Area (mm^2)	0.04	-	-	-	-	-
Phase Margin	-	84°	60°	53.4	48.1°	49.8°
Technology (nm)	180	500	180	350	180	180

TABLE II. Simulation Result Of Proposed Op-Amp

Parameter	Obtained Value
Power Supply	1.3 V
Gain	107 dB
f_{-3dB} Bandwidth	65KHz
Unity Gain Bandwidth	2.3 GHz
CMRR	318 dB
PSRR	137 dB
Slew rate	4.25 V/μs
DC Offset	22 μV
Power dissipation	0.7 mW
Area	111 μm^2
Technology	130 nm
Phase margin	60°
Settling time	0.58 μs

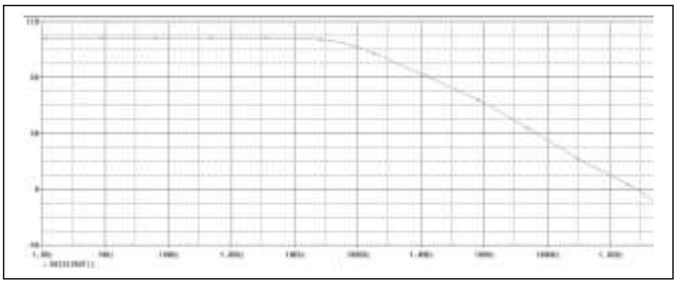

Fig. 5. Frequency response of Op-amp

VI. Conclusion

In this research worka high performance Op-amp is designed which operates at 1.3V supply. Less area, low power and wide bandwidth Op-amp is demonstrated in this design. For maintaining the stability miller compensation is used. Overall circuit is designed with only MOS transistor including bias circuit and compensation capacitor. High CMRR, PSRR as well as short settling time areachieved.

Acknowledgment

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