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Performance Analysis of Full Adder Circuits Using CMOS 90nm Technology

Aastha Gupta
B.Tech. Student
M.I.T, Moradabad
Moradabad, India
e-mail: 12.aastha.gupta@gmail.com

Akshay Goyal
B.Tech. Student
M.I.T, Moradabad
Moradabad, India
e-mail: me.akshaygoyal@gmail.com

Pragati Gupta
Assistant Professor
M.I.T, Moradabad
Moradabad, India
email: guptapragati30@gmail.com

Abstract: This paper represents designing of full adder circuit using CMOS 90nm technology. In this paper three full adder circuits have been proposed using 28 and 36 transistors and comparison analysis is done between 28T(a),28T(b) and 36T on the basis of area, power and number of transistors. By comparison it shows that proposed 28T(b) full adder circuit is better than 28T(a) and 36T full adder circuits as it required power less than other two circuits.

Keywords: *CMOS, Full Adder, VLSI, Transistor*

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I. INTRODUCTION

The number of components are increasing day by day in integrated circuits due to which the circuits are becoming more complex and due to the same reason the power consumption also increases with a rapid rate. Due to the increase in power consumption temperature of the circuit increases which affects the reliability of the circuit. With the increase in the power consumption the packaging and cooling cost goes up. Three major sources of power consumption in complementary metal oxide semiconductor (CMOS) circuits are:

1. Switching power due to output transistor.
2. Short circuit power due to current between V_{DD} and ground during switching.
3. Static power due to leakage and static currents. Static power consumption varies with the process technology.

The dynamic power of the circuit depends upon the charging and discharging of load capacitance which is given by

Dynamic power = $\alpha(V_{DD})^2 f C_l$ -----(1)

Where α is the switching activity, V_{DD} is the supply voltage, f is the switching capacity and C_l is the load capacitance. As the equation suggest power consumption mainly depends upon $V_{DD.}$ So by decreasing V_{DD} power consumption also decreases

As the need of portable device is increasing day by day ,so it is required to optimize power consumption of very large scale integration (VLSI) circuits. Power optimization is the basic constraint which is to be kept in mind designing the VLSI circuits.

An adder is a basic building block of various VLSI circuits like comparators, parity checkers, compressors etc. The performance of an adder circuit highly affects the overall capability of the circuit. Thus any improvement in an adder circuit will improve the capability of the whole system.

II. ADDERS

Basically an adder is of two types – half adder and full adder.

A basic full adder takes three inputs and computes two outputs that are denoted as sum and carry. A full can be easily assembled with the help logic gates, transistors, CMOS technology etc.

Table 1. Truth Table of a Full Adder

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Adder is one of the most important component of a processor. It is used in arithmetic logic unit (ALU) and in other parts of processor. Its use is increasing in mobile electronics devices such as cellular phones, laptops etc.

The basic operation performed in most of the components is the binary addition. So it need to be performed using low power, less area and at greater speed. There is no ideal full adder cell that can satisfy the requirements of all applications, so various architectures are proposed which have their own set of advantages and disadvantages.

III. SIMULATION

We have designed three full adder circuits with 28 transistors, 32 transistors and 36 transistors using CMOS technology.

Complementary metal oxide semiconductor (CMOS) consists of p-type metal oxide semiconductor (PMOS) and n-type metal oxide semiconductor (NMOS) transistors, in which source of PMOS transistor is connected to the drain of the NMOS transistor and there base is connected together. The input to the CMOS is applied to the base of the transistors and output is taken at the junction of the drain and source. When logic 1 is applied at the input the PMOS transistor behave as open circuited and the NMOS transistor behaves as short circuited due to which the output line connected to ground through the NMOS transistor and the output switches to 0 and when logic 0 is applied PMOS is short circuited and NMOS is open circuited thus the output line is connected to the supply and switches the output to logic 1. A CMOS circuit is shown in fig. 1

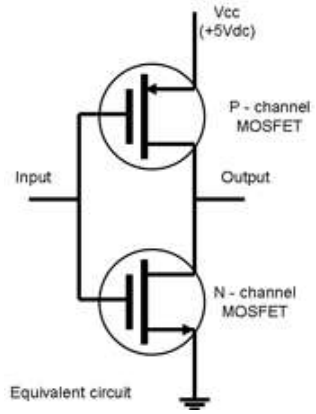

Fig. 1 CMOS circuit

The same concept is used for building the adder circuits using CMOS technology.
The schematic of 28T, 32T and 36T full adder circuits is shown in fig. 2, 3, 4 respectively.

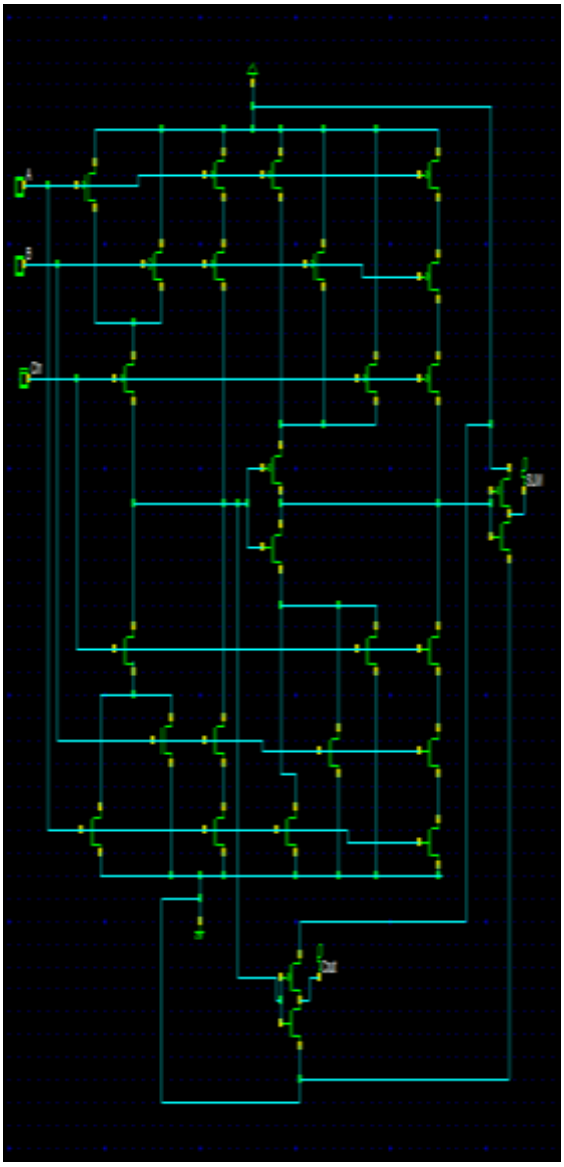

Fig. 2 Schematic of 28T full adder

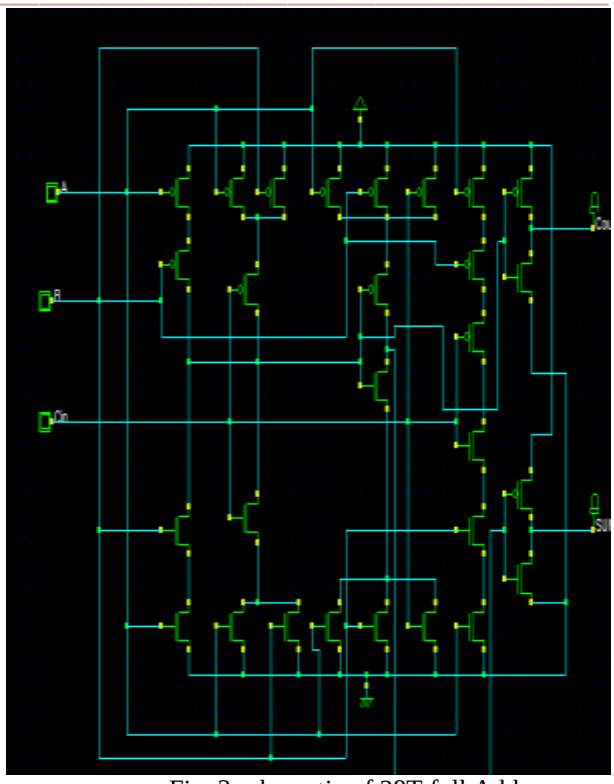

Fig. 3 schematic of 28T full Adder

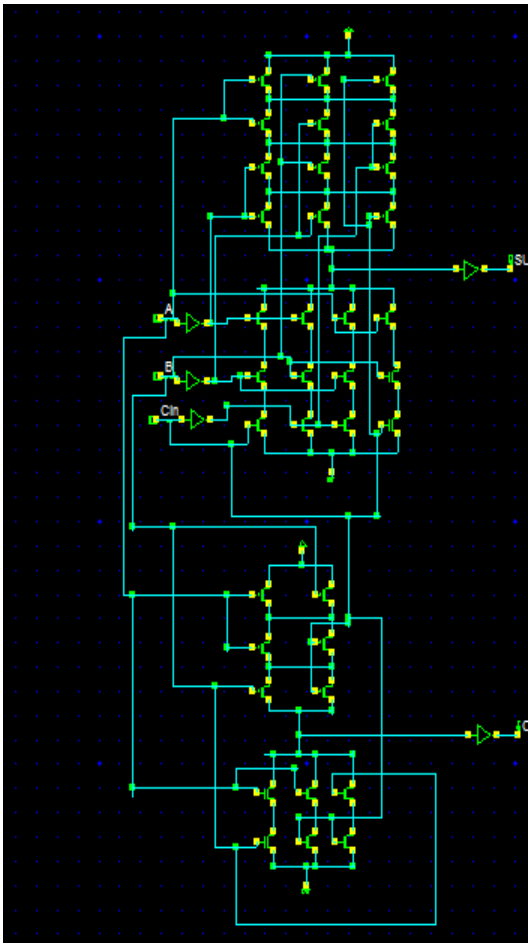

Fig.4 Schematic of 36T Full Adder

Timing diagram of schematics are shown in figures 5,6,7.

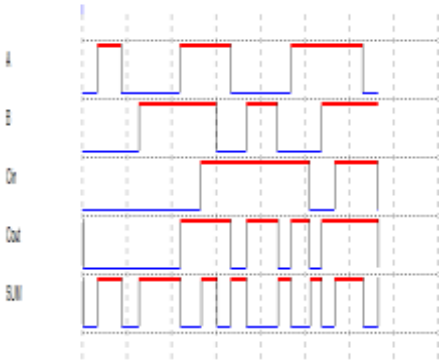

Fig. 5 timing diagram of schematic shown in fig. 2

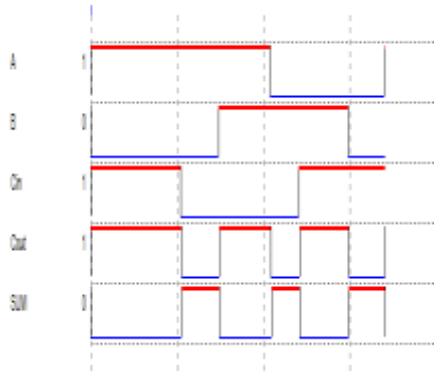

Fig.6 timing diagram of schematic shown in fig. 3

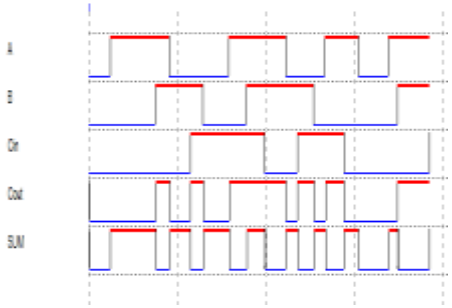

Fig. 7 timing diagram of schematic shown in fig. 4

Layout of schematics of full adder circuits is shown in fig. 8, 9, 10.

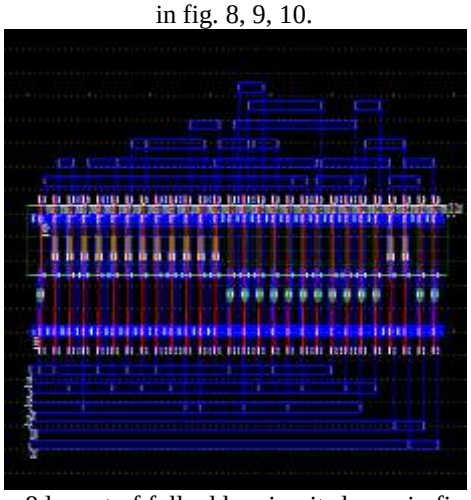

Fig. 8 layout of full adder circuit shown in fig. 2

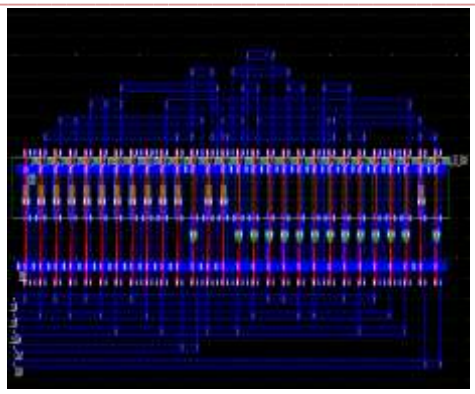

Fig. 9 layout of full adder circuit shown in fig. 3

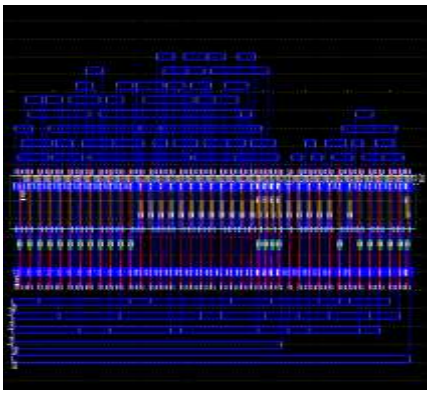

Fig. 10 layout of full adder circuit shown in fig.4

Timing diagram of layouts are shown in fig. 11, 12 ,13.

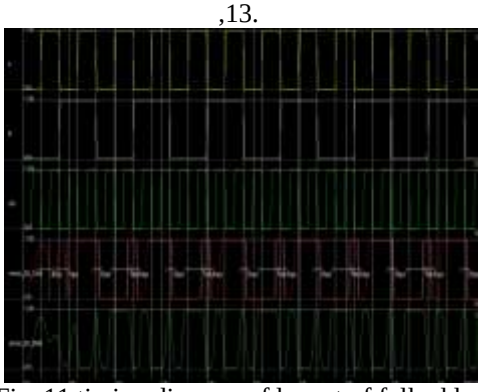

Fig. 11 timing diagram of layout of full adder shown in fig.8

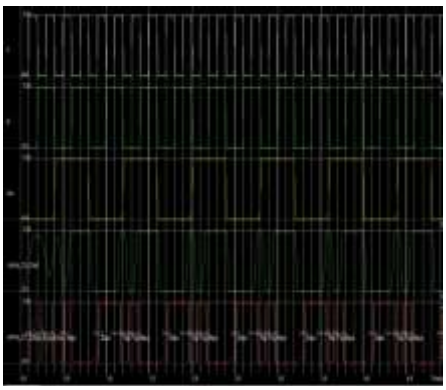

Fig. 12 timing diagram of full adder layout shown in fig. 9

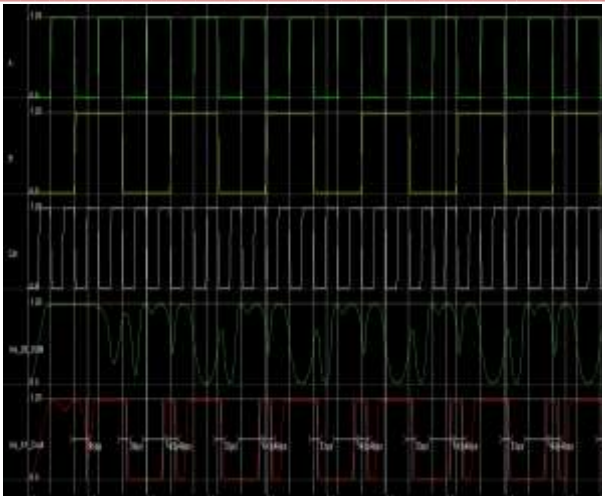

Fig. 13 timing diagram of full adder layout shown in fig. 1

IV. COMPARISION OF RESULT

Comparison is made between three proposed full adder circuits with respect to the height , width, area and power requirement.

The height, width and area of 28T(a) and 28T(b) full adder circuit are same as the number of transistors are equal(height=7.8µm,width=34.5µm and area=269.1 μm^2) whereas the height, width and area of the 36T full adder circuit is greater than that of 28T(height=8.6µm,width=48.1µm and area= 413.66μm^2), as shown fig. 14.

In 36T full adder circuit the power requirement is more as the number of transistor is greater than the number of transistors used in other two circuits. The power of 36T full adder circuit is 0.267 mW, for 28T(a) full adder circuit it is 0.152 mW and that of 28T(b) full adder circuit is 0.113 mW. The power requirement of 28T(a) full adder circuit is greater than that of 28T(b) full adder circuit though there are same number of transistors because the data path for both the circuits is different.

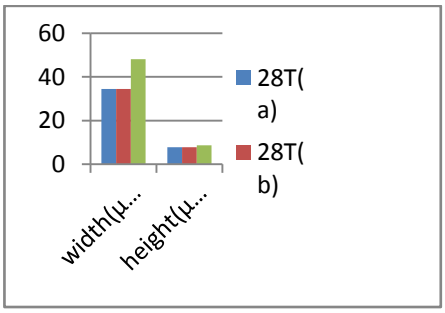

Fig. 14 Comparison of width and height,

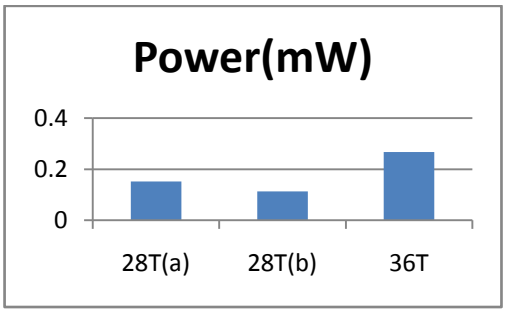

Fig. 12 Comparison of power

V. CONCLUSION

In this paper we have presented 3 full adder circuits using CMOS 90nm technology. Simulated results has shown that the power dissipated from different full adder circuit is dependent on number of transistors used and the data path. As 28T(a) and 28T(b) has same number of transistors but the power dissipated by both of them is different. Power dissipated by 28T(a) circuit is 1.34 times greater than the 28T(b) circuit and the power dissipated by the 36T circuit is 2.36 times greater than 28T(b) circuit.

Area required by the circuit mainly depends upon the number and type of components used as the area required by the 28T(a) and 28T(b) circuit is same and the area required by 36T circuit is 1.53 times greater than the area required by the other two circuits.

VI. REFRENCES

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