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# Validation of Octanary Adders in VHDL

Jasbir Kaur

Assistant Professor, E&CE Department,
PEC University of Technology
Chandigarh, India
*jasbirkaur70@yahoo.co.in*

Parv Sapra

PG Scholar, E&CE Department
PEC University of Technology
Chandigarh, India
*parvsapra@gmail.com*

*Abstract*—Adders being the lowest building block in circuits, if can handle more data then certainly it can lead to smaller Silicon Area, low power consumption & Higher speed which can help in increasing portability in devices.  Binary Logic Circuit design is limited by the number of bits that can be handled and interconnections. Multi Valued logic gives an extra dimension and thus extends the binary logic where more than two values can be dealt with.
This paper gives the concept of octanary adders, and its simulation on Xilinx ISE Design Studio 13.1

*Keywords*- *Multi Valued Logic, Octanary Adders, VHDL, Xilinx*
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## I.    INTRODUCTION

Computing machines deal with On's and Off's i.e. '1's and '0's, because of the widespread use of two valued primitives which govern their working. There have been advancements in the higher Radix systems, though the ease of the decimal system may take time to be achieved.

In Processors and other computing elements, adders play a pivotal role, not just for their use in arithmetic operations and ALU's but also other functions like incrementing and decrementing the various pointers and flag control, address calculation and maintaining of the table indices along with other similar operations.

Complexity of IC's is saturating to the point where majority of the Silicon real-estate is occupied with interconnections among devices thus the drawback. The first implication being increased system complexity with more number of pins. With increased density and interconnections leads to high chances of cross-talk. They limit the design of higher speed circuits, even more in the low power environment.

Speed of a processor is governed by the speed of the adders that make up the processor. Speed of any adder depends on the speed with which the carry is propagated. The more the number of states the lesser number of times a carry is generated which needs to be propagated. MVL (Multi-Valued-Logic) can be treated as an alternative to the more prevalent binary logic system. In Binary logic there are two states in OCTANARY there are 8 so the carry to be propagated is reduced a lot.

## II.    RELATED WORK

Multi-Valued Logic Synthesis by Robert K Brayton and Sunil P Khatri [1] has greatly motivated to extend the use of the binary logic system. Extension to the concept of Quaternary full adders based on output generator sharing proposed by Hirokatsu with reduction in delay and power [2] form the basis of this paper.

### A.  Idea of working of a Octanary Half Adder

Addition is basically counting. The concept is the same as taught to toddlers for better understanding. The Carry is the figure in the head whilst the numbers to be counted are those in the hand. The number added is equal to the skips in the levels. For Example 7(Y) is to be added to 2(X) , that means ' 2' two is the first number and '7' seven is the number to be added .

So we start and keep our pointer at '2'  and skip 7 levels. i.e. starting from two moving to level three is one skip. From three to four is the second skip and from four to five is the third and so on. So '7' skips after '2' lead to the position '1'(S). A carry is generated each time there is a crossing of '0'. The number of times '0' is crossed the carry is generated. Purpose of a carry- is to move to the next level. As soon as the numbers/levels finish the carry is a way that we can start again keeping a record of the number of times the numbers/ levels finished.
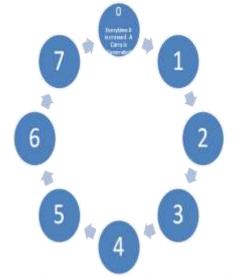


Figure 1: Circular Approach for Octanary Adders

Table 1: Truth Table of Octanary Half Adder

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| INPUTS | | OUTPUTS | | INPUTS | | OUTPUTS | |
|---|---|---|---|---|---|---|---|
| X | Y | Sum | Carry | X | Y | Sum | Carry |
| 0 | 0 | 0 | 0 | 4 | 0 | 4 | 0 |
| 0 | 1 | 1 | 0 | 4 | 1 | 5 | 0 |
| 0 | 2 | 2 | 0 | 4 | 2 | 6 | 0 |
| 0 | 3 | 3 | 0 | 4 | 3 | 7 | 0 |
| 0 | 4 | 4 | 0 | 4 | 4 | 0 | 1 |
| 0 | 5 | 5 | 0 | 4 | 5 | 1 | 1 |
| 0 | 6 | 6 | 0 | 4 | 6 | 2 | 1 |
| 0 | 7 | 7 | 0 | 4 | 7 | 3 | 1 |
| 1 | 0 | 1 | 0 | 5 | 0 | 5 | 0 |
| 1 | 1 | 2 | 0 | 5 | 1 | 6 | 0 |
| 1 | 2 | 3 | 0 | 5 | 2 | 7 | 0 |
| 1 | 3 | 4 | 0 | 5 | 3 | 0 | 1 |
| 1 | 4 | 5 | 0 | 5 | 4 | 1 | 1 |
| 1 | 5 | 6 | 0 | 5 | 5 | 2 | 1 |
| 1 | 6 | 7 | 0 | 5 | 6 | 3 | 1 |
| 1 | 7 | 0 | 1 | 5 | 7 | 4 | 1 |
| 2 | 0 | 2 | 0 | 6 | 0 | 6 | 0 |
| 2 | 1 | 3 | 0 | 6 | 1 | 7 | 0 |
| 2 | 2 | 4 | 0 | 6 | 2 | 0 | 1 |
| 2 | 3 | 5 | 0 | 6 | 3 | 1 | 1 |
| 2 | 4 | 6 | 0 | 6 | 4 | 2 | 1 |
| 2 | 5 | 7 | 0 | 6 | 5 | 3 | 1 |
| 2 | 6 | 0 | 1 | 6 | 6 | 4 | 1 |
| 2 | 7 | 1 | 1 | 6 | 7 | 5 | 1 |
| 3 | 0 | 3 | 0 | 7 | 0 | 7 | 0 |
| 3 | 1 | 4 | 0 | 7 | 1 | 0 | 1 |
| 3 | 2 | 5 | 0 | 7 | 2 | 1 | 1 |
| 3 | 3 | 6 | 0 | 7 | 3 | 2 | 1 |
| 3 | 4 | 7 | 0 | 7 | 4 | 3 | 1 |
| 3 | 5 | 0 | 1 | 7 | 5 | 4 | 1 |
| 3 | 6 | 1 | 1 | 7 | 6 | 5 | 1 |
| 3 | 7 | 2 | 1 | 7 | 7 | 6 | 1 |

### B. Octanary Full Adder(OFA)

The proposed Octanary full adder is constructed using the Octanary Half Adder. The block diagram of Octanary Full adder is shown in figure 2.
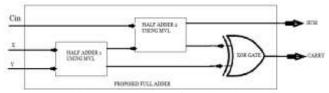


Figure 2: Concept of a Full Adder

The Octanary Full Adder is constructed by using two half adders and one XOR gate in a similar way as a conventional full adder. The first Octanary half adder is given with the two Octanary inputs X and Y. The second Octanary Half Adder is given one input as Cin and the other is the sum output of the first half adder. The sum output of the second half adder gives the sum of OFA. The carry output of the first half adder is given as one input to the XOR gate and the carry output of the second half adder is the second input to the XOR gate to get the carry output of the proposed full adder. The truth table of an Octanary Full Adder for carry = 0 and carry = 1 is given in table 2 & 3 respectively.

Table 2: Truth table of OFA with Carry = 0

| INPUTS | | | OUTPUTS | | INPUTS | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|
| Cin | X | Y | Sum | Carry | Cin | X | Y | Sum | Carry |
| 0 | 0 | 0 | 0 | 0 | 0 | 4 | 0 | 4 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 4 | 1 | 5 | 0 |
| 0 | 0 | 2 | 2 | 0 | 0 | 4 | 2 | 6 | 0 |
| 0 | 0 | 3 | 3 | 0 | 0 | 4 | 3 | 7 | 0 |
| 0 | 0 | 4 | 4 | 0 | 0 | 4 | 4 | 0 | 1 |
| 0 | 0 | 5 | 5 | 0 | 0 | 4 | 5 | 1 | 1 |
| 0 | 0 | 6 | 6 | 0 | 0 | 4 | 6 | 2 | 1 |
| 0 | 0 | 7 | 7 | 0 | 0 | 4 | 7 | 3 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 5 | 0 | 5 | 0 |
| 0 | 1 | 1 | 2 | 0 | 0 | 5 | 1 | 6 | 0 |
| 0 | 1 | 2 | 3 | 0 | 0 | 5 | 2 | 7 | 0 |
| 0 | 1 | 3 | 4 | 0 | 0 | 5 | 3 | 0 | 1 |
| 0 | 1 | 4 | 5 | 0 | 0 | 5 | 4 | 1 | 1 |
| 0 | 1 | 5 | 6 | 0 | 0 | 5 | 5 | 2 | 1 |
| 0 | 1 | 6 | 7 | 0 | 0 | 5 | 6 | 3 | 1 |
| 0 | 1 | 7 | 0 | 1 | 0 | 5 | 7 | 4 | 1 |
| 0 | 2 | 0 | 2 | 0 | 0 | 6 | 0 | 6 | 0 |
| 0 | 2 | 1 | 3 | 0 | 0 | 6 | 1 | 7 | 0 |
| 0 | 2 | 2 | 4 | 0 | 0 | 6 | 2 | 0 | 1 |
| 0 | 2 | 3 | 5 | 0 | 0 | 6 | 3 | 1 | 1 |
| 0 | 2 | 4 | 6 | 0 | 0 | 6 | 4 | 2 | 1 |
| 0 | 2 | 5 | 7 | 0 | 0 | 6 | 5 | 3 | 1 |
| 0 | 2 | 6 | 0 | 1 | 0 | 6 | 6 | 4 | 1 |
| 0 | 2 | 7 | 1 | 1 | 0 | 6 | 7 | 5 | 1 |
| 0 | 3 | 0 | 3 | 0 | 0 | 7 | 0 | 7 | 0 |
| 0 | 3 | 1 | 4 | 0 | 0 | 7 | 1 | 0 | 1 |

| | | | | |
|---|---|---|---|---|
| 0 | 3 | 2 | 5 | 0 |
| 0 | 3 | 3 | 6 | 0 |
| 0 | 3 | 4 | 7 | 0 |
| 0 | 3 | 5 | 0 | 1 |
| 0 | 3 | 6 | 1 | 1 |
| 0 | 3 | 7 | 2 | 1 |

| | | | | |
|---|---|---|---|---|
| 0 | 7 | 2 | 1 | 1 |
| 0 | 7 | 3 | 2 | 1 |
| 0 | 7 | 4 | 3 | 1 |
| 0 | 7 | 5 | 4 | 1 |
| 0 | 7 | 6 | 5 | 1 |
| 0 | 7 | 7 | 6 | 1 |

| | | | | |
|---|---|---|---|---|
| 1 | 3 | 4 | 0 | 1 |
| 1 | 3 | 5 | 1 | 1 |
| 1 | 3 | 6 | 2 | 1 |
| 1 | 3 | 7 | 3 | 1 |

| | | | | |
|---|---|---|---|---|
| 1 | 7 | 4 | 4 | 1 |
| 1 | 7 | 5 | 5 | 1 |
| 1 | 7 | 6 | 6 | 1 |
| 1 | 7 | 7 | 7 | 1 |

Table 3: Truth table of OFA with Carry = 1

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| Cin | X | Y | Sum | Carry |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 2 | 0 |
| 1 | 0 | 2 | 3 | 0 |
| 1 | 0 | 3 | 4 | 0 |
| 1 | 0 | 4 | 5 | 0 |
| 1 | 0 | 5 | 6 | 0 |
| 1 | 0 | 6 | 7 | 0 |
| 1 | 0 | 7 | 0 | 1 |
| 1 | 1 | 0 | 2 | 0 |
| 1 | 1 | 1 | 3 | 0 |
| 1 | 1 | 2 | 4 | 0 |
| 1 | 1 | 3 | 5 | 0 |
| 1 | 1 | 4 | 6 | 0 |
| 1 | 1 | 5 | 7 | 0 |
| 1 | 1 | 6 | 0 | 1 |
| 1 | 1 | 7 | 1 | 1 |
| 1 | 2 | 0 | 3 | 0 |
| 1 | 2 | 1 | 4 | 0 |
| 1 | 2 | 2 | 5 | 0 |
| 1 | 2 | 3 | 6 | 0 |
| 1 | 2 | 4 | 7 | 0 |
| 1 | 2 | 5 | 0 | 1 |
| 1 | 2 | 6 | 1 | 1 |
| 1 | 2 | 7 | 2 | 1 |
| 1 | 3 | 0 | 4 | 0 |
| 1 | 3 | 1 | 5 | 0 |
| 1 | 3 | 2 | 6 | 0 |
| 1 | 3 | 3 | 7 | 0 |

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| Cin | X | Y | Sum | Carry |
| 1 | 4 | 0 | 5 | 0 |
| 1 | 4 | 1 | 6 | 0 |
| 1 | 4 | 2 | 7 | 0 |
| 1 | 4 | 3 | 0 | 1 |
| 1 | 4 | 4 | 1 | 1 |
| 1 | 4 | 5 | 2 | 1 |
| 1 | 4 | 6 | 3 | 1 |
| 1 | 4 | 7 | 4 | 1 |
| 1 | 5 | 0 | 6 | 0 |
| 1 | 5 | 1 | 7 | 0 |
| 1 | 5 | 2 | 0 | 1 |
| 1 | 5 | 3 | 1 | 1 |
| 1 | 5 | 4 | 2 | 1 |
| 1 | 5 | 5 | 3 | 1 |
| 1 | 5 | 6 | 4 | 1 |
| 1 | 5 | 7 | 5 | 1 |
| 1 | 6 | 0 | 7 | 0 |
| 1 | 6 | 1 | 0 | 1 |
| 1 | 6 | 2 | 1 | 1 |
| 1 | 6 | 3 | 2 | 1 |
| 1 | 6 | 4 | 3 | 1 |
| 1 | 6 | 5 | 4 | 1 |
| 1 | 6 | 6 | 5 | 1 |
| 1 | 6 | 7 | 6 | 1 |
| 1 | 7 | 0 | 0 | 1 |
| 1 | 7 | 1 | 1 | 1 |
| 1 | 7 | 2 | 2 | 1 |
| 1 | 7 | 3 | 3 | 1 |

### C. Comparison of an Octanary Full Adder v/s Conventional Full Adder:-

The basic principle of any adder is to add two numbers; a better adder is which does the job in the fastest manner possible. Below is a comparison on how two possible additions can take place.

- Octanary Addition



- Bit By Bit Addition



The Number of carries involved in the Octanary Adder are 4, whilst the number of carries to be taken care of, in the binary addition of the same numbers is 12. This also shows that the wiring complexity is also greatly reduced.

### III.    SIMULATION RESULTS



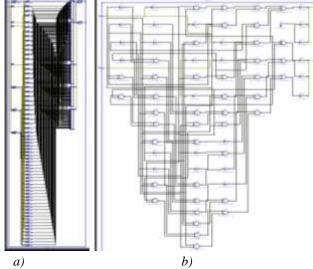*a)*                                          *b)*

Figure 3: (a) Schematic Symbol of Octanary Half Adder created in Xilinx.
(b) Technology Schematic Symbol of Octanary Half Adder created in Xilinx.

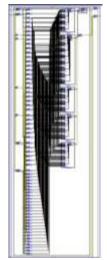Figure 4: Output Waveform of Octanary Half Adder in Xilinx



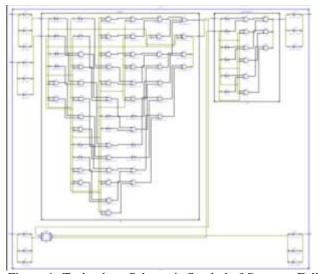Figure 5:  Schematic Symbol of Octanary Full Adder created in Xilinx.



Figure 6:  Technology Schematic Symbol of Octanary Full Adder in Xilinx



Figure 7: Output Waveform of Octanary Full Adder in Xilinx

## IV.   CONCLUSION

The Octanary Full Adder using Octanary Half Adders can transmit more data and information than its binary counterparts. The simulated output waveform of the Octanary Adders is obtained and the results verified from the truth tables.

Advantages like increased computational ability, less wiring complexity, are some which make such adders using MVL more favourable and increase their importance in the future. Applications of this may be used in DSP, Communication and Memory Elements.

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