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20W Output Broadband Amplifier with Automatic Gain Control and Thermal Protection

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***Abstract*—** The requirement is to explore concept, design, fabrication and testing of a common source class B, cwrf amplifier by using readily available MOSFET that can withstand a load mismatch at all phase angles with more than a VSWR of 20:1. This amplifier must give an output of more than 20W with 13dB gain in the frequency range of 28 to 46MHz i.e. 37 ± 9MHz. This module will make one of the stages for a multistage cascaded high power cwrf solid state amplifier. The amplifier must be over current and over voltage protected by using external self-regulated dc power supply at the drain. The amplifier MOSFET device is presently to be biased at the gate with a variable dc supply. This arrangement will make it gain controlled. This will be feed backed from the cwrf output so as to make it automatic gain controlled in future. Various techniques of sampling forward and reflected power at the output must also be explored. A thermoswitch at the heat sink of MOSFET is to be added along with necessary circuitry to regulate the operating temperature, thereby protecting the device from overheating.

Keywords- *VSWR, impedance matching, SSPA*

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I. INTRODUCTION

The cwrf solid state low, medium and high power amplifiers are most demanding and costly modules of all communication receiver and transmitter systems for very low intensity base signals. The low power amplifiers (LPA) of 1µW to 1W, medium power amplifiers (MPA) of 1W to 100W and high power amplifiers of more than 100W have various other applications in industries, medical and scientific experiments depending upon the output power, gain, operating frequency range, signal to noise ratio, efficiency, load fluctuation withstanding etc. The mechanical features like shape, size and weight etc. of amplifiers and related accessories including power supplies and cooling are crucial also. These parameters are important while selecting available cwrf amplifier for a particular application.

There are prescribed frequency bands like 13.553 to 13.567MHz, 26.957 to 27.283MHz and 40.66 to 40.70MHz etc. for the Communication, Industrial, Scientific and Medical applications. In our particular work i.e. scientific applications, there are no boundaries in terms of frequencies, power output, mismatched load, signal to noise ratio, compactness etc. Most of the commercially available solid state modules are either unprotected and goes bad quite often or very costly. These mostly need importing. Therefore, custom made i.e. in house development of the rf amplifiers as per need of the application is very popular.

II. MOTIVATION AND OBJECTIVE

The project is to initially understand the requirement and explore conceptual design of the cwrf amplifier. Finally, design, fabrication, testing and performance optimization is to be carried out for a 20W output cwrf amplifier module. The required cwrf drive of 1W maximum would be available from another ongoing project. The proposed module in turn must be able to provide 20W maximum thus a gain of 13dB at least. This may be useful as output stage or driver stage for another under development amplifier stage for more than 200W cwrf power output in the frequency range of 28 to 46MHz i.e. 37 ± 9MHz.

The amplifier module is decided to be made by using MOSFET for the want of required output power, bandwidth, higher gain and load mismatch withstanding etc. The amplifier is to be operated in common source class B for lower harmonic level in the output and ease of controlling gain with biasing at the gate. The amplifier is made over current and over voltage protected by using external self-regulated dc power supply at the drain.

The M/A-COM make rf MOSFET MRF137 is selected out of the available choices from various manufacturers due to expected optimized performance as per requirement. This is N-Channel enhancement mode device, made for wideband large signal output and drive stages up to 400MHz. This device can be operated in class A and facilitates manual or auto gain control. This comes tested for load mismatch at all phase angles with 30:1 VSWR under given circumstances. This is made to deliver a maximum of 30W at 150MHz while using 28V supply with a minimum gain of 13dB and efficiency 60% in class BC. Total device dissipation capability is 100W at 25ºC ambient and de rates at 0.57W/ºC.

The requirement to withstand load mismatch while operating the amplifier must be well understood. The standing waves occur due to interference of reflected power with forward waves in output circuitry. A cwrf amplifier must have good source-load impedance correlation at varied input power and bias voltages. Otherwise, standing waves may lead to junction breakdown and device failure.

The intensity of Standing Waves is referred to as VSWR. VSWR, reflection coefficient, mismatch loss and return loss can characterize impedance mismatch and ultimately power transfer to the load. Following terms must be well understood,

Reflection coefficient (T) $= (Z_L-Z_S)/(Z_L+Z_S)$
VSWR $= E_{max}/E_{min} = (E_{inc}+E_{ref})/(E_{inc}-E_{ref}) = (1+T)/(1-T)$
Return loss $= 10 \log(P_r/P_i) = 20 \log(E_r/E_i)$
Mismatch loss $= 10 \log(1-T^2)$

For example: with output mismatch of VSWR 10:1, 67% of the output power is reflected back by the load to the MOSFET while only 33% is transmitted. An efficient amplifier design must ensure that the reflected power should not damage the device and keep functioning at de rated value.

III. Amplifier Protection Scheme

In rf and microwave sources including amplifiers there are four most relevant ways in general for protecting devices from reflected power. These are,

(a) Self regulated power supply
(b) Output power feedback controlled power supply
(c) Output power feedback controlled input attenuator
(d) Output power feedback controlled output gain control

The generalized protection scheme is shown in figure 1. These mechanisms aim at MOSFET output power control via various means.

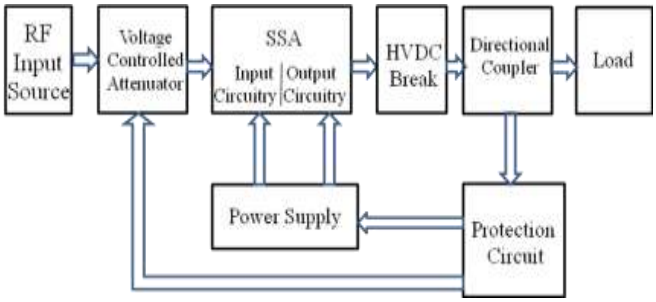

Figure 1. Block Diagram of Generalized Protection Scheme

Directional coupler samples the forward and reflected rf output power signals in terms of corresponding voltages. Protection circuit acts to rectify, filter and generate proportionate dc voltage level. The protection circuit includes comparator circuits that operate on received and reference voltage signal to produce an error signal. This error signal acts as input to the voltage controlled attenuator, automatic gain control and power supply regulator control.

Power supply is regulated by means of voltage divider network to control the amplifier drain biasing also.

IV. Amplifier Simulation with TINA

As no software other than TINA is available for performing simulations of amplifier circuit with desired MOSFET and power, various amplifier circuits of lesser power were designed and simulated in order to learn the procedure. Variations in nature of impedance matching networks, bypass capacitor networks and biasing networks were examined. Different device modules i.e. input and output were also simulated separately. The best possible Solid State Amplifier input and output circuit simulated by TINA are shown in Figure 2 and 3 respectively.

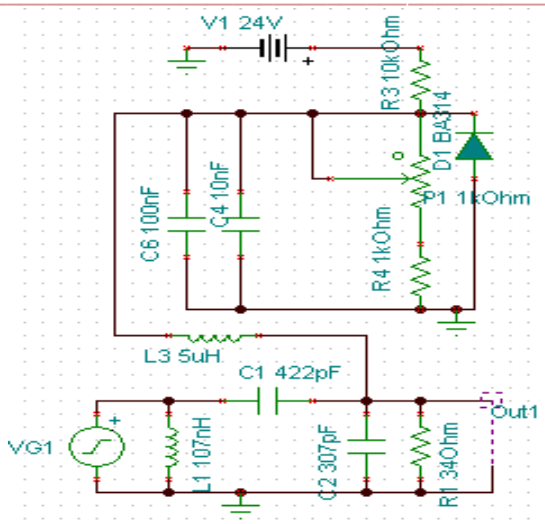

Figure 2. Simulated amplifier input circuit

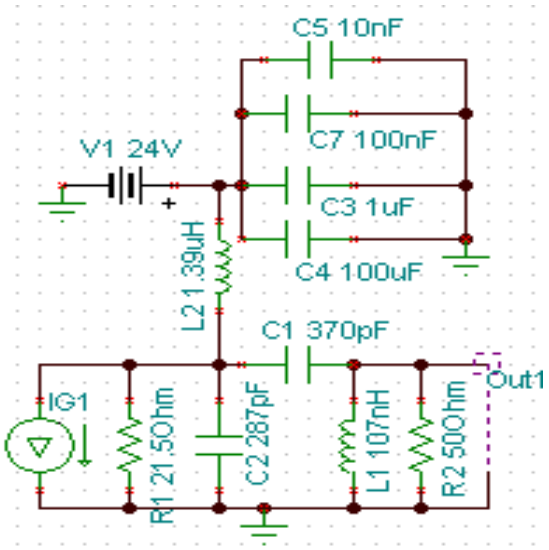

Figure 3. Simulated amplifier output circuit

This can be seen in figure 2 that a voltage source of 20.2V and 50Ω internal impedance has been coupled with characteristic input impedance of MOSFET i.e. 34-j14 through high pass filter. A network of resistors and 4V zener diode has been used to improve the MOSFET gate biasing.

In figure 3, current source of 4.24A is connected in parallel to characteristic output impedance of MOSFET i.e. 21.5-j15. Circuit output side is matched with 50Ω line impedance through high pass filter.

V. Design Calculations

For the Solid State Power Amplifier (SSPA) under consideration, available cwrf input power is 1W maximum thus $V_{rms}^2/R = 1$. For R = 50Ω, we get

$$V_{pp} = 2*(2)^{1/2}* V_{rms} = 20.2V$$

Maximum output of input circuit is,

$$V_M = 15.3/(2*(2)^{1/2}) = 5.45V$$

Minimum output of input circuit is

$V_m = 11/(2*(2)^{1/2}) = 3.9V$

Trans conductance of MRF137 is r = 750 mmhos, therefore
Maximum output current is $V_M*r = 5.45*(0.75) = 4.1A$
Minimum output current is $V_m*r = 3.9*(0.75) = 2.92A$

At 37MHz and 4.1A, Maximum output power of the amplifier is $P_{max} = V_{ppo}^2/(8*R) = 135^2/(8*50) = 45W$.
At 28MHz and 2.92A, Minimum output power by amplifier is $P_{min} = V_{ppo}^2/(8*R) = 80^2/(8*50) = 16W$.

Thus simulated output power range of amplifier = 16-45 W.

VI. Simulation Results

Simulated output waveforms of MRF137 input circuit on TINA Virtual Oscilloscope are shown in figure 4. The reading of 15.34V was taken with 20.2V input at 37MHz.

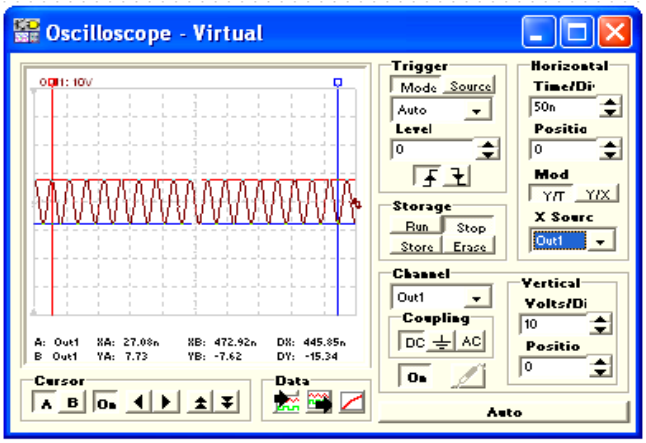

Figure 4. Maximum output by amplifier input side

Simulated output waveforms of MRF137 output circuit on TINA virtual oscilloscope are shown in figure 5. The reading with input of 4.1A was taken at 37MHz. It can be seen, there is no noise, amplitude or phase modulation in the output.

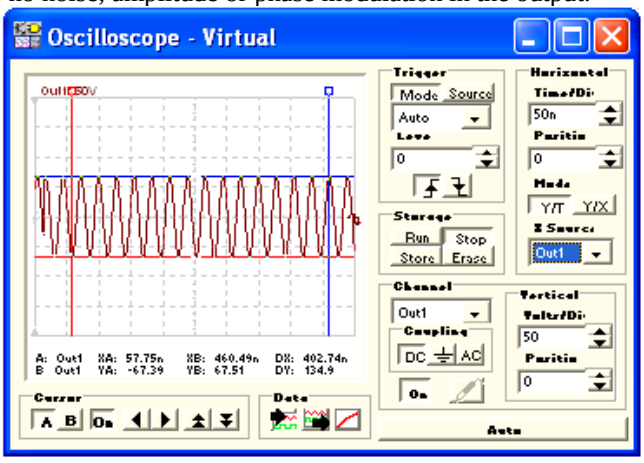

Figure 5. Maximum output by amplifier output side

VII. Practical Circuit Fabrication

The input and output circuits are fabricated on rf compatible 2mm thick insulation material. These are mounted on the same heat sink while making short connections with the MRF137. The fabricated circuit and overall amplifier module are shown in figure 6a and 6b.

Figure 6a. Fabricated amplifier circuit

Figure 6b. Overall view of the amplifier module

The input circuitry consists of the following components,
(a) Gate biasing filter capacitors: 100kpF and 10kpF
(b) Voltage divider resistor network: 1kΩ and 10kΩ
(c) Zener diode for over voltage protection: 5V
(d) Emitter follower to regulate MRF137 gate bias: 2N2222A
(e) Series bias resistor to control MOSFET impedance response
(f) LC tank circuit to match impedance between MOSFET and source: 310nH and 420pF

The output circuitry consists of the following components,
(a) 24Vdc supply filter capacitors: 1kpF and 10kpF
(b) Drain RFC: 0.7uH
(c) Bypass capacitor network to couple any RF noise from MOSFET to ground: 1kpF, 100kpF and 10kpF
(d) LC tank circuit to match impedance between MOSFET and load: 190nH and 390pF

The MOSFET MRF137 can be seen mounted directly on the heat sink that is forced air cooled with 75x75mm Rexnord make electronic fan. A thermo-switch is mounted on the heat sink to protect the MOSFET by open circuiting the drain supply in case of overheating above 60ºC. The fabricated SSPA is tested with the help of,
(a) A signal source, 1W amplifier, gate biasing supply and oscilloscope at the input.
(b) Dummy load, drain biasing supply, multi tester and oscilloscope at the output.

The drain is operated at 24V and the gate bias varied from 0 to 2.5V is found providing quiescent current of 0 to 60mA. The system has been tested for varying input power from 40 to 200mW. Table1a, 1b and 1c displays the response of SSPA i.e. Pout at various input power (P_i) and gate bias (V_G).

Table1a. Solid state amplifier power output for P_i=40mW.

S.No.	Operating Frequency	Power Output (P_{out})		
		V_G=0V	V_G=1V	V_G=2V
1.	28 MHz	0.00W	0.21W	1.64W
2.	30 MHz	0.00W	0.25W	2.00W
3.	32 MHz	0.00W	0.28W	2.10W
4.	34 MHz	0.01W	0.36W	2.60W
5.	36 MHz	0.01W	0.40W	3.40W
6.	38 MHz	0.02W	0.44W	4.10W
7.	40 MHz	0.02W	0.49W	4.80W
8.	42 MHz	0.02W	0.56W	5.70W
9.	44 MHz	0.03W	0.60W	5.80W
10.	46 MHz	0.03W	0.64W	5.60W

Table1b. Solid state amplifier power output for P_i=120mW.

S.No.	Operating Frequency	Power Output (P_{out})		
		V_G=0V	V_G=1V	V_G=2V
1.	28 MHz	0.7W	2.8W	6.4W
2.	30 MHz	0.8W	3.1W	7.8W
3.	32 MHz	1.0W	3.7W	8.5W
4.	34 MHz	1.3W	4.1W	11.6W
5.	36 MHz	1.4W	5.0W	15.0W
6.	38 MHz	1.7W	6.3W	15.7W
7.	40 MHz	1.8W	7.8W	15.7W
8.	42 MHz	2.0W	9.0W	14.4W
9.	44 MHz	2.2W	9.1W	13.8W
10.	46 MHz	2.5W	9.1W	12.3W

Table1c. Solid state amplifier power output for P_i=200mW.

S.No.	Operating Frequency	Power Output (P_{out})		
		V_G=0V	V_G=1V	V_G=2V
1.	28 MHz	2.6W	6.3W	11.3W
2.	30 MHz	3.0W	7.4W	13.7W
3.	32 MHz	3.5W	8.3W	15.3W
4.	34 MHz	3.9W	8.6W	19.4W
5.	36 MHz	5.0W	12.2W	20.8W
6.	38 MHz	6.3W	15.0W	20.1W
7.	40 MHz	6.3W	15.0W	20.1W
8.	42 MHz	8.4W	14.7W	18.5W
9.	44 MHz	8.9W	14.1W	17.6W
10.	46 MHz	9.0W	13.8W	15.7W

Desired maximum output power of more than 20W is obtained for input of 200mW at gate bias of 2V in the frequency range of 36 to 40MHz. At operating voltage of 24Vdc, drain current of 1.26A is drawn at output power of more than 20W. Thus, a gain of 20dB and efficiency of 66% is obtained. A -3dB power bandwidth of 28 to 46MHz is found available as required. The data clearly indicate variation of amplifier gain with changing gate voltage by a remote wired source which may be replaced with output voltage feedback in future.

VIII. Output Response Curves

The data of observation Tables1c is plotted for visual feel of the output power with frequency response and gain control of the SSPA with gate bias. In Figure 7, SSPA response at input power of 200mW with various 0 to 2.5V gain control gate bias is displayed.

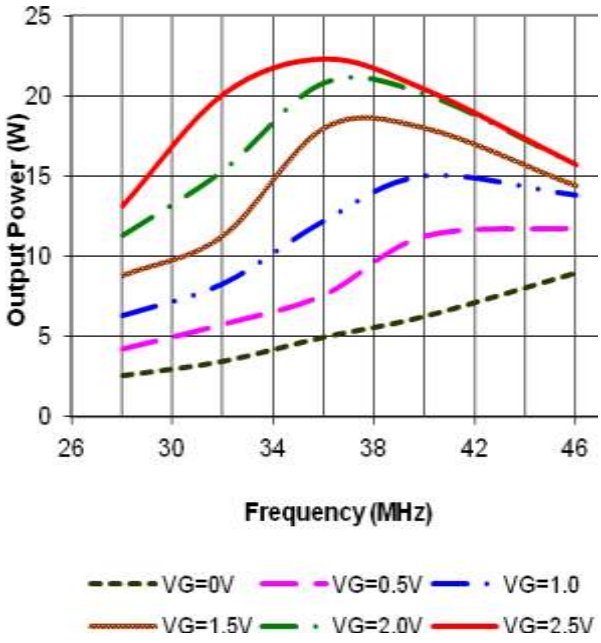

Figure 7. Solid State Power Amplifier response for P_i=200mW

It can be observed that the output power varies from 16 to 22W over 30-46MHz for V_G=2.5V. This indicates that higher output power and gain may be obtained in class A mode of operation if desired in future at the expense of efficiency.

IX. Conclusion

The assigned project work i.e. 20W output broadband amplifier with automatic gain control and thermal protection is successfully completed. The detailed design including simulation of the amplifier by using 'input and output i.e. two circuit halves' through TINA is accomplished and presented. The SSPA is fabricated as per simulation and systematically tested. Enough exposure with instrumentation is gained while testing before and after required modifications. The targeted output, bandwidth and gain are found available. The SSPA could not be tested for high VSWR but simulation and analysis indicate a rugged 20W power amplifier. Gain of the SSPA found variable with external control bias and thermal protection is added successfully.

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