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Design of Ternary Memory Cell Using QDGFET

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***Abstract*—** Ternary logic is able to handle higher data in less number of gate counts. So it can be said that it is a promising option to running binary logic. So this approach is very cost effective as less number of gates require less area in a chip. A novel design of a ternary memory cell based on QDGFETs is proposed. Two B2B (Back to Back) connected inverters are use to make memory cell. It is the regular 6T memory cell design. Hence the advantage of QDGFET is that it does not do any change and can be used directly in the circuit by replacing CMOS. Embedded memory requires the largest share of area in modern high-performance circuit designs. As the technology progresses the demand for high capacity memories also increases. So to fulfil this demand, researchers are trying to come up with new technology and solutions. The use of ternary logic instead of binary logic is a possible solution. So in this research ternary memory cell is designed which can store one bit of ternary logic data.

Keywords*-QDGFET, VLSI, Ternary Logic, MVL, Ternary Memory*

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I. INTRODUCTION

A conventional FET conducts based on the applied voltage in its gate terminal. When the gate voltage is higher than the threshold voltage of the FET, an inversion layer is formed underneath the gate region which allows charge carriers to flow from the source region to the drain region of the transistor. According to Moore's law, the number of transistor in the integrated circuits doubles after every 2 years. There are two approaches to follow Moore's law: one is to decrease the dimensions of the electronic devices and the other one is to increase the bit-handling capacity per device. As the different dimensions of the device decrease, other issues like gate leakage current [1]–[3], ON–OFF ratio as well as the noise margin, and so on also degrade. So the second approach, which is, to increase the bit-handling capacity of transistor, becomes more important to achieve Moore's law.

Multivalued logic (MVL) has the following advantages.

- In MVL, each wire can transmit more logic state than a binary component. As a result, the number of connections within the chip is reduced.
- Since each MVL component can process more information than a binary element, the complexity of circuits may be decreased.
- The ON- and OFF-chip connections can be reduced to assist alleviate the pin-out difficulties that arise with increasingly larger chips.
- The speed of serial information transmission will be quicker because the transmitted information per unit time is increased.

However, theory also predicts several disadvantages of using MVL circuits.

- For fixed values of the highest and the lowest voltages, the tolerances of the MVL circuits with more logic levels will be more crucial than the binary circuits.
- To realize low-output impedance, additional sources of power are necessary to produce the intermediate voltage outputs.
- The process technology for the MVL circuit may be more complex because the elements in a circuit must deal with multivalued signals.

There are many applications of ternary logic circuits. The main advantage of the ternary logic circuit is the high density of logic elements. For example, in an N bit processor, the number of bits per word that needs to be stored is N2, whereas in the ternary logic, the number of bits per word should be $N * \log 32$. Three-valued memory can reduce 37% overall area of the upcoming microprocessor units. The number of memory cells and hence the capacitance of both the bit lines and the word lines also decreases using three-value logic circuit, which can produce significant advantage in terms of the read power and the write power [4]. The comparison of a binary full adder and a ternary full adder in terms of delay, power, and power-delay product is discussed in other works [4].

The drawback of three-valued logic circuit is the static power dissipation. But since the number of circuit elements is less in the ternary logic, the total power is also less for the large memory size. For large memory size, ternary logic can noticeably reduce the area and the power consumption.

MVL can be implemented using different kinds of devices like resonant tunneling diodes [5], [6], resonant tunneling transistors [7]–[8], modulation-doped FETs [9]–[11], high electron mobility transistors [13]–[15], carbon nanotube field effect transistors (CNTFETs), single electron transistors (SETs), and so on. Among these semiconductor devices, CNTFET, SET and QDGFET are the most promising devices to implement the MVL in future.

In the CNTFET based ternary logic circuits [18], the circuit design is based on different CNTFETs which have different Vth based on the CNTFET is different than the conventional CMOS architecture. In the resistor based CNTFET circuits, the value of the resistor is so high that it is difficult to fabricate on the chip. Whereas, the conventional CNTFET-based circuit has more number of elements than that in the CMOS circuit, for example, standard ternary inverter (STI) has six CNTFETs. Besides this uniform CNTs having same diameter and similar orientation are difficult to fabricate.

On the other hand, the main problems of SET-based [19] logic implementation is lithography techniques, background

charge, co-tunneling, and room temperature operation. Two major drawbacks of the SET as an electronic circuit component are, it does not have internal memory and it cannot carry direct current, so that an ultrasensitive electrometer is necessary to measure its charge state.

Randomness of the background charges of an SET may also produce capacitive coupling between the different gates of the different transistors.

Direct copying of CMOS circuits using SET is impossible, and in order to get substantial parameter margins, even the simplest logic gates have to be redesigned. Besides this, their operation range starts shrinking under the effect of thermal fluctuations as soon as their scale kBT reaches approximately 0.01 E.

Because of the presence of quantum dots in the gate region, QDGFET produces one extra intermediate state between its two stable states in its transfer characteristics [15], [16]. The generation of the intermediate state can be explained by the resonant tunneling of charge carriers from the inversion layer to the quantum dots on top of the gate region. Because of the quantum dots in the gate region are cladded by a high band gap insulator, charge leakage for these devices are very small, which gives the stability to the generation of the intermediate state between its normal ON and OFF states. Another advantage of QDGFET is that it can be fabricated in conventional CMOS process at room temperature. The quantum dot self-assembly is also performed at room temperature. The threshold voltage of QDGFET can be controlled easily either by changing the gate insulator thickness or changing the number of quantum dot layers on top of the gate region. The background charge problem of SET is also absent in QDGFET. In our proposed circuit design, we use QDGFET as the key circuit element which itself can produce three stable states in its transfer characteristics. QDGFETs can be used in the conventional CMOS architecture to implement ternary logic circuits. The design complexity will decrease when implementing ternary logic circuits based on QDGFET.

In three-value logic circuit, one more substantial drawback is that none of the transistors in each complementary pair is closed too well, so that the static leakage current in these circuits is fairly substantial. The static power consumption for relatively large devices operating at helium temperatures is negligible. However, at the prospective room temperature operation, this power becomes on the order of 10−7 W per transistor. Though apparently low, this number gives an unacceptable static power dissipation density (>10 kW/cm2) for the circuits which would be dense enough (>1011 transistors per square centimeter) to present a real challenge for the prospective CMOS technology. Static leakage current flow in QDGFET based ternary logic circuit is very low.

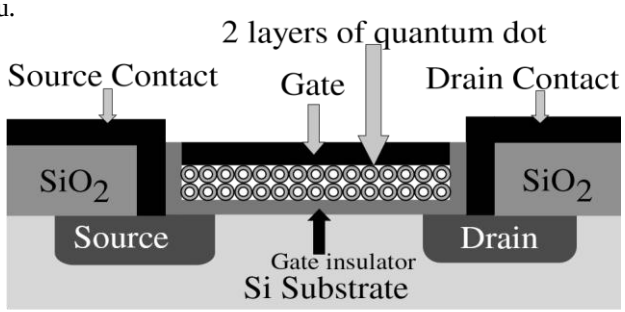
This paper is organized as follows. Section II describes the fabrication methodology of a QDGFET. Sections III describes circuit model. IV explains inverter operation. Section V explains proposed memory cell. Section VI gives conclusion and after that there are references which are used to do research for this topic.

II. FABRICATION METHODOLOGY

Structurally the QDGFET and the QDG nonvolatile memory are same. The basic differences are: i) absence of any control oxide layer separating the quantum dot layer and the gate electrode and ii) inclusion of two layers of cladded quantum dots in the gate region of the QDGFET. NVMs work even with one layer of quantum dots serving as a floating gate.

The detailed method of fabrication is discussed in different papers [17].

P-type silicon wafer is used to fabricate QDGFET. Phosphorous is diffused at 1000 °C for 5 minutes in the source and drain regions of the sample where 1200-Å oxide is used as a mask, Source and drain diffusion is followed by the growth of the gate oxide. In this process, first, the gate region is etched with buffered oxide etch, and 20-Å oxide is grown at 800 °C for 5 min in a dry oxidation furnace. Quantum dots are deposited on top of the gate oxide by a site-specific self-assembly method. In this method, SiOx-cladded -Si quantum dots are deposited on top of the gate insulator because of the pH of the quantum dot solution. Silicon dots of desired size can be obtained by repeatedly oxidizing and etching the dot solution. Silicon dot self-assembly is followed by the source/drain contact formation using gold–arsenic (AuAs). At last, gate contact is formed by evaporating aluminum on top of the sample and forming metal interconnect by patterning the Au.



(a)

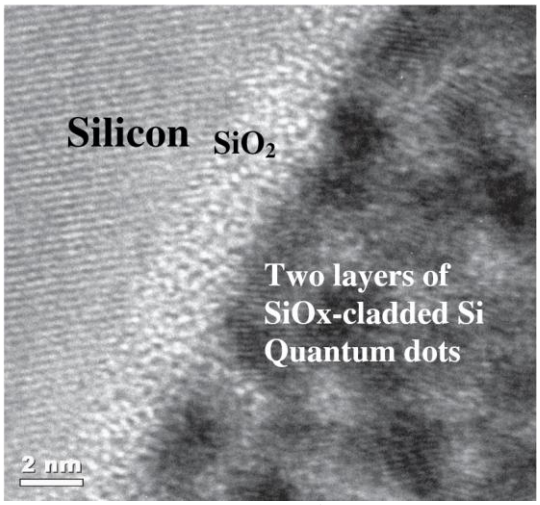


Figure 1. (a) Cross-sectional schematic of QDGFET. (b) High-resolution micrograph image (HRTEM) picture of a fabricated QDGFET

Fig. 1(a) shows the cross-sectional schematic of a QDGFET. Fig. 1(b) shows the HRTEM of a fabricated QDGFET which shows the presence of two layers of silicon oxide cladded -Si quantum dots on top of the gate insulator.

III. CIRCUIT MODEL

Initially, the effective threshold voltage is divided into three regions, OFF state, intermediate state and ON state, based on the fabricated device transfer characteristics. The threshold voltage of a QDGFET can be given according to (1).

As the gate voltage increases, initially the threshold voltage is same as a conventional FET which is represented by VT.

When the gate voltage increases through a range of voltages, Vg1 to Vg2, the threshold voltage changes linearly with respect to the gate voltage. This changes is controlled by the α parameter. With α= 0, the model behaves like a conventional FET and with α= 1 the model has a threshold voltage that changes directly with the gate voltage which represents QDG-FET characteristics. The parameter α depends on the size and number of dots which can be controlled at fabrication time, and as a result change the QD gate charge. The Vg1 and Vg2 terms are also determined at fabrication time. Using the equations for VTeff from Eq.(1), the drain current equations can be derived using traditional MOSFET circuit modeling techniques.

$$V_{T\,eff} = \begin{cases} V_T, & V_{GS} < V_{g1} \\ V_T + \alpha\left(V_{Gs} - V_{g1}\right), & V_{g1} < V_{GS} < V_{g2} \\ V_T + \alpha\left(V_{g2} - V_{g1}\right), & V_{GS} > V_{g2} \end{cases} \quad (1)$$

$$I_{DS} = \begin{cases} 0, & V_{GS} < V_{T\,eff} \\ \frac{W}{L} C_o \mu \left(V_{GS} - V_{T\,eff} - \frac{V_{DS}}{2}\right) V_{DS}, & V_{DS} < V_{GS} - V_{T\,eff} \\ \frac{W}{L} C_o \mu \frac{\left(V_{GS} - V_{T\,eff}\right)^2}{2}, & V_{DS} > V_{GS} - V_{T\,eff} \end{cases} \quad (2)$$

It should be noted that QD gate lowers the current when $V_{GS}>V_{g1}$. Moreover when α = 1, $V_{Teff} = V_T + V_{GS} - V_{g1}$, meaning that IDS = $(W/L)C_o\mu[V_{g1} - V_T - (V_{DS}/2)]$ Over the Vg1 to V_{g2} region. According to this equation I_{DS} is independent of V_{GS} over this region, leading to a flat current curve over the region. Using these principles, the Vth of conventional FET is modified according to (1) in Berkeley Simulation model (BSIM 3.2.0 and BSIM 3.2.4) which is very popular for nano-FET modeling and conducted simulations of QDGFET based ternary logic circuits using Cadence.

IV. THREE STATE COMPLEMENT FUNCTION

A three stare complement is an operation with one input (r)and three outputs (l0, l1,and l2) such that r is the number of states in the logic space [18]. The implementation of ternary inverters requires three inverters: negative ternary inverter (NTI), STI, and positive ternary inverter (PTI) where l_0, l_1,and l_2 should be the different outputs, respectively [19]. The truth table for these three inverters is shown in Table I.

$$l_0 = \begin{cases} 2, & if\ r - 0 \\ 0, & if\ r \neq 0 \end{cases}$$

$$l_1 = 2 - r$$

$$l_2 = \begin{cases} 2, & if\ r \neq 2 \\ 0, & if\ r = 2 \end{cases}$$

The circuit diagram of QDGFET STI is shown in Fig 2. This circuit is the same as a conventional CMOS inverter, except that the transistors have been replaced by QDGFETs. In this circuit, when the input is 0, the P-QDGFET is in the ON state and the N-QDGFET is in the OFF state, which makes the output 2. When the input is 2, the P-QDGFET is OFF and the NQDGFET is ON, which make the output 0. When Vin is equal to 1, both transistors are in the intermediate mode, thus making both of them behave like a resistor. In this situation, the circuit behaves like a voltage divider which produces an intermediate logic output assuming both transistors have equivalent βs. This intermediate logic output depends on different parameters of both QDGFETs and their size ratios. In other words, changing the size ratio will give different complement functions.

The circuit diagram for the NTI and the PTI is same as given in Fig. 4(a) where the QDGFETs are replaced by conventional pMOS and nMOS transistors with 22 nm feature size parameters. According to the Vth of pMOS and nMOS, the inverter can behave as a NTI or as a PTI. For NTI, the threshold voltage of the pMOS is −0.3 V and that of the nMOS is 0.11 V. When the input voltage is below 0.11 V, the nMOS is OFF and the output is 0.5 V. When the input voltage is above 0.11 V, nMOS is ON and the output is zero. For the PTI implementation, the threshold voltage of the nMOS and the pMOS should be 0.3 V and −0.2V, respectively.

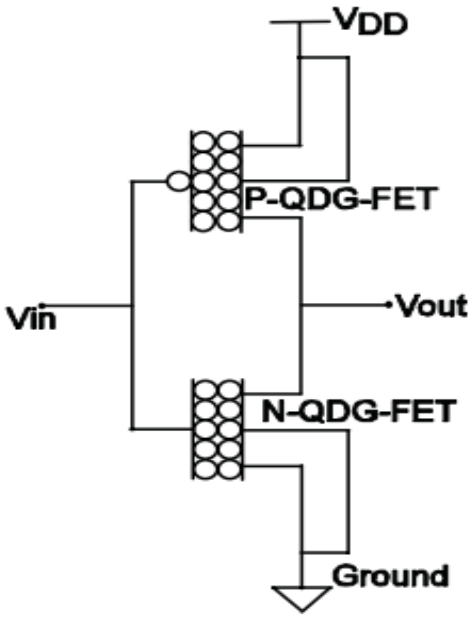


Figure 2: Circuit Diagram of STI

Input	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

Table 1: Truth table of STI, PTI and NTI

V. TERNARY MEMORY CELL

The schematic diagram of ternary memory cell is shown in fig 3.

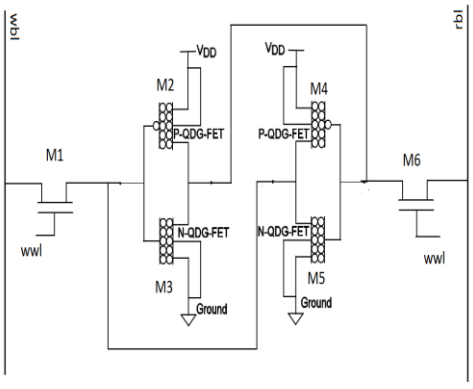


Figure 3: Circuit diagram of ternary memory cell

As shown in the fig 3, back to back connected two inverters form the memory cell. Four transistors M1, M2, M3 and M4 form the two back to back connected inverters. Transistors M1

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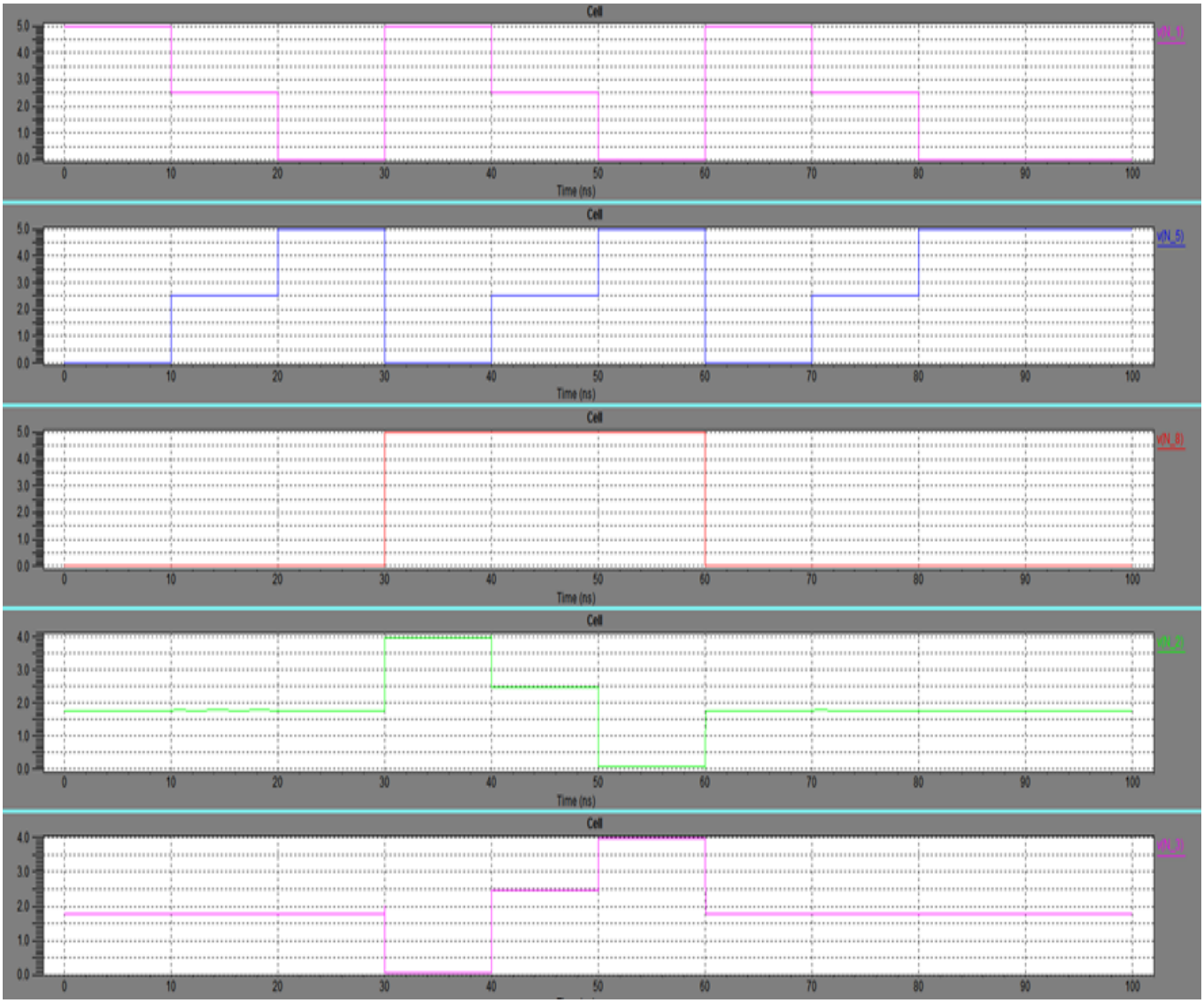

Figure 4: Output waveform of ternary memory cell.

and M6 form the wwl logic.

Output waveform of the circuit shown is shown in the fig 4.

In the waveform, first two lines waveforms are of wbl and rbl. The inputs wbl and rbl are inverse of each other. Third waveform is wwl logic. And Last two waveform is of first and second inverters.

As we can see in the output waveform, when ever the wwl line is enabeld, both the inverters are connected to wbl and rbl lines. And the value supplied in wbl and rbl lines is reflected in the output of the both the inverters. So from the output waveforms we can say that QDGFET works as a stable ternary memory cell eliment.

VI. CONCLUSION

From the properties and behaviour of QDGFET, it can be concluded that there are many advantages of using QDGFETs than other CMOS device because it require less no of circuit element than CNTFET and CMOS. Low power consumption was also observed in the QDGFET-based three-value logic circuits than the other. QDGFET allows MVL processing which gives one intermediate state between the two stable states. Apart from these advantages, the main advantage of QDGFET is that it can be used directly by replacing cmos with QDGFET in the existing circuit. No need to design the circuit from the scratch.

REFERENCES

[1] K. Kuhn, “Moor’s law past 32 nm: Future challenges in device scaling,” in Proc. 13th Int. Workshop Comput. Electron., 2009, pp. 1–6.

[2] S. Borkar, “Design perspectives on 22 nm CMOS and beyond,” in Proc. 46th IEEE Design Autom. Conf., Jul. 2009, pp. 93–94.

[3] H. Ru, W. HanMing, K. JinFeng, X. DeYuan, S. XueLong, A. Xia, T. Yu, W. RunSheng, Z. LiangLiang, Z. Xing, and W. YangYuan, “Challenges of 22 nm and beyond CMOS technology,” Sci. China Ser. F, Inf. Sci., vol. 52, no. 9, pp. 1491–1533, 2009.

[4] A. Raychowdhury, “Designing of low power and high-performance digital circuits with carbon nanotube transistors,”

Ph.D. thesis, Dept. Electr. Comput. Eng., Purdue Univ., West Lafayette, IN, 2007.

[5] H. C. Lin, "Resonant tunneling diodes for multi-valued digital applications," in Proc. 24th IEEE Int. Symp. Multiple-Valued Logic, May 1994, pp. 188–195.

[6] A. Forster, "Resonant tunneling diodes: The effect of structural properties on their performance," in Advances in Solid State Physics, vol. 33. New York: Springer-Verlag, 1994, pp. 37–62.

[7] A. C. Seabaugh, W. R. Frensley, J. N. Randall, M. A. Reed, D. L. Farrington, and R. J. Matyi, "Pseudomorphic bipolar quantum resonanttunneling transistor," IEEE Trans. Electron Devices, vol. 36, no. 10, pp. 2328–2334, Oct. 1989.

[8] F. Capasso and R. A. Kiehl, "Resonant tunneling transistor with quantum well base and high-energy injection: A new negative differential resistance device," J. Appl. Phys., vol. 58, no. 3, pp. 1366–1368, Aug.1985.

[9] A. A. Ketterson, J.-W. Seo, M. H. Tong, K. L. Nummila, J. J. Morikuni, K.-Y. Cheng, S.-M. Kang, and I. Adesida, "A MODFET-based optoelectronic integrated circuit receiver for optical interconnects," IEEE Trans. Electron Devices, vol. 40, no. 8, pp. 1406–1416, Aug. 1993.

[10] S. M. S. Imtiaz and S. M. El-Ghazaly, "Performance of MODFET and MESFET: A comparative study including equivalent circuits using combined electromagnetic and solid-state simulator," IEEE Trans. Microw. Theory Tech., vol. 46, no. 7, pp. 923–931, Jul. 1998.

[11] H. Rohdin, A. Nagy, V. Robbins, C.-Y. Su, A. S. Wakita, J. Seeger, T. Hwang, P. Chye, P. E. Gregory, S. R. Bahl, F. G. Kellert, L. G. Studebaker, D. C. D'Avanzo, and S. Johnsen, "0.1-μm gate-length AlInAs/GaInAs/GaAs MODFET MMIC process for applications in high-speed wireless communications," Hewlett-Packard J., no. 4, pp. 1–26, Feb. 1998.

[12] J.-H. Tsai, "High-performance AlInAs/GaInAs δ-doped HEMT with negative differential resistance switch for logic application," Solid-State Electron., vol. 48, no. 1, pp. 81–85, Jan. 2004.

[13] W. Kruppa and J. B. Boos, "Observation of DC and microwave negative differential resistance in InAlAs/InGaAS/InP HEMTs," Electron. Lett., vol. 28, no. 3, pp. 267–269, Jan. 1992.

[14] E. M. Chumbes, A. T. Schremer, J. A. Smart, Y. Wang, N. C. MacDonald, D. Hogue, James J. Komiak, S. J. Lichwalla, R. E. Leoni, and J. R. Shealy, "AlGaN/GaN high electron mobility transistors on Si(111) substrates," IEEE Trans. Electron Devices, vol. 48, no. 3, pp. 1–7, Mar. 2001

[15] F. C. Jain, E. Heller, S. Karmakar, and J. Chandy, "Device and circuit modeling using novel 3-state quantum dot gate FETs," in Proc. Int. Semicond. Device Res. Symp., Dec. 2007, pp. 1–2.

[16] J. A. Chandy and F. C. Jain, "Multiple valued logic using 3-state quantum dot gate FETs," in Proc. 38th Int. Symp. Multiple Valued Logic, 2008, pp. 186–190.

[17] E. Suarez, M. Gogna, F. Al-Amoody, S. Karmakar, J. Ayers, E. Heller, and F. Jain, "Nonvolatile memories using quantum dot (QD) floating gate assembled on II–VI tunnel insulator," J. Electron. Mater., vol. 39, no. 7, pp. 903–907, 2010.

[18] S. Lin, Y.-B. Kim, and F. Lombardi, "CNTFET-based design of ternary logic gates and arithmatic circuits," IEEE Trans. Nanotechnol., vol. 10, no. 2, pp. 217–225, Mar. 2001.

[19] W. Gang, C. Li, and L. Qin, "Ternary logic circuit design based on single electron transistors," J. Semicond., vol. 30, no. 2, pp. 025011–025015, Feb 2009.

[20] S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, and D. Buchanan, "Volatile and non-volatile memories in silicon with nano-crystal storage," in Proc. IEDM, Dec. 1995, pp. 521–525.

[21] S. Karmakar, J. A. Chandy, and F. C. Jain, "Design of ADCs and DACs using 25 nm quantum dot gate FETs," in Proc. Lester Eastman Conf. High Perform. Devices, Aug. 2010, pp. 1–8.

[22] S. Chuang and N. Holonyak, "Efficient quantum well to quantum dot tunneling: Analytical solutions," Appl. Phys. Lett., vol. 80, no. 7, pp. 1270–1272, 2002.

[23] A. Raychowdhury and K. Roy, "A novel multiple-valued logic design using ballistic carbon nanotube FETs," in Proc. 34th Int. Symp. MultipleValued Logic, May 2004, pp. 14–19.

[24] P. C. Balla and A. Antoniou, "Low power dissipation MOS ternary logic family," IEEE J. Solid-State Circuits, vol. 19, no. 5, pp. 739–749, Oct. 1984.

[25] T. Hanyu and M. Kameyama, "A 200 MHz pipelined multiplier using 1.5 V-supply multiple valued MOS current-mode circuits with dual-rail source-coupled logic," IEEE J. Solid-State Circuits, vol. 30, no. 11, pp. 1239–1245, Nov. 1995.

[26] S. C. Kleene, "On a notation for ordinal numbers," J. Symbolic Logic, vol. 3, no. 4, pp. 150–155, Dec. 1938.

[27] A. Raychowdhury and K. Roy, "Carbon-nanotube-based voltage-mode multiple-valued logic design," IEEE Trans. Nanotechnol., vol. 4, no. 2, pp. 168–179, Mar. 2005.

[28] A. P. Dhande and V. T. Ingole, "Design implementation of 2-bit ternary ALU slice," in Proc. 3rd Int. Conf. Sci. Electron. Technol. Inf. Telecommun., Mar. 2005, pp. 1–11.

[29] P. C. Balla and A. Antoniou, "Low power dissipation MOS ternary logic family," IEEE J. Solid-State Circuits, vol. 19, no. 5, pp. 739–49, Oct. 1984

[30] G. Eason, B. Noble, and I. N. Sneddon, "On certain integrals of Lipschitz-Hankel type involving products of Bessel functions," Phil. Trans. Roy. Soc. London, vol. A247, pp. 529–551, April 1955. *(references)*

[31] J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68–73.

[32] I. S. Jacobs and C. P. Bean, "Fine particles, thin films and exchange anisotropy," in Magnetism, vol. III, G. T. Rado and H. Suhl, Eds. New York: Academic, 1963, pp. 271–350.

[33] K. Elissa, "Title of paper if known," unpublished.

[34] R. Nicole, "Title of paper with only first word capitalized," J. Name Stand. Abbrev., in press.

[35] Y. Yorozu, M. Hirano, K. Oka, and Y. Tagawa, "Electron spectroscopy studies on magneto-optical media and plastic substrate interface," IEEE Transl. J. Magn. Japan, vol. 2, pp. 740–741, August 1987 [Digests 9th Annual Conf. Magnetics Japan, p. 301, 1982].

[36] M. Young, The Technical Writer's Handbook. Mill Valley, CA: University Science, 1989.

[37] Electronic Publication: Digital Object Identifiers (DOIs):

Article in a journal:

[38] D. Kornack and P. Rakic, "Cell Proliferation without Neurogenesis in Adult Primate Neocortex," Science, vol. 294, Dec. 2001, pp. 2127-2130, doi:10.1126/science.1065467.

Article in a conference proceedings:

[39] H. Goto, Y. Hasegawa, and M. Tanaka, "Efficient Scheduling Focusing on the Duality of MPL Representatives," Proc. IEEE Symp. Computational Intelligence in Scheduling (SCIS 07), IEEE Press, Dec. 2007, pp. 57-64, doi:10.1109/SCIS.2007.357670.