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Area Efficient, Low Power 4:1 Multiplexer using NMOS 45nm Technology

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Abstract: The field of electronics is trending with miniaturization and reduction in the threshold voltage. In this paper, we dealt with the efficient use of die area and optimum usage of power. This paper shows the contrast between "conventional MUX" and "MUX using NMOS transistors" and accentuates the advantages of the latter. The conventional 4:1 MUX consisted of a total of four AND gates and few inverters which made it occupy more die area but in this paper we have presented the design of 4:1 MUX which occupies less area on the die. Multiplexer is a device which works on the principle of MISO (Multiple Input Single Output).

Keywords: *MUX, PISO, SIPO, DeMUX*.

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[I] Introduction

In digital electronics we deal only with high and low or ON and OFF state of the current. As we know that actually nothing is digital and all the digital signals are obtained from their analog counterpart, so we talk of the digital world but not without the analog signals. The processes involved in doing the jump from analog to digital involves some continuous series of processes which includes first sampling then quantizing and then encoding of the digital signal. The manipulation of digital signals involves digital devices which include gates, decoders, registers, counters and multiplexers, etc. and in this paper we present the area efficient design of a 4:1 Multiplexer.

Multiplexers (also known as MUX) are the type of digital devices which have many inputs and only one output. The output is nothing but is only either of the inputs and the selection of the inputs is decided by the combination of the select lines. It works on Parallel Input Serial Output (PISO) principle. If we have an m-to-1 MUX, where $m=2^n$, then we would have to use 'n' select lines for selecting the 'm' inputs accordingly. Thus, different types of MUX can be made like 2:1, 4:1, 8:1, 16:1, 32:1 etc., by choosing the 'n' number of select lines.

[II] Multiplexers

As stated previously, a multiplexer, abbreviated as MUX, is a device that has multiple inputs and one output. The schematic of MUX is shown in figure 1.

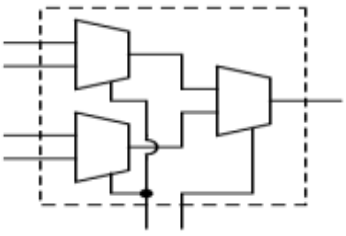

Fig. 1: Schematic symbol of 4:1 MUX

MUX is a device which is used for the transmission of multiple streams of digital data along one channel. These are fitted at the transmitter side. At the receiver side, we have de-multiplexers (De-MUX) which work just the opposite way as of MUX i.e. they have one input and multiple outputs. It works on the principle of Serial Input Parallel Output (SIPO). Multiplexers can also be expanded with the same naming conventions as de-multiplexers.

[III] Conventional design of 4:1 MUX using AND & NOT gates

A 4-to-1 MUX will consist of two select lines S_1 and S_2 whose combinations will decide which input is to be selected.As shown in table 1, the combination of S_1S_2 will decide which input is to be fed to the output.

Table 1: Truth table of 4:1 MUX

S_1	S_2	Output
0	0	Input 1
0	1	Input2
1	0	Input 3
1	1	Input 4

At the output, we have connected four LEDs which will glow when the output is high as shown in fig. 2.

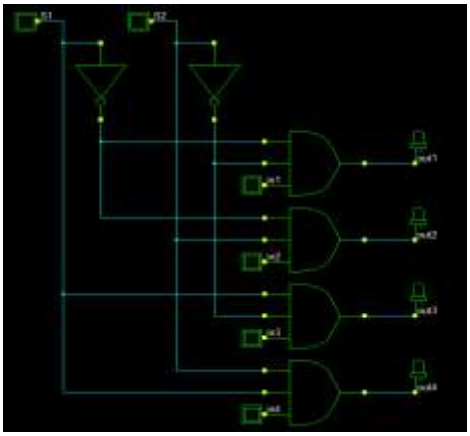

Fig. 2: 4:1 MUX using AND &NOT gates

In the circuit, we have taken four 3 input AND gates which are made of total of 8 NMOS and 8 PMOS

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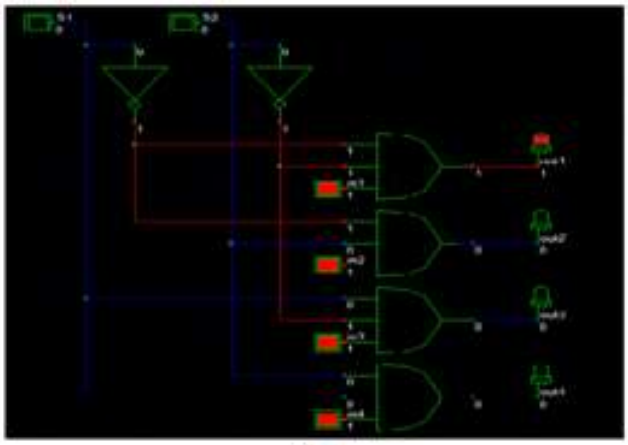
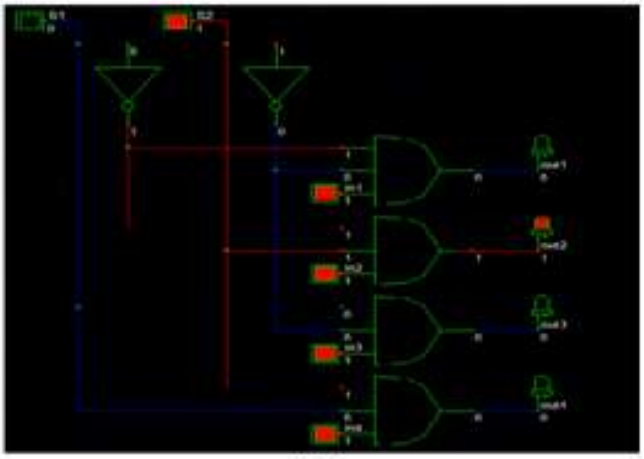
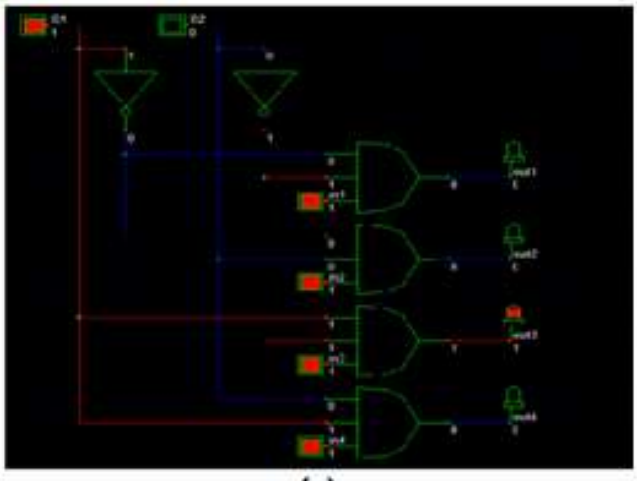
transistors and two inverters are made by a total of 2 PMOS and NMOS transistors. Thus, this whole circuit is made up of a total of 36 transistors which are huge! This lot number of transistors leads to high power dissipation and more die area.



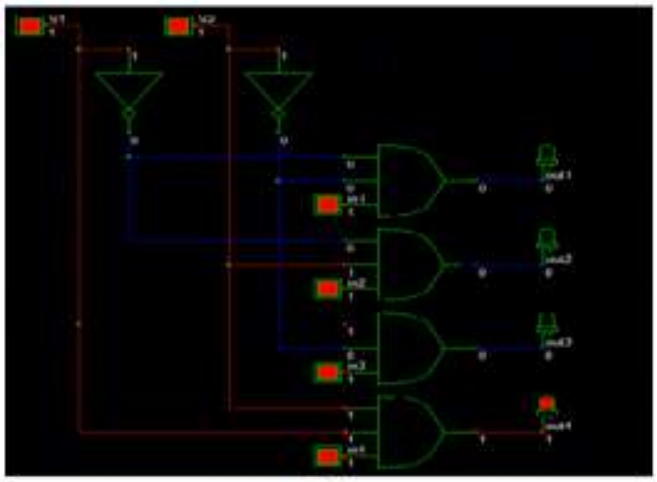
(a)



(b)



(c)



(d)

Fig. 3: Working diagram of 4:1 MUX

The working of the 4:1 MUX can be explained with the help of fig. 3 which shows how the input is selected the output when the select lines S_1 and S_2 are selected and how LEDs will glow accordingly.When both the select lines are zero that means S_1=S_2=0 then input 1 is selected at the output, as shown in fig.3 (a). Similarly, when S_1=0 and S_2=1 then input 2 is selected at the output, as shown in fig. 3 (b). Fig 3 (c) shows when select lines S_1=1 and S_2=0 then input3 is fed to the output of the multiplexer (4:1). Fig. 3 (d) shows when select lines S_1=1 and S_2=1 are selected then input 4 is selected at the output of the MUX. Thus, fig. 3 works according to the truth table 1.

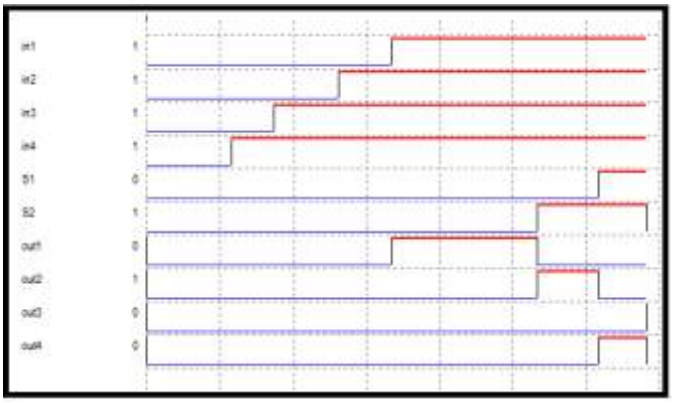


Fig. 4: Output waveform of 4:1 MUX

The output waveform of 4-to-1 MUX is shown in fig.4. In this diagram it can be seen that when S_1& S_2 are low (0) then output1 is high (1), this means that the input1 is selected at the output. Similarly, when S_1& S_2 are low and high respectively, output2 is high. Output3 is high when S_1 is high and S_2 is low and output 4 is high when S_1 and S_2 both are high.The fabrication layout of 4:1 MUX is shown in fig. 5.

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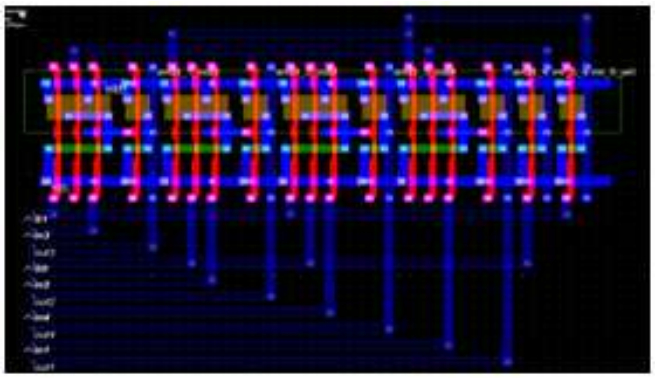

Fig. 5: Fabrication layout of 4:1 MUX

In today's miniaturization scenario, the main requirement is of lower power dissipation and less die area for the implementation of any circuit. So the circuit shown in figure 3 lags on these parameters. Hence, to overcome these problems, we present an area efficient design of a 4-to1 MUX in this paper using NMOS transistors only.

[IV] Proposed design of 4:1 MUX using NMOStransistor

The area efficient design of a 4-to-1 MUX is shown in fig. 6. In this design, 6 NMOS transistors are used and 1 LED to show the status of the output.

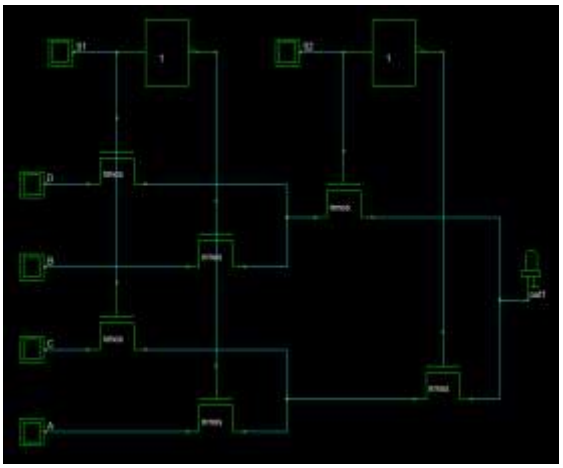

Fig. 6: 4:1 MUX using NMOS

In fig. 6, A, B, C and D are the four inputs to the MUX and S_1 and S_2 are the select lines. Table 2 shows how the input A, B, C and D are selected at the output.

Table 2: Truth table of 4:1 MUX (NMOS)

S_1	S_2	Output
0	0	Input A
0	1	Input B
1	0	Input C
1	1	Input D

The working diagram of 4:1 MUX using NMOS is shown in the fig. 7.

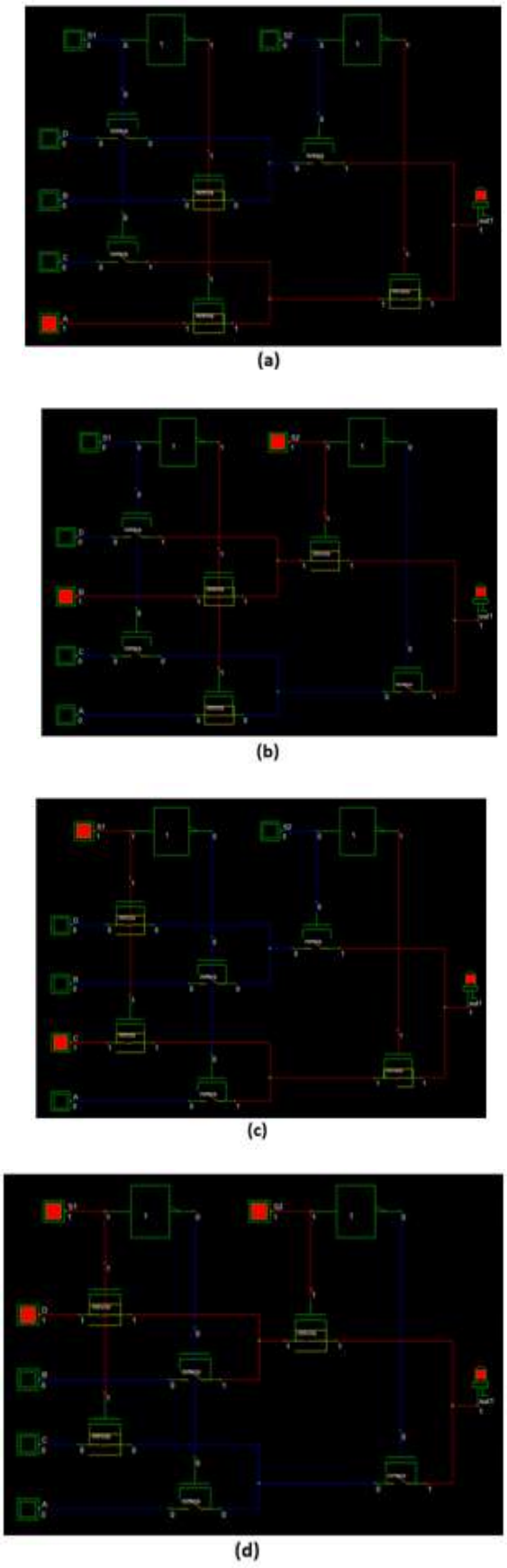

Fig. 7: Working diagram of 4:1 MUX using NMOS transistor

It is clear from fig. 7 that when the combination of S_1S_2 is 00 then input A is selected and for 01; input B is selected, for 10; input C is selected and for 11 input D is carried forward to the output of the MUX. Thus, verifying the truth table 2 of a 4:1 MUX.

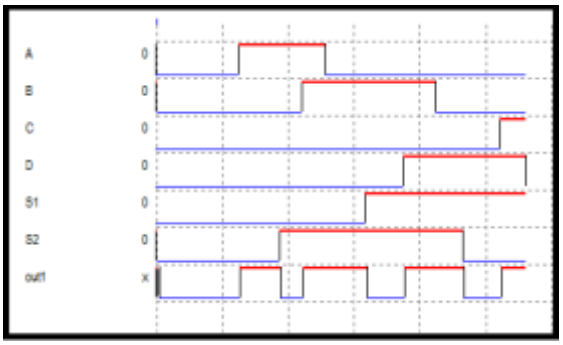

Fig. 8: Output waveform of 4:1 MUX using NMOS transistor

The output waveform of NMOS MUX is shown in the fig. 8 in which when S_1S_2 both are low (0) then input A is high (1); when input S_1 and S_2 are low and high respectively then input B is high; for input C to be high S_1 is high and S_2 is low. Similarly, when S_1S_2 both are high, input D is high. Thus the combination of S_1S_2 is solely responsible for the selection of inputs and then giving the corresponding output. The fabrication layout is shown in the fig. 9.

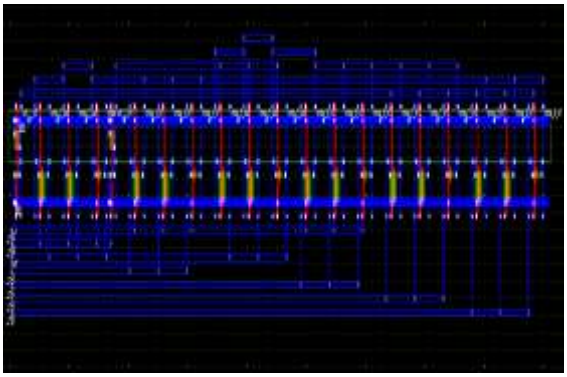

Fig.9: Fabrication layout of 4:1 MUX using NMOS transistor

From the diagrams, it is clear that the use of NMOS transistors for making 4-to-1 MUX helps to reduce the die area and the power dissipation in turn.

[V] Result analysis

From the above discussion, it was seen that the design of 4:1 MUX using NMOS transistors was much more area efficient than the conventional MUX made using logic gates (AND & NOT Gates). In the table 3 given below, it can also be seen that not only the area but other parameters like power consumption, speed of operation and number of transistors are also improved and in such way, the design of MUX shown in fig. 6 is more advantageous than the conventional MUX design.

Table 3: Comparison between conventional MUX and MUX using NMOS

Properties	Conventional MUX	NMOS MUX
Number of transistors	36 (NMOS+PMOS)	6 (NMOS)
Power consumption	75.596μW	75.65μW
Length	68.5μm	45.7μm
Breadth	9.4μm	8.2μm
Area	640.1μm^2	374.7μm^2

[VI] Conclusion

From table 3, it can be concluded that the percentage decrease in the area of the die is approximately 41% as compared to the fabrication of 4:1 MUX using logic gates, which is a huge achievement! This decrease in area will in turn result in the reduction of complexity and efficient usage of power. Thus the area efficient design of a 4:1 MUX using NMOS 45 nm technology is implemented.

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