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Design of Reconfigurable Network-on-Chip Topology

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Abstract **-** A Network-on-Chip (NoC) is used instead of buses to provide better interconnection between the IP modules, as the number of IPs in a SoC increases. The use of NoC enables the SoC designer to find suitable solution for different characteristics and constraints. The reconfigurable Network-on-Chip architecture aims at gaining low latency and low power consumption. As different applications have different requirements and the NoC should be flexible enough to meet these requirements. In this NoC architecture design we aim to combine both packet switching and circuit switching. By combining these two switching techniques it becomes possible to generate application specific topologies on a general Network-on-Chip based system.

Keywords **–** *Network-on-Chip; System-on-chip; Packet Switching; Circuit Switching.*

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I. INTRODUCTION

In the recent years there has been a dramatic change in the semiconductor technology and design techniques. This has led to the use of NoCs in place of buses, to provide better interconnection among the IPs. The bus-based interconnection prevents the system from meeting the proper requirements as the number of IPs used increases. For certain applications, the SoC is built around a highly efficient and dedicated network-on-chip that delivers very high performance for connecting a large number of components such as IPs and memory.

When a large number (tens to hundreds) of SoC systems are packed onto a single die, the bus is not feasible and may become a throughput bottleneck. To overcome the problems of a bus based system, the idea of network-on-chip (NoC) has been proposed in the recent years. This bottleneck can be easily overcome by the use of NoCs. The NoCs provide a better solution in terms of bandwidth, latency and power required. The processor, memory and intellectual property (IP) are connected to the router.

In NoCs, interconnects have a very important part in determining the overall system performance and can have a large impact on the total power consumption, wiring area and achievable system performance.

II. NETWORK-ON-CHIP ARCHITECTURE

The generalized Network-on-Chip architecture is shown in figure 1. The figure shows a number of IP cores are connected in mesh topology using Network Interfaces (NI), Router and Physical Links. By connecting the NI, router and physical link in different forms we can get different topology configurations- such as star, ring, fat binary tree, torus etc. each of these topologies have different advantages and can be used to serve different purpose. The topology is chosen according to the requirements of the application.

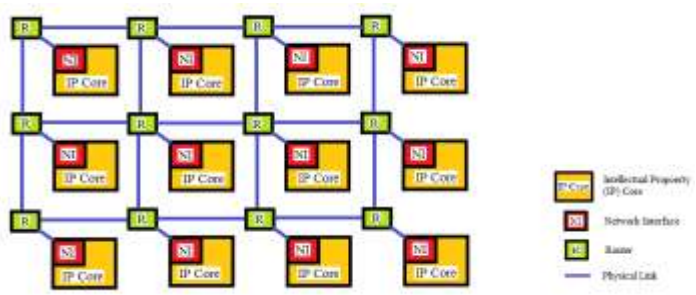

Fig. 1. Generalized NoC Architecture

The NoC uses data packets to transfer data between the IPs using routers and Interconnection links or wires.

The Intellectual Property (IP) Core is a reusable logic unit that can either be a processing element- such as CPUs or a storing element- such as RAM. The IP is the property of a third party designer and the implementation of IP is not a part of NoC design.

The Network Interfaces (NI) or Network Adapter (NA) is present between the IP core and the router. The main task of the NI is to convert the transaction requests into packets for injection into network. The NI encapsulates the IP data with necessary header information which is required by the router for further processing.

The main task of the router is to route the data packets from source to destination. The routing decision is made with the help of decoding the information in the header and the implemented routing algorithm.

The links form a critical part of NoC design. The two main types of connections usually required is between router-to-router and router-to-IP. There can be short length links between routers and IPs or global and semi-global links between routers and IPs.

A. *Reconfigurable NoC Architecture*

In the reconfigurable NoC architecture, the application running on the SoC determines the NoC configuration. The NoC architecture as viewed by the application is actually a logical topology built on the real physical topology.[1] Before this application starts the logical topology is configured according to the communication requirements in the initialization phase. The reconfiguration of topologies result in better parameters such as - area, power requirements and latency efficiency in contrast to traditional NoC topologies.

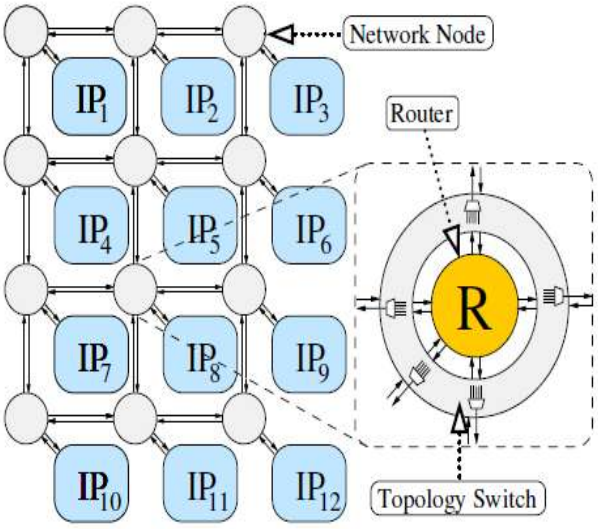

Fig. 2 Topology Switch which encapsulates the router present in the NoC.

The combination of both the switching techniques- physical circuit switching and packet switching makes it possible to create reconfigurable NoC, which are application specific on a general SoC platform.

III. NoC SWITCHING TECHNIQUES

The flow of data in the network is controlled in the router and is determined with the help of different switching techniques. The two main switching techniques are- circuit switching and packet switching.

A. *Circuit Switching:*

In this switching technique the path from the source to destination is reserved before the actual transmission of data begins. After the connection is made, the data bits contained in the instruction line can be transferred without any other information like- header, routing or arbiter.

The main advantage of using physical circuit switching is that no buffer, arbiter and router is needed as the link is dedicated. This switching technique leads to the full bandwidth utilization once the channel is set up, this result in low latency and guaranteed throughput. The limitation of using physical circuit switching is that it is not scalable as the links remain occupied for the entire duration of the data transfer. There is also a fixed latency as a certain amount of time is required to set up the path.

B. *Packet Switching:*

In contrast to circuit switching, no path is reserved in packet switching. Once the packets are transmitted from the source they make their own path independently to reach the destination. The role of buffering, arbitration and routing is important in packet switching technique. The links are not dedicated and can be shared easily.

Store and Forward Switching, Wormhole Switching, and Virtual Cut Through Switching are some of the commonly used switching techniques that are implemented to transfer data in packet switching methodology.

The main advantage of packet switching is that it is scalable. In this technique there is no fixed latency associated with it; the latency may vary from time to time. In comparison to packet switching circuit switching shows better latency and throughput performance.

IV. PROPOSED ARCHITECTURE

The three main components of the router are- FIFO Buffer, Round Robin Arbiter and the Topology Switch.

A. *FIFO Buffer:*

In each and every router the data packets are first received and stored in the input buffer. The input buffer is used to store data temporarily before it is actually transmitted to the destination IP core.

In many applications such as multimedia applications like video streaming buffer plays an important role to support busty data. A high buffer size may help to manage traffic, avoid collision and reduce the latency of the network.

The status of the buffer is indicated using ‘full’ and ‘empty’ signals. Buffer needs to be optimized in terms of area, and power consumption. Buffers may either be used at input port or at both input and output ports depending upon the application.

B. *Round Robin Arbitration:*

In a situation where a number of packets arrive at the input channel for same or different destination, the need of

an arbiter arises. The Arbitration protocol decides the sequence of access based upon the priority assigned.

An arbiter can have fixed-priority or variable-priority arbitration. The most commonly used arbitration mechanisms are - Round Robin, First Come First Serve, Priority Based, and Priority Based Round Robin. In the round robin arbiter, the request served in current cycle will get lowest priority in the next cycle.[15]

In round robin arbitration no starvation takes place, the unused time slots are freed immediately and re-allocated to be used by others.

C. Topology Switch:

The main task of the switch is to carry the data packets to its final destination. The switch transfers data for its input port to one or more output port. Fig 2 shows the topology switch.

The topology switch is inserted as a level between the network link and the router, this allows the links to be connected to a port on the router or directly to other links.

Topology switches are meant to be configured infrequently such as once every time the chip is powered up, or when a new application is started.[1]

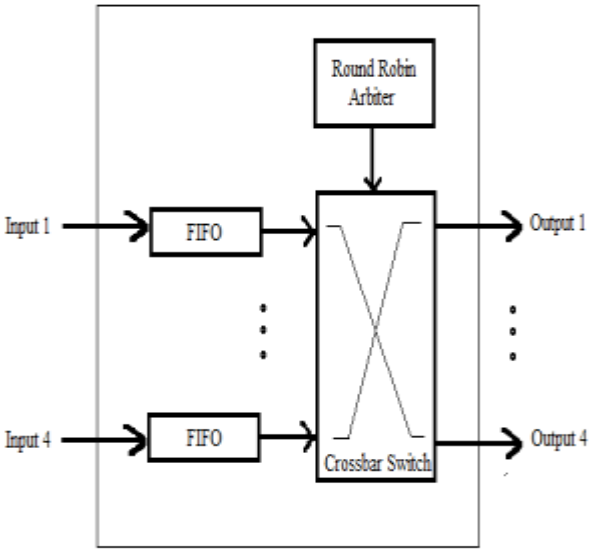

Fig. 3 Proposed NoC Architecture

V. SIMULATION RESULT

The router module is implemented using Xilinx ISE and for calculation of power Xilinx power estimator is used.

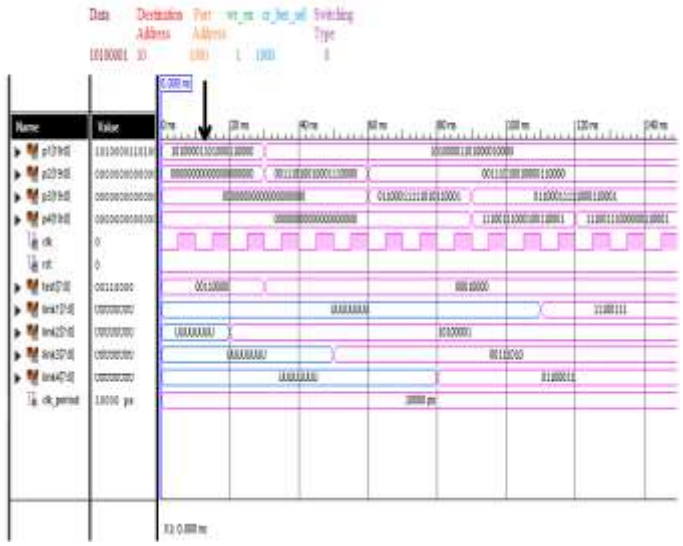

Fig. 4 Simulation Result of Reconfigurable NoC

As compared to traditional routers there is a significant improvement in latency and power. Fig. 5 shows the reconfigurable router's latency report and Fig.6 displays the total power requirements.

Fig.5 Latency Report

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.038	0.000	0.037
Vccaux	2.500	0.009	0.000	0.009
Vcco25	2.500	0.005	0.000	0.005

	Total	Dynamic	Quiescent
Supply Power (W)	0.081	0.000	0.080

Fig.6 Total Power Calculations

VI. CONCLUSION

In this paper, a unique Network-on-Chip architecture is proposed. The uniqueness of this architecture is that it combines two different switching techniques- packet switching and circuit switching. From the simulation result we can see that the data is being transferred to the destination address using both the switching techniques. The

results show that the router is optimized in power as well as latency.

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