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# Design and Development of Memristor Based Combinational Circuits.

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***Abstract*—** Now a days the memristor based devices are gaining a lot of attention because of its nano device range and its non-volatile memory. The objective of our research work is to design an efficient, low power Combinational Circuits using memristor and to compare the performance of the memristor based combinational circuits with CMOS based combinational circuits using EDA tools. In this paper we are focusing on the design of full adder, full subtractor, and encoders /decoders using hybrid-CMOS memristor structure. Combining CMOS and memristor gives the promising solutions for area reduction on a chip.

***Keywords*—** *Memristor, hybrid-CMOS memristor, Combinational circuits, EDA tool.*

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## I. INTRODUCTION

In the course of the most recent three decades, Moore's law has been the leading light for the transformative advancements that have driven the CMOS innovation towards 12nm components as we see it today. The wealth of exploration towards new devices, together with outline tenets and simulation environments have made the fundamental outline space for planners to embrace new innovations with additional certainty than what was conceivable previously. At the level of device, the unpredictability of further scaling the customary CMOS so as to keep pace with the Moore's expectation has experienced real difficulties. Until now the drawbacks of the conventional approach to design combinational circuits have been tolerated.

Some of the drawback of customary methodology can be succeed by using a forth fundamental circuit element proposed by L.O.Chua in 1971[1], which proves the relation between charge $q(t)$ and flux $\varphi(t)$. According to Chua Memristor provides the symmetry between resistor R ,capacitor C, and inductor L mathematically. In 2008 , Hewlett-Packard (HP) Labs illustrated Memristor that contains a thin film of titanium oxide($TiO_2$ )doped with oxygen ,sandwiched between two metallic wire of Platinum on both sides [2].

Memristor is a device having two terminals , and it is proficient in performing logic operations as well as memory operations. A major field of study is the logic operations performed by the memristor. There are various methodologies proposed for logic computation, one of them is Hybrid-CMOS logic. Both CMOS and memristor are used to design combinational circuits. There are many mathematical models available for the memristor , for the sake of simplicity we are using linear ion drift model. This paper is organized as follows: Section II Memristor characteristics and modelling, Section III basic logic gates using memristor , Section IV Combinational circuits using memristor Section V performance analysis Section VI conclusion.

## II. MEMRISTOR CHARACTERISTICS AND MODELLING

The memristors can be considered as the variable resistance which is known as the Memristance '*M*' of the device, '*M*' depends on the net current passing through that device. The equation for current controlled and time-invariant memristive device can be given as

$$v = R(w,i)i \tag{1}$$

$$\frac{dw}{dt} = f(w,i) \tag{2}$$

Where $w$ is the state variable of the device, $f$ and $R$ are the function of time , $v$ and $i$ are the voltage and current of the device respectively.

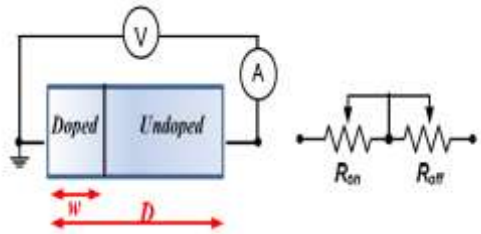


Figure 1 linear ion model of memrister. Two resistance Ron and Roff connected in series

The most familiar model of memristor is linear ion drift model, illustrated by HP labs in 2008 . Memristor having physical width of '*D*' is considered in linear ion drift model[3], the device have two regions doped region and undoped region as shown in Figure 1. The region having the width '$w$' is high doping concentration region.

It also behaves as a device state variable , here the oxygen vacancies are used as dopants i.e. $TiO_{2-x}$ . The other region having the width '$D$- $w$' is the undoped region and made up of $TiO_2$. The doped region is the low resistance region ($R_{on}$) whereas the undoped region is the high resistance

($R_{off}$) region. So the memristor can be modeled as two resistance connected in series as shown in fig 1.

The uniform field is assumed in linear ion drift model , also we assume that the ions are having the same average mobility equal to $\mu_v$. So (1) and (2) can be rewritten as

$$v(t) = \left(R_{on}\frac{w(t)}{D} + R_{off}\left(1 - \frac{w(t)}{D}\right)\right) i(t) \quad (3)$$

$$\frac{dw}{dt} = \mu_v \frac{R_{on}}{D} i(t) \quad (4)$$

Integrating (4) gives the following solution for state variable $w(t)$ as

$$w(t) = \mu_v \frac{R_{on}}{D} q(t) \quad (5)$$

As $R_{off} \gg R_{on}$ and putting the value from (5) to (3), the equation can be further reduced as

$$M(q) = R_{off}\left(1 - \mu_v \frac{R_{on}}{D^2} q(t)\right) \quad (6)$$

Here $M(q)$ can be represent as the memristance of the memristor. The linear ion drift model is bounded between the physical width of the memristor i.e. {0, $D$}. In order to keep the state variable $w(t)$ within the bounds a window function is applied. Here we are using the Prodomakis window function [4] which is proposed by Prodromakis et.al as follows

$$f(w) = j\left(1 - \left[\left(\frac{w}{D} - 0.5\right)^2 + 0.75\right]^p\right) \quad (7)$$

Where $j$ is the parameter of control which decides the maximum of $f(w)$. Figure 2 shows the characteristics of memristor using linear ion drift model and Prodromakis window function for frequency ($w_0$).

## III. BASICS LOGIC GATES USING MEMRISTOR

Memristor is passive component having two terminals, and it is proficient in being equipped as a combination of many digital circuits, storage element and logic [5]. A main property of memristor is , the data stored in memristor can be applied to another memristor to change the state.

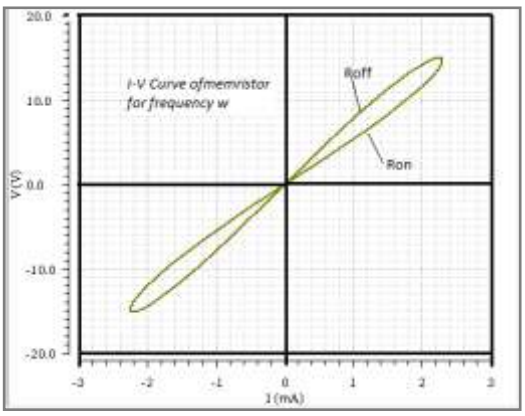


Figure 2. I-V Characteristics of memristor of frequency *wo* for linear ion drift model and Prodromakis window function.

The basic two input (*a* and *b*) logic gates AND and OR can be implemented using memristor as shown in Figure 3 and Figure 4 respectively. By using appropriate polarity next to input the AND and OR logic are generated. The only distinction between AND and OR is the reversed polarity. Figure 5 and Figure 6 shows the behavior of the AND and OR gate with respect to inputs ( *a* and *b*).

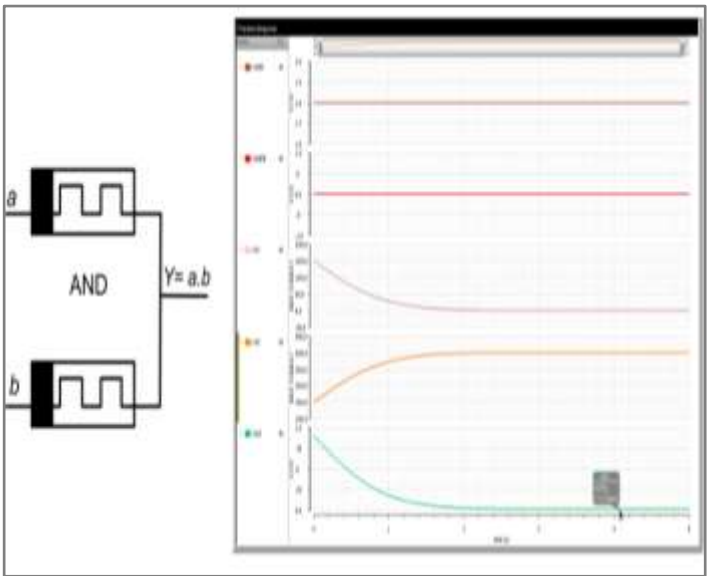


Figure 3. AND gate using memristor and nature of output (Y) for the given inputs ( *a = logic 1* and *b = logic 0*).

In case of AND gate a positive voltage *vdd* (high or logic '1') is applied to one input of the memristor and another input is connected to *gnd* (low or logic '0') , at the output terminal we get low voltage or logic'0'.

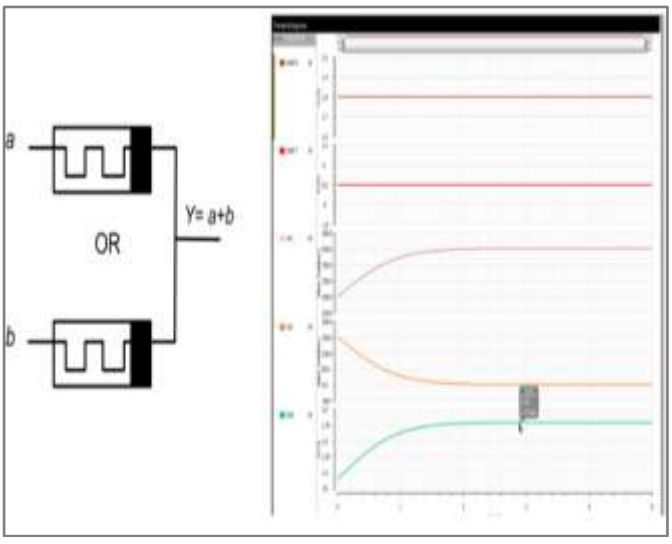


Figure 4. OR gate using memristor and nature of output (Y) for the given inputs( *a = logic 1* and *b = logic 0*).

Similarly for OR gate corresponding outputs can be observed. likewise NAND and NOR logics are implemented by applying a CMOS inverter at the output terminal of AND and OR gate.

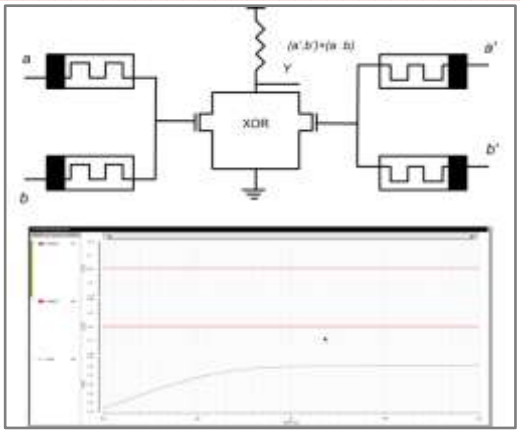


Figure 5. XOR gate using memristor and nature of output (Y) for the given inputs( *a = logic 0* and *b = logic 1*).

The same model can be used in realization of XOR gate as shown in Figure 5, here two NAND gates are used and a resistor is used to pull up the voltage level.

## IV. COMBINATIONAL CIRCUITS USING MEMRISTOR

### *A. Full adder and Full Subtractor.*

Adders are the basic blocks for any computations. .Figure 6 shows the realization of a Full adder using hybrid –CMOS memristor logic. Here two XOR gates are used to get summation of three bits ( *a* ,*b* and $c_{in}$ ) and for the carry out three AND and two OR gates are used.
Similarly full subtractor can also be implemented using memristor as shown in Figure 7.

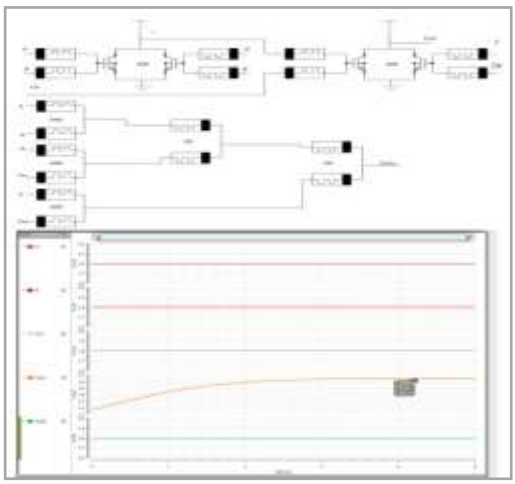

Figure 6. Full adder using memristor and nature of output (*sum=logic 1*,$c_{out=}$ *logic 1*) for the given inputs( *a = logic 1* and *b = logic 1* $c_{in=}$ *logic 1*).

### *B. Encoder*

Encoder is a frequently used many input combinational circuit, the output generated by encoder is encoded consistent with the input signal. Encoder having $2^n$ inputs and *n* output lines is a *n* –bit encoder. The output of encoder produces the binary value of input, which is set to logic '1' at that time instance. Every output by encoder illustrated by a logic function of given input signal, and those logic function can be implemented by memristor [6]. Figure 8 shows the methodology for implementing encoder and decoder using memristor.

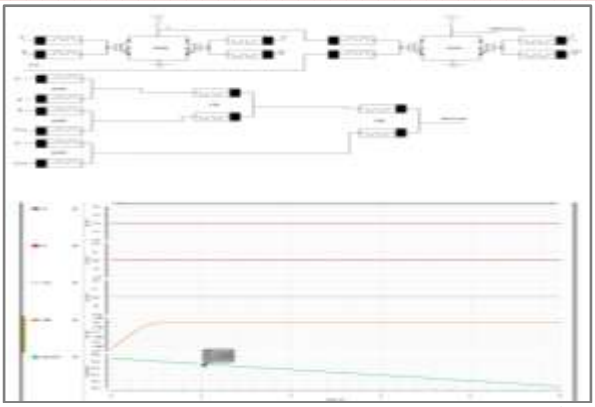

Figure 7 Full subtractor using memristor and nature of output (*difference=logic 1*,*borrow*$_{=}$ *logic 0*) for the given inputs( *a = logic 1* and *b = logic 0* $c_{in=}$ *logic 0*).

## V. PERFORMANCE ANALYSIS

Performance of the hybrid –CMOS memristor based combinational circuits can be analyzed by comparing them with CMOS based combinational circuits. Table 1. Shows the performance of the hybrid-CMOS memristor based circuits on the basis of power.

Generally in the case of CMOS, power consumption is more due to static leakage in the device. But the memristive device consumes less power in comparison to CMOS.

In the case of area utilization the memristive devices utilize more area for e.g. in case of Full adder the area utilization is 47%. Delay of memristive devices is comparatively less than that of CMOS devices.

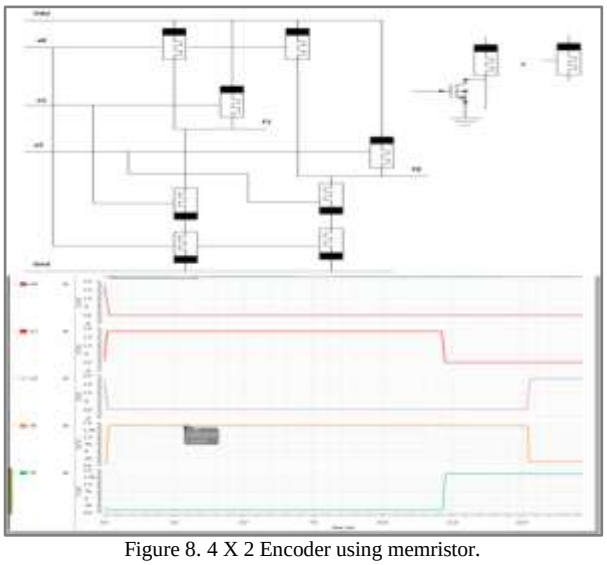

Figure 8. 4 X 2 Encoder using memristor.

## VI. CONCLUSION

In this paper we studied the methodology to design the memristor based combinational circuits. We have used the linear ion drift model for the designing of combinational circuits. Some other models are also available for modelling of memristor. As far as speed is concerned the memristive device provides less delay (*ps*) between input and output, that can be further reduced by using different models of memristor . Memristor provides lesser power consumption , different circuits can be used to reject power consumption. Area is the

prominent factor in case of memristor, which gives an excellent opportunity to realize various complex circuits using memristor.

Table 1. Shows the performance of the hybrid-CMOS memristor based on circuits power.

| Logic | Power($\mu W$) In Memristor | Power($\mu W$) In CMOS |
|---|---|---|
| XOR | 4.776 | 13.28 |
| Full Adder | 7.8 | 13.13 |
| Full Subtractor | 8.36 | 14.13 |

Table 1.

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