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Memristor Logic versus TTL Logic: A Comparative Design Analysis and Validation

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***Abstract*—**High speed, cost effective, low power, and high density non-volatile memory devices aids as driving force to carry out research in the field of solid state non-volatile memories. Memristor (Memory-Resistor) is a new category of non-CMOS non-volatile memory whose functional operation is manifested itself as the movement of ionic defects in the lattice of a crystalline material. As the name "Memory Resistor" implies that it is a non-volatile random access memory (NVRAM) i.e. it does not lose its data even when the power is switched-off. In this paper, a new model called Voltage Threshold Adaptive Memristor (VTEAM) model is presented in the context of analysing the logic gates made of Memristors .This paper focuses on the parametric variation of the VTEAM model and also on the implementation of the basic logic gates using Memristors as the basic component. On the basis of simulation results, it is observed that the device shows better accuracy and also faster read operation compared to TTL counterpart. As a case study, NAND and XOR gates are implemented and tested.

Keywords*-Memristor,Non-volatile memory, voltage-controlled, Logic gates*

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I. INTRODUCTION

Three basic circuit elements such as resistors, capacitors and inductors are currently used for design of electronic circuits. Having a magnificent accomplishment, in 1971, Leon Chua, originally postulated the existence of a fourth fundamental element which he named as memristor [1] but it remained as a theoretical concept. But in 2008, an exact fabricated device exhibiting pinched hysteresis characteristics was demonstrated by HP lab. Memristor has a combination of both memory and resistor behaviour. Memristor is a two terminal element which shows the relation between flux and charge. Memristor remembers its recent resistance value when the device is turned off and until the next time, the device is turned on. The memristor finds its application in oscillators, logic gates [2]-[5] and Neuromorphic system [6]-[9].All the six relation of fundamental passive elements are depicted in Fig. 1 in the context of voltage(v) , current(i) , charge(q) &flux(ø).

II. MEMRISTOR-AS A MEMORY ELEMENT

It is basically a two terminal passive device, nonlinear and a variable resistor. It is attractive due to its non-volatility nature i.e. it remembers its state when power supply is removed. The first Memristive device was made in HP labs by Stanley Williams in the year 2008 [10]. They fabricated the titanium dioxide based memristor by sandwiching the thin film TiO2 between two platinum electrodes. In Fig. 2 the model of the titanium dioxide based memristor is shown.

The length of the active region is defined as D and w is the internal variable width which changes with respect to applied voltage. The whole resistance of the device is recognized by the two variable resistors connected in series, where the resistances are assumed for the complete length of the device. It consists of two layers as non-stoichiometric (i.e. oxygen vacancy are present) and stoichiometric layer.

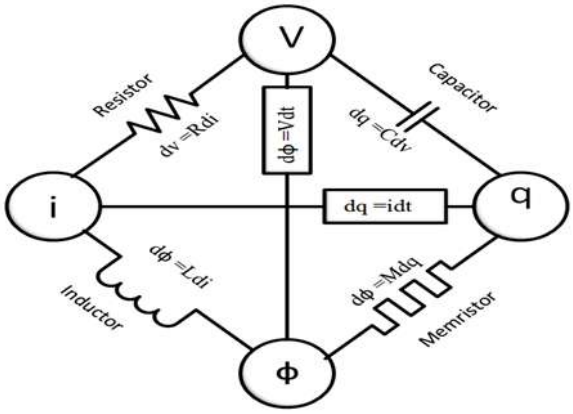

Figure 1. Relation between four passive elements

When a sinusoidal voltage is applied across the positive terminal of the memristor it is found that the width of the doped region increases resulting in lowering the effective resistance of the device called low resistance state (LRS, RON).Similarly when the polarity reverses it decreases the length of the doped region thereby increasing the net resistance called as high resistance state (HRS, ROFF). Fig. 3 shows that the Memristor is a frequency dependent device and as the frequency increases the current through the memristor decreases which imply that less amount of charge stored when the frequency is high, thus giving rise to low current.

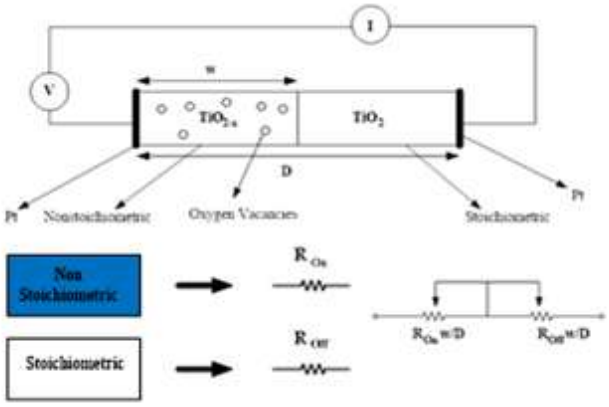

Figure 2. The basic model of memristor

A charge-controlled memristor is given by:

$$v(t) = M\big(q(t)\big).i(t) \quad (1)$$

$$M\big(q(t)\big) = \frac{d\Phi/dt}{dq/dt} = \frac{V(t)}{I(t)} \quad (2)$$

Where, M (q (t)) is the Memristance of the memristor which has the same units of resistance. Its resistance value depends on the magnitude and the polarity of the applied voltage.

A current-controlled time-invariant Memristive device is represented by:

$$v(t) = R(w).i(t) \quad (3)$$

$$\frac{dw}{dt} = f(w,i) \quad (4)$$

R (w) is the instantaneous resistance that is dependent on the internal state variable '*w*' of the device. If a voltage is applied across the memristor, then the voltage drop across the variable resistor is

$$v(t) = \left(R_{on}\frac{w(t)}{D} + R_{off}\left(1 - \frac{w(t)}{D}\right)\right) i(t) \quad (5)$$

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{on}}{D} i(t) \quad (6)$$

Where μ_v is the mobility of oxygen vacancies and D is the length of active region of the memristor, which yields the following expression for w (t):

$$w(t) = \mu_v \frac{R_{ON}}{D} q(t) \quad (7)$$

Substituting equation (6) in equation (4) we obtain the Memristance as

$$M(q) = R_{OFF}\left(1 - \frac{\mu_v}{D^2} q(t)\right) \quad (8)$$

III. Voltage Threshold Adaptive Memristor(VTEAM)

Previously, many memristor models [11]-[13] have been proposed. After several experiments, it was inferred that threshold voltage is shown to be existed rather than threshold current for designing physical memristor. The TEAM model is basically based on current threshold [14], so the resistance of the device does not change below certain limit of current.

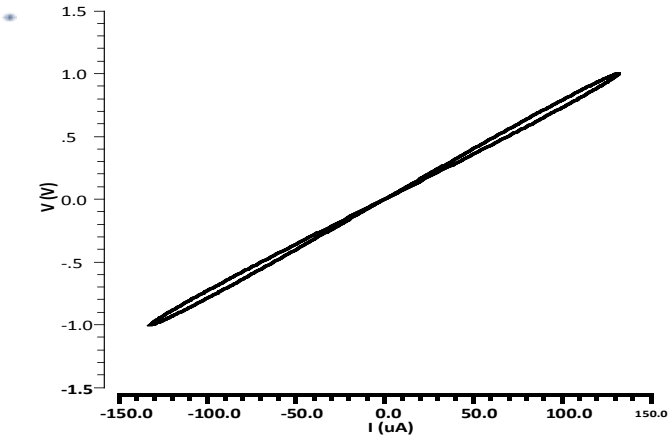

Figure 3. I-V characteristics of a Memristor
[Linear ion drift model]

The VTEAM model is nothing but the extension of previously proposed TEAM model (i.e. designer friendly, simple) with the threshold voltage. This model assumes asymmetric and nonlinear switching behavior. The VTEAM model is computationally efficient and accurate in comparison to the existing device model [15].

A voltage-controlled time-invariant Memristive device [16] is presented as:

$$\frac{dw}{dt} = f(w,v) \quad (9)$$

$$i(t) = G(w,v).v(t) \quad (10)$$

Where, $G(w,v)$ is the device conductance. The above expressions show the presence of a threshold voltage. The internal state variable derivative of VTEAM is mathematically presented as:

$$\frac{dw(t)}{dt} = \begin{cases} k_{off}\cdot\left(\frac{v(t)}{v_{off}} - 1\right)^{a_{off}} \cdot f_{off}(w), 0 < v_{off} < v \\ 0 \qquad\qquad\qquad\qquad\qquad , v_{on} < v < v_{off} \\ k_{on}\cdot\left(\frac{v(t)}{v_{on}} - 1\right)^{a_{on}} \cdot f_{on}(w), v < v_{on} < 0 \end{cases} \tag{11}$$

Where k_{off} , k_{on} , a_{off} a_{on} are constants, and parameters v_{on} and v_{off} are threshold voltage $f_{off}(w)$ and $f_{on}(w)$ are the window function [15].

The I-V relation is expressed as:

$$i(t) = \left[R_{on} + \frac{R_{off} - R_{on}}{w_{off} - w_{on}}.(w - w_{on})\right]^{-1}.v(t) \tag{12}$$

Where w_{on} and w_{off} describes the bounds of internal state variable, w [15].In Table-I, a comparison is depicted between previously proposed Memristive models and VTEAM model

Table I. Comparison of previous model and VTEAM

MODEL	LINEAR ION DRIFT MODEL [10]	NON- LINEAR DRIFT MODEL [17]	SIMON TUNNELING BARRIER [18]	TEAM [14]	VTEAM [15]
State variable	$0 \le w \le D$ Doped width	$0 \le w \le 1$ Doped width	$x_{on} \le x \le x_{off}$ Undoped width	$x_{on} \le x \le x_{off}$ Undoped width	$w_{on} \le w \le w_{off}$ Doped width
Controlled mechanism	Current-controlled	Voltage-controlled	Current-controlled	Current-controlled	Voltage-controlled
Symmetricity	Yes	Yes	Yes	No	No
Accuracy for practical Memristive device	Lowest	Low	High	Sufficient	Highest
Threshold	No	No	No	Yes(threshold current)	Yes (threshold voltage)

In VTEAM, below a particular threshold voltage, the resistance of the memristor will not be altered. For logic operation and memory application, threshold voltage of a memristor is more accurate that of threshold current in comparison to TEAM model.

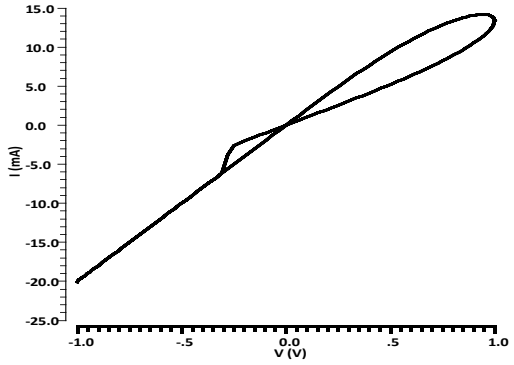

Figure 4. The VTEAM model driven for Von=-0.2V and Voff=0.02V

Variation in threshold voltages, i.e. v_{on} and v_{off}, determines how fast the reading mechanism occurs .Two Frequency dependency curve for no window function is taken into account as depicted in Fig. 4 and Fig. 5 for different threshold voltages. Observing both the figures, the threshold voltages values taken for Fig. 4 have faster reading mechanism than Fig. 5. In comparison to the previously existing models the hysteresis plot shows that the response is asymmetric in nature and it has a fast switching as the reading operation is performed faster.

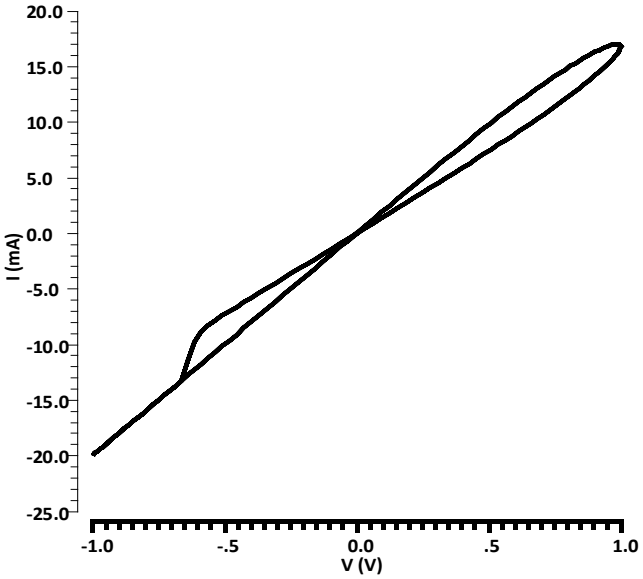

Figure 5. The VTEAM model driven for Von=-0.5V and Voff=0.05V

IV. VTEAM BASED LOGIC DESIGN

To obtain logic'1'or logic'0', the resistance of the memristor should be known. High resistance of the device indicates logic'0' whereas Low resistance indicates logic'1'. NAND and XOR gate is described using VTEAM model having no window function.

A. NAND gate:

The schematic of Memristor based NAND gate is shown in Fig. 6. When a positive voltage is applied to positive terminal,i.e., p-side of the Memristor, there is a shift in state variable from 0 to D which results in increase in resistance of the memristor which implies logic '0' is obtained. As it is a NAND gate a CMOS inverter is connected to the output for performing inversion operation, so we get logic '1'. The truth table is shown in Table-II.

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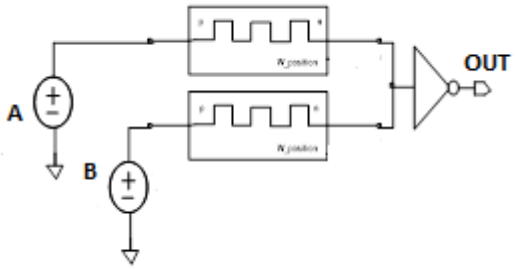

Figure 6. Schematic diagram of NAND Gate using Memristor

Table II. Truth table of NAND gate.

A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 7 shows that as we applied positive voltage to the memristor M1 and a negative voltage to M2 ,the resistance across M1 increases as the width of the undoped region decreases and the resistance across the memristor M2 decreases, due to which logic'0'is obtained at the common node and because of inverter we get output as logic '1'.

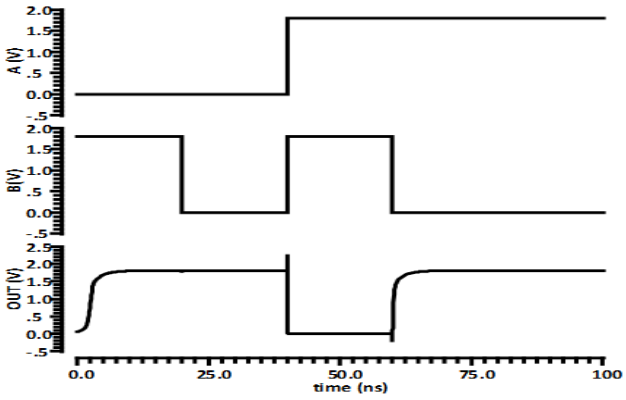

Figure 7. Output waveform of NAND Gate

B. OR GATE:

The schematic of memristor based X-OR gate is shown in Fig.8. In this two 2-input NAND gate based memristor is used. If A='1'and B='0', NMOS gets off and output Z='1', hence satisfying the Boolean function $Z = A \oplus B$.

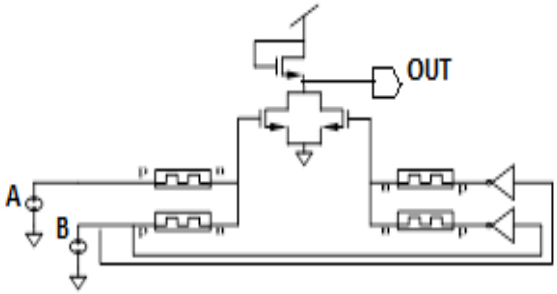

Figure 8. Schematic diagram of XOR Gate

The Fig. 8 shows that the basic expression of XOR gate i.e. $A \oplus B = (AB + A'B')'$, where the OR implementation is replaced by NMOS driven by a simple resistor instead of PMOS device. The truth table is shown in Table-III.

Table III. Truth table of EX-OR-gate.

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

Fig. 9 shows that as a case study, we applied positive voltage to the Memristor M1and a negative voltage to M2, the resistance across M1 increases as the width of the undoped region decreases and the resistance across the Memristor M2

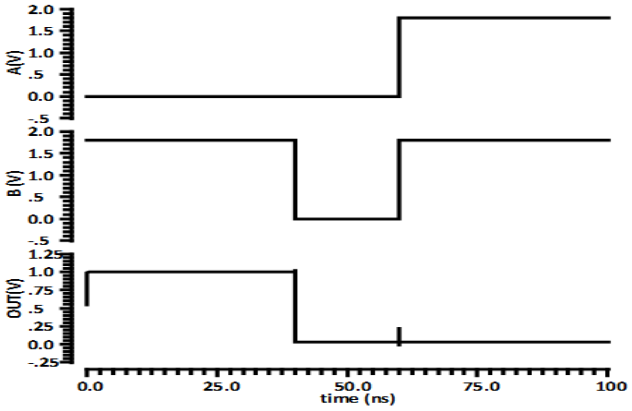

Figure 9. Output waveform of XOR Gate

decreases, due to which logic'0' is obtained at the common node and this is fed to the base of NMOS, so NMOS gets off. So all the supply voltage with some drop due to the resistor appeared at the output node. So we get output as logic '1'.

V. RESULTS AND DISCUSSION

Based on the above results it is found that memristor based design occupied less die area in comparison to CMOS based design. In Table III., a comparison study has been done to

show the number of Memristors and transistors required for the construction of NAND and XOR logic design

TABLE III. COMPARISON OF TRANSISTOR BASED AND HYBRID MEMRISTOR BASED DESIGN

Design	Transistor based design (Number of Transistors(T))	Hybrid Memristor based design (Number of Memristors(M) and Transistors(T))
NAND gate	4T	2M+2T
XOR gate	8T	4M+3T

VI. CONCLUSION

The memristor with voltage threshold based on Verilog-A is modeled. Parametric analysis, hysteresis plot and logical operations have been conducted using Cadence Virtuoso tool, to show the effectiveness of VTEAM model. Based on present study, it is found that the reading operation can be performed faster than the writing operation comparison to the existing models. The Memristive model is successfully implemented for logic gates as the case study. It is found that the logic gates uses comparatively less die area than that of CMOS technology.

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