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Implementation of Low Power Multiplexer usign Adiabatic Logic

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***Abstract*—** Adiabatic logic is a low power logic based on charge recovery principle. In this paper, an adiabatic logic based 2x1 multiplexer and 4x1 multiplexer are designed on the basis of Two-Phase Adiabatic Static Clocked Logic (2PASCL) technique. The power dissipation of proposed technique is compared with conventional CMOS technique according to the various values of input signal switching frequencies, number of active devices and total nodes. The simulation is performed on S-edit of TANNER tools with BSIM4 at 90nm technology.

Keywords- *Adiabatic Technique, Charge recovery logic, Oscillating power clock, 2PASCL logic, T-Spice.*

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I. INTRODUCTION

Increasing demand of portable systems and the complexity of this portable system gradually increases due to increasing the functionality which is more responsible for energy dissipation in VLSI technology. In conventional CMOS circuit there are different techniques used to reduce the power dissipation like reducing supply voltage, output load capacitance, and input signal transition frequency. But in adiabatic technique not used constant supply voltage instead of an oscillating power supply are used that are also called power clock. Each power clock consists of four intervals: In pre-¬charge phase the output load capacitor is charged according to adiabatic logic, whereas in hold state output are kept in hold state for providing necessary computation, In recovery phase the charge from output load capacitor are transferred to the oscillating power supply and last wait state is provided then after again pre-charge state are begin. In adiabatic technique the input signal switching frequency are reduced for reducing the switching activity of devices, because the low power dissipation is also a design parameters compare to other design parameter like performance and area [1].

Figure 1. Four phase of Power clock [2].

II. ADIABATIC CHARGING PROCESS

Charging process of adiabatic logic consist of capacitor C in series with a resistance R and using a constant current supply to charge the load capacitor. At the beginning the voltage beyond the capacitor is zero. Where R is a resistance of pMOS devices in the pull up network and Vc is voltage across capacitor at the initially.

The charge beyond the capacitor at time T is given by

$$Q = CVc\ (t) \quad (1)$$

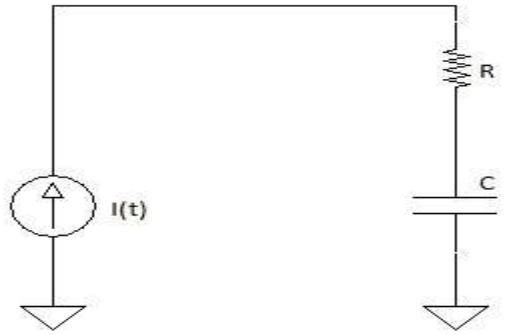

Figure 2. Adiabatic charging of a capacitor

Suppose that if current is constant during the time period 0 to T hence the energy dissipation is given by the expression[3]:

$$E_{dissipation} = R\ I^2\ (t)dt \quad (2)$$
$$= R\ I^2\ (t)\ T \quad (3)$$

And also we know that constant current is given by

$$I\ (t) = Q/T \quad (4)$$
$$I\ (t) = CV/T \quad (5)$$

Put the value of equation (5) into equation (3) then

$$E_{dissipation} = R\ (CV/T)^2\ T \quad (6)$$
$$E_{dissipation} = (RC/T)\ C\ V^2 \quad (7)$$

Where Edissipation is the total energy consumed during charging period. If charging time T is greater than the charging time constant RC, Then power dissipation can be reduced very large amount compare to CMOS logic.

III. CMOS INVERTER

In CMOS inverter the drain of pMOS and nMOS are connected to the output and gate of both devices are connect to the input. A supply voltage is \attached at the source terminal

of pMOS, and a ground attaches at the nMOS source terminal. When the input is low then pMOS is on and nMOS stay off. Hence charging path exists between power supply and output load capacitance, this is called charging stage of CMOS inverter. The basic CMOS inverter is shown in figure 3.

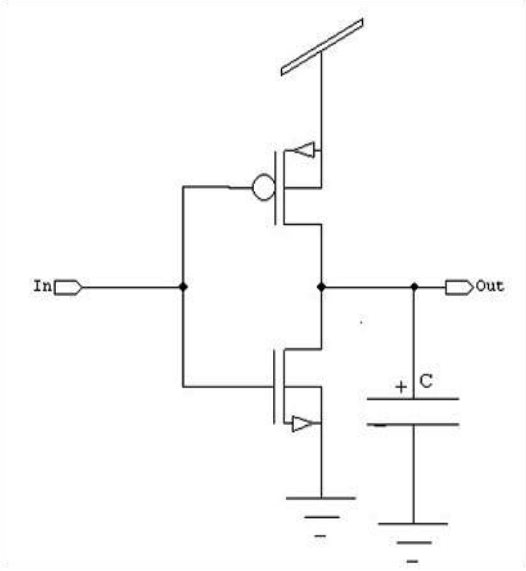

Figure 3. CMOS Inverter

$$E_{charge} = 1/2CLV_{dd}^2 \quad (8)$$

When the input is high then nMOS is on and pMOS stay off. Hence there is no direct path exist between supply voltage and output load capacitance. This is called discharging stage, and charge are discharged from output load capacitance to ground that cannot be recovered.

$$E_{discharge}=1/2CLV_{dd}^2 \quad (9)$$

Total amount of energy dissipation during charging and discharging stage is given by

$$E=CLV_{dd}^2 \quad (10)$$

IV. 2PASCL INVERTER

2PASCL inverter consists of two sinusoidal power supplies that are called power clock. Where one clock is in phase while the other is inverted, this both power clock replaces the constant power supply and ground in the conventional CMOS circuits. The operation of 2PASCL inverter can be described as: when input voltage is low than pMOS transistor which connect to the input is ON and nMOS transistor are OFF, Which charge the output capacitor according to the magnitude of power clock. Whereas when input voltage is high then nMOS transistor is ON and pMOS transistor which connect to input are OFF, by using this two diodes the charge from output load capacitor can be recycled instead of dissipated energy to ground. Here the operation "evaluation" and "hold" can be performed sequentially. The 2PASCL inverter is shown in figure 4.

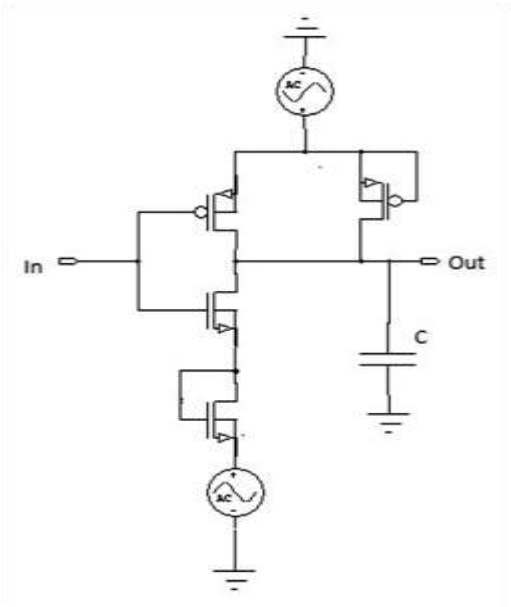

Figure 4. 2PASCL Inverter

V. MULTIPLEXER

A Multiplexer also known as a data selector is combinational logic circuits that accepts several data inputs and allows only one of them transmits to the output at a time. Routing of desired data input is controlled by select line. The relationship between input output and select line is given by n = 2^m. where m and n is equal to number of select inputs and number of data input respectively. In multiplexer the number of data outputs is always equal to one. Multiplexer are used in various applications like data routing, parallel to serial converter, a seven segment multiplexer, and a logic function generator.

A. Basics of 2X1 Multiplexer

In 2x1 multiplexer the number of data inputs and select line is two and one respectively. When select line S is equal to zero then input data I0 is routed to the output, and when select line S is high then I1 is transferred to the output. The output expression for a 2x1 multiplexer is given by

$$Y = \bar{S}I0 + SI1 \quad (11)$$

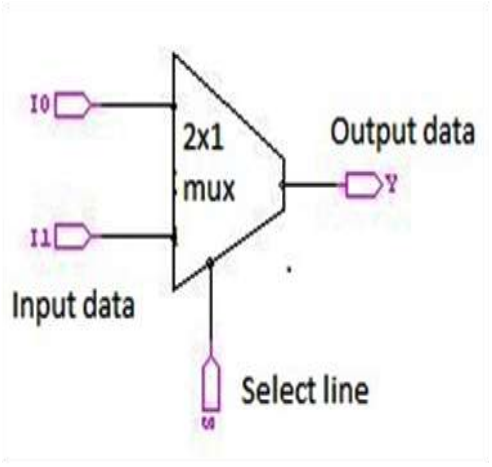

Figure 5. Function diagram

TABLE I. FUNCTIONAL TABLE OF 2X1 MULTIPLEXER

Select line	Data output
S_0	I_0
S_1	I_1

2x1 multiplexer design using CMOS and 2PASCL adiabatic logic as shown in figure 6 and figure 7 vice- versa.

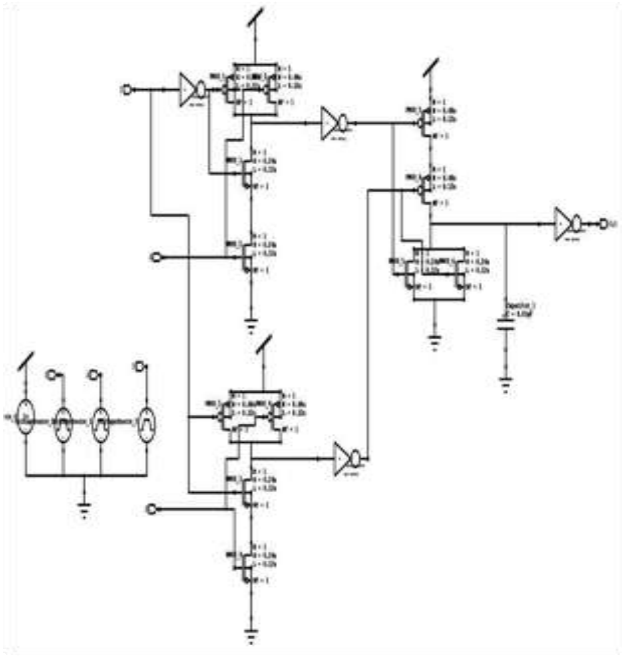

Figure 6. Schematic of 2x1 multiplexer using CMOS

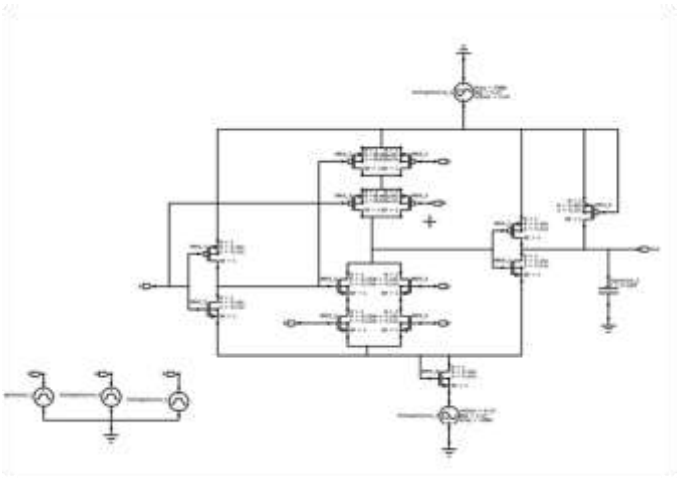

Figure 7. Schematic of 2x1 multiplexer using 2PASCL adiabatic logic

B. Basics of 4X1 Multiplexer

In 4x1 multiplexer I0, I1, I2, I3 are four data inputs and S1, S0 are two select lines. For the appropriate combination of both select lines the input data are transferred to the output. The output expression of 4x1 multiplexer is given by

$$Y = \bar{S}1\bar{S}0I0 + \bar{S}1S0I1 + S1\bar{S}0I2 + S1S0I3 \quad (12)$$

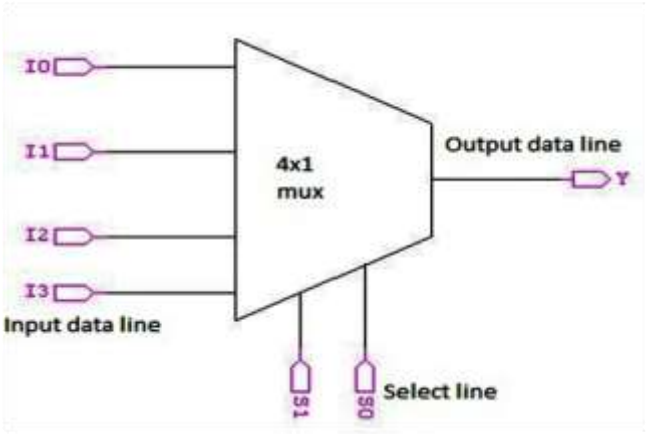

Figure 8. Function diagram

TABLE II. Functional Table of 4x1 Multiplexer

Select lines		Output data line
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Similarly 4x1 multiplexer design using CMOS and 2PASCL adiabatic logic as shown in figure 9 and figure 10 vice- versa.

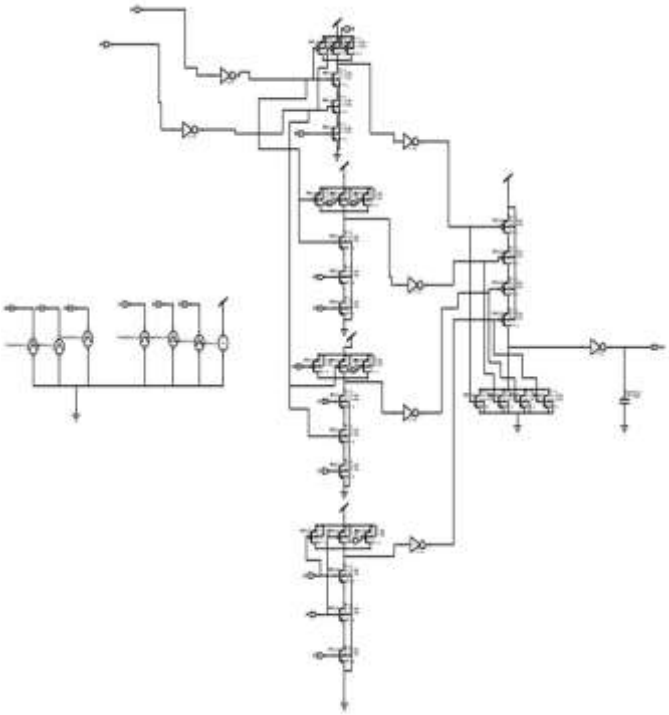

Figure 9. Schematic of 4x1 multiplexer using CMOS

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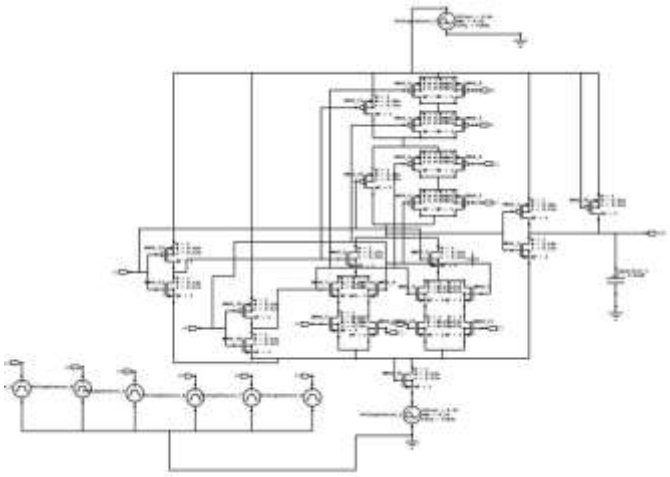

Figure 10. Schematic of 4x1 multiplexer using 2PASCL adiabatic logic

VI. SIMULATION AND RESULT

In this section simulation of our proposed logic and CMOS based multiplexer are designed on s-edit of tanner tool at 90nm technology. Below figures show the simulated waveforms of different multiplexer designed by conventional CMOS and proposed logic.

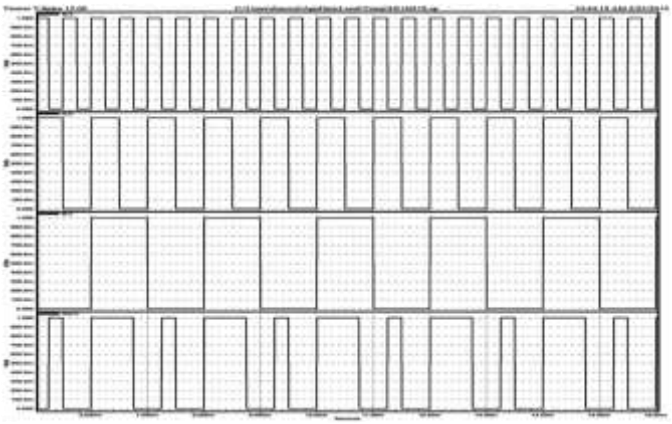

Fig. 8. Simulation waveform of 2x1 multiplexer using CMOS

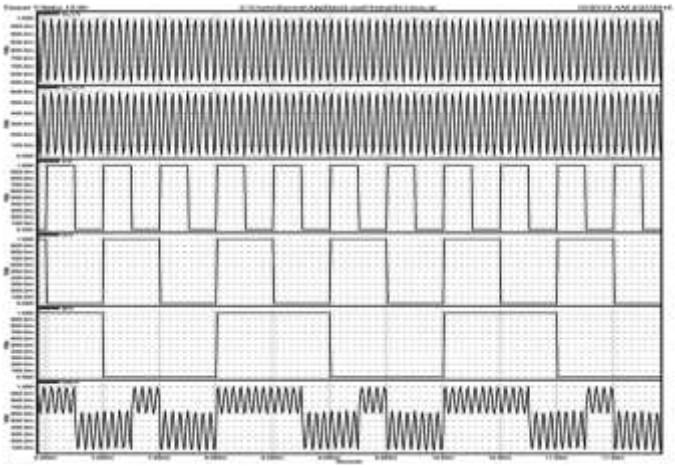

Fig. 9.simulation waveform of 2x1 multiplexer using 2PASCL LOGIC

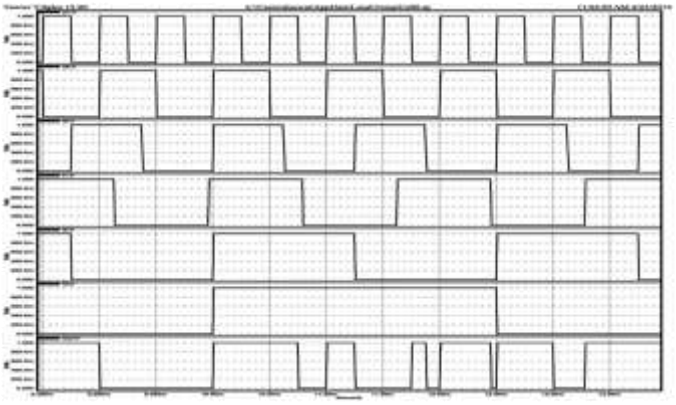

Fig. 7. Simulation waveform of 4x1 multiplexer using CMOS logic

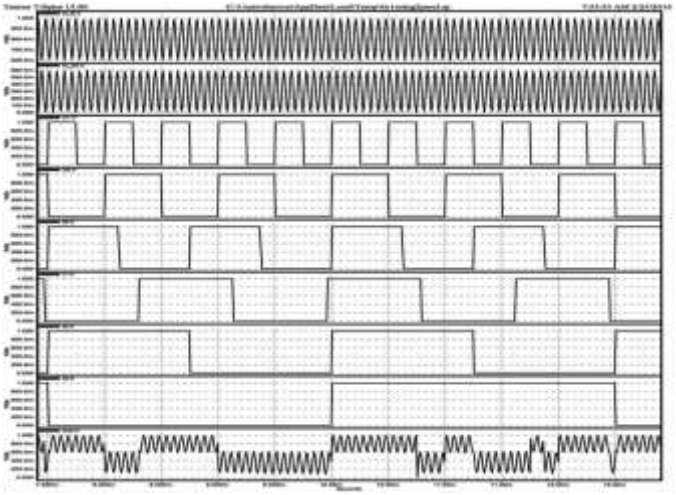

Fig. 8. Simulation waveform of 4x1 multiplexer designed by 2PASCL logic

TABLE III. COMPARISON OF SIMULATION RESULT OF PROPOSED LOGIC WITH CMOS

2x1 multiplexer	Frequency	CMOS(µw)	2PASCL(nw)
	2KHZ	0.252	0.743
	4KHZ	0.447	0.894
	10KHz	1.19	1.04
4x1 multiplexer	2KHZ	0.348	4.17
	4KHZ	0.744	5.31
	10KHZ	1.51	14.81

In TABLE III compares the power dissipation of proposed multiplexer with CMOS multiplexer on the basis of different values of input frequency.

TABLE IV. COMPARISON OF DESIGN MATRIX'S BETWEEN PROPOSED AND CMOS LOGIC

	Parameters	CMOS	2PASCL
2x1 multiplexer	Active devices	20	14
	Total nodes	95	69
	Maximum frequency	10KHZ	10KHZ
	Average power	1.19 (µw)	1.04 (nw)
4x1 multiplexer	Active devices	46	28
	Total nodes	215	135
	Maximum frequency	10KHZ	10KHZ
	Average power	1.51 (µw)	15.04 (nw)

In TABLEIV compare the proposed multiplexer with CMOS multiplexer on the basis of active devices, total nodes and average power dissipation at maximum frequency.

VII. CONCLUSION

This project work is focused on improving the design parameter and observed that the proposed logic based multiplexer have 99.91 and 99.02 percentage power saving compare to CMOS logic based multiplexer.

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