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Simulation of a High Voltage Gain dc-dc Converter Integrating with Coupled Inductor and Two Voltage Multiplier Cells

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***Abstract*:** In this paper, a high voltage gain dc-dc converter is presented for renewable energy applications. This paper develops step up converter which consists of two voltage multiplier cells with coupled inductor in order to achieve the multiple voltage requirements with high voltage gain. And also two capacitances are provided for charging when the device is under turned-off condition, by utilizing the stored energy levels in the coupled inductor which can enhances the voltage transfer capability levels of the system The voltage imbalance levels are compensated at main power switch. The implemented model operates with low resistance $R_{DS(ON)}$ at main power switch which can reduce the switching losses. The developed simulink models are tested and verified within the MATLAB/SIMULINK with multiple output functions with high voltage gains.

***Keywords*: -** *dc/dc converters, Coupled inductor, voltage multiplier.*

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I. INTRODUCTION

The non-conventional sources are available free of cost, are pollution-free and inexhaustible Man has used these sources for many centuries in propelling ships, driving windmills for grinding corn and pumping water, etc. Because of the poor technologies then existing, the cost of harnessing energy from these sources was quite high. Also because of uncertainty of period of availability and the difficulty of transporting this form of energy, to the place of its use are some of the factors which came in the way of its adoption or development. The use of fossil fuels replaced totally the non-conventional methods because of inherent advantages of transportation and certainty of availability; however these have polluted the atmosphere to a great extent.

People began to realize that the fossil fuels are not going to last longer. But unfortunately, coal energy pose serious environmental problems. The combustion of coal may upset the planet's heat balance. As a result of these problems, it was decided by almost all the countries to develop and harness the non-conventional sources of energy, even though they are relatively costlier as compared to fossil-fuel sources. It is hoped that with advancement in technology and more research in the field of development of non-conventional sources of energy, these sources prove to be cost-effective as well. The future of wind, solar, tidal and other energy sources is bright and these will play an important role in the world energy scenario.

Nowadays, photovoltaic (PV) [1] energy appears quite attractive for electricity generation because of its noiseless, pollution-free, scale flexibility, and little maintenance. Due to cost reduction of PV modules and government incentives, grid-connected photovoltaic power systems are getting more and more attention in the last decade. However, the output voltage of PV arrays is relatively low. The generated power of the PV arrays is decreased greatly because of the PV power generation dependence on sun irradiation level, ambient temperature, and unpredictable shadows.

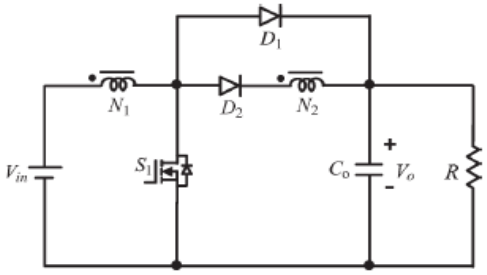

Fig.1 *Conventional high step up dc-dc converter*

Conventionally, the PV arrays are series connected [2-3] to provide high voltage for grid inverters. The generated power of the PV arrays is decreased greatly because of partial shield Based on this reason; the parallel-connected PV arrays are more efficient than series connected. However, the output voltage in the parallel connected PV arrays is low. The converters need to raise low DC voltage (12V) to high DC voltage (380V) [4] for the PV inverter. Thus, the research on the high step-up DC–DC converters was developed. Theoretically, conventional boost converters can achieve high-voltage gain with an extremely high duty ratio. However, the performance of the system will be deteriorated with a high duty cycle due to several problems.

A conventional high step-up dc–dc converter with a coupled inductor technique [5] is shown in Fig.1. The structure of this converter is very simple, and the leakage inductor energy of the coupled inductor can be recycled to the output. Coupled-inductor based converters can achieve high step-up voltage gain. However, the voltage stresses on switch S_1 and diode D_1, which are equal to the output voltage, are high and deteriorates the efficiency. To overcome this, coupled inductor based converter with an active clamp circuit are introduced. Some transformer-based [6] converters like push–pull, or flyback converters can achieve high step-up voltage gain by adjusting the turn ratio of the transformer However; the leakage inductor of the transformer will cause serious problems. Transformer less [7] dc–dc high step-up converter eliminates the drawbacks of transformer based converters.

Some literatures like transformer less with coupled inductor, switched capacitors [8-10], voltage double techniques [11-13] have been widely used. However these techniques have some drawbacks as high charging currents and conduction losses. High step-up converters with two switches, single switch are introduced in some literatures.

This paper presents a high voltage gain dc-dc converter for renewable energy applications. The suggested structure consists of two voltage multiplier cells with coupled inductors in order to achieve the multiple voltage requirements with high voltage gain. And also two capacitances are provided for charging when the device is under turned-off condition; by utilizing the stored energy level in the coupled inductor which can enhances the voltage transfer capability levels of the system. The voltage imbalance levels are compensated at main power switch. The implemented model operated with low resistance $R_{DS(ON)}$ at main power switch which can reduce the switching losses. This developed step-up converter step up the low voltage (40V) to high voltage (600V) with high voltage gain.

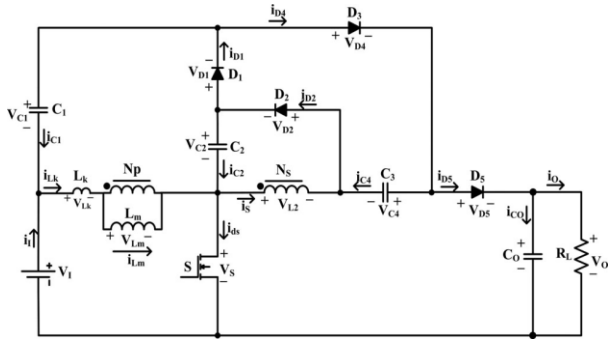

Fig 2Circuit configuration of the high-step-up converter

II. OPERATING PRINCIPLE OF THE CONVERTER

The system design of the proposed framework is appeared in Fig. 2. The proposed system connection has a dc voltage (VI), dynamic force switch (S), coupled inductor, four diodes, then four capacitors Then Capacitor C1 then diode D1 is filling in as braces system exclusively.

The capacitor C3 is included as the capacitor of the long voltage multiplier cell. So that capacitor C2 then diode D2 is the circuit components of the voltage multiplier which upsurge the voltage of clipping capacitor C1. The coupled inductor is open as a perfect transformer with a turn proportion N (NP/NS), a polarizing inductor Lm and spillage inductor Lk.

Keeping in mind the end goal to diminish the circuit investigation of the converter, some preparing are watchful as takes after:

1) All Capacitors are suitably expansive; in this way VC1, VC2, VC3 then VO are reserved to be steady finished one exchanging period;

2) All instruments are perfect however the spillage inductance of the coupled inductor is unhurried. Providing for the previously stated presumptions, the constant conduction mode (CCM) operation of the proposed converter incorporates five interims in one exchanging period.

According to the aforementioned assumptions, the continuous conduction mode (CCM) operation of the proposed converter includes five intervals in one switching period. Some typical waveforms under CCM operation are illustrated in Fig. 3 and the current-flow path of the proposed converter for each stage is depicted in Fig. 4

The operating stages are explained as follows:

1) Stage I [t0 < t < t1 see Fig. 4(a)]: In this stage, switch S is turned ON. In like manner, diodes D2 and D4 are turned ON and diodes D1 and D3 are killed. The dc source (VI) polarizes Lm through S.

2) Stage II [t1 < t < t2 see Fig. 4(b)]: In this stage, switch S and diode D3 are turned ON and diodes D1, D2, and D4 are killed. The dc source VI polarizes Lm through switch S. In this way, the current of the spillage inductor Lk and charging inductor Lm increment straightly

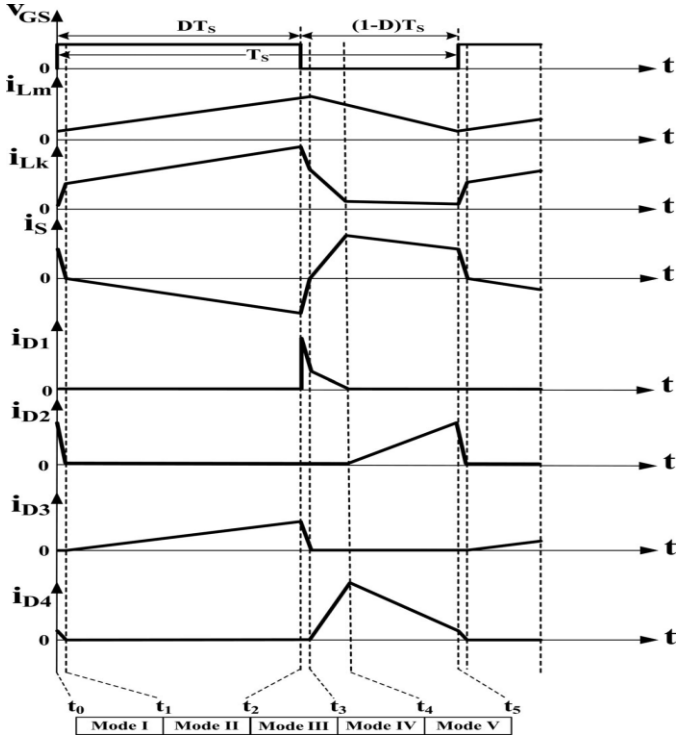

Fig. 3: Some typical waveforms of the proposed converter at CCM operation

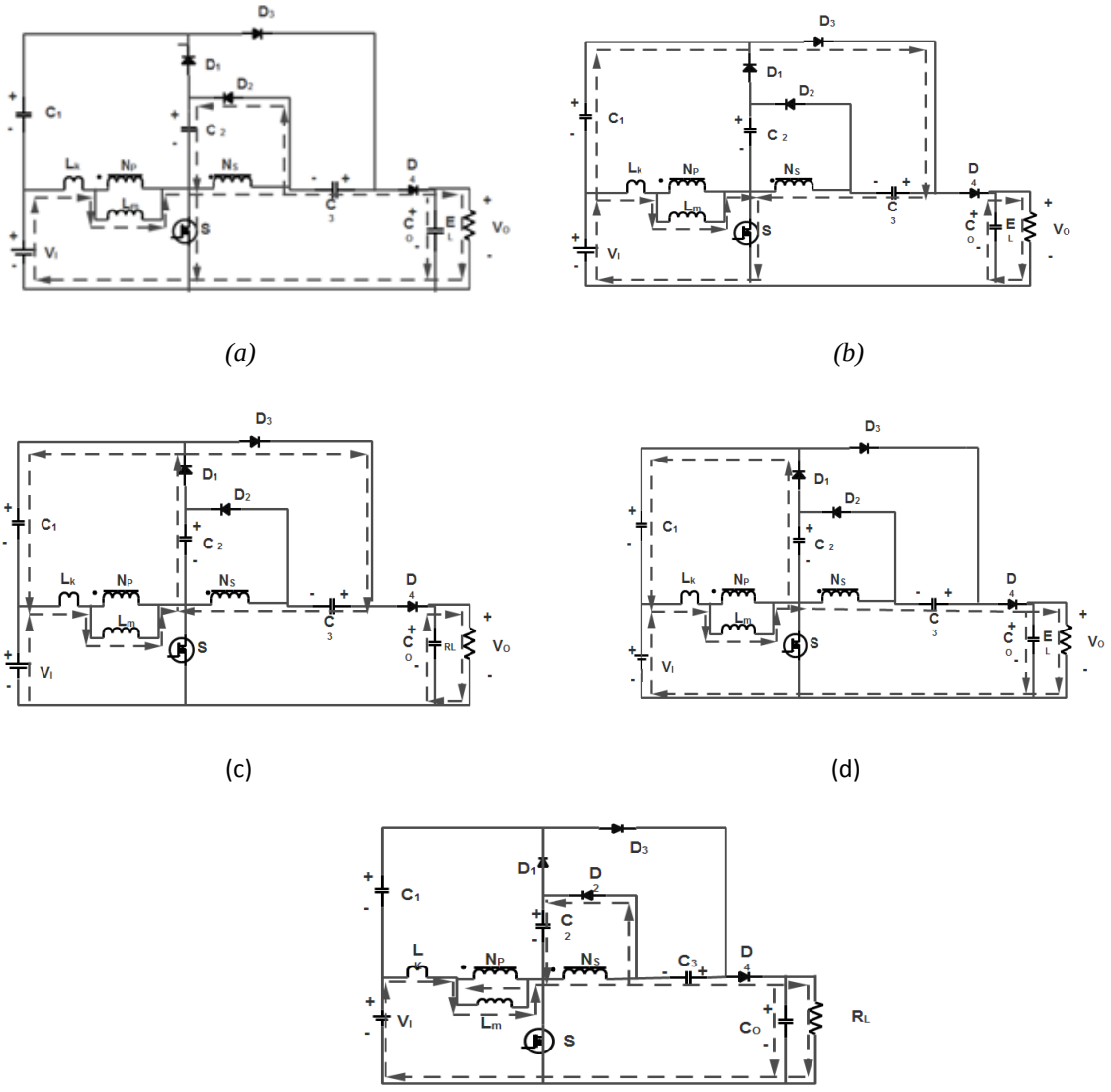

Fig 4:.Current path of operating modes during one switching period at CCM operation. (a) *Stage* I. (b) *Stage* II. (c) *Stage* III. (d) *Stage* IV. (e) *Stage* V.

3) Stage III [t2 < t < t3 see Fig. 4(c)]: In this stage, switch S is killed. Diodes D1 and D3 are turned ON and diodes D2 and D4 are killed. The clasp capacitor C1 is charged by the put away vitality in capacitor C2 and the energies of spillage inductor Lk and polarizing inductor Lm.

4) Stage IV [t3 < t < t4 see Fig. 4(d)]: In this stage, S is killed. Diodes D1 and D4 are turned ON and diodes D2 and D3 are killed.

5) Stage V [t4 < t < t5 see Fig. 4(e)]: In this stage, S is killed. Diodes D2 and D4 are turned ON and diodes D1 and D3 are killed. The streams of the spillage inductor Lk and charging inductor Lm lessening directly.

III.STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

A. CCM Operation

To simplify the steady-state analysis, only stages II, IV, and V are considered since these stages are sufficiently large in comparison with stages I and III.

During stage II, L_k and L_m are charged by dc source V_I.Therefore, the following equation can be written according to Fig. 4(b).

$$V_{L_m} = kV \tag{1}$$

Where k is the coupling coefficient of coupled inductor, which equals to $L_m/(L_m+ L_k)$.Capacitor $C_3$is charged by clamp capacitorC_1,dc source(V_I), and the secondary-side of the coupled inductor. The voltage across the capacitor C_3can be expressed by

$$V_{C3} = V_{C1} + (kn+1)V \tag{2}$$

Where n is the turn ratio of coupled inductor, n=Ns/Np. As shown in Fig. 2(d), during stage IV, Lk and Lm demagnetize to the clamp capacitor $C1$ with the help of capacitor $C2$. Hence, the voltage across Lm can be written as

$$V_{L_m} = k(V_{C2} - V_{C1}) \tag{3}$$

Also, the output voltage can be formulated based on Fig. 2(d)

$$V_O = V_1 + V_{C3} + (kn+1)(V_{C1} - V_{C2}) \tag{4}$$

According to Fig. 2(e), in the time interval of stage V, the voltage across L_m can be expressed by

$$V_{L_m} = -\frac{V_{C2}}{n} \tag{5}$$

Moreover, the output voltage is derived as

$$V_O = V_1 + V_{C3} + \left(\frac{1}{kn} + 1\right)V_{C2} \tag{6}$$

According to aforementioned assumption, the output capacitor voltage is constant during one switching period. Therefore, by equalization of (4) and (6), the following equation is derived as:

$$V_{C1} = \frac{(kn+1)}{kn}V_{C2} \tag{7}$$

Using the volt-second balance principle on L_m and equations (1), (3), (5) and (7), the voltages across capacitors C_1 and C_2 is obtained as

$$V_{C1} = \frac{(kn+1)D}{(1-D)}V_1 \tag{8}$$

$$V_{C2} = \frac{knD}{1-D}V_1 \tag{9}$$

Substituting (8) into (2), yields

$$V_{C3} = \frac{kn+1}{1-D}V_1 \tag{10}$$

Substituting (9) and (10) into (6), the voltage gain is achieved as

$$M_{CCM} = \frac{2+kn+knD}{1-D}V_1 \tag{11}$$

When k equals 1, the ideal voltage gain is obtained as

$$M_{CCM} = \frac{2+n+nD}{1-D}V_1 \tag{12}$$

Based on the description of the operating modes, the voltage Stresses on the active switch S and diodes D_1, D_2, D_3 , and D_4 are expressed as

$$V_{DS} = V_{D1} = \frac{1}{1-D} V_1 = \frac{1}{2+2n}\left(V_O + nV_1\right) \tag{13}$$

$$V_{D3} = V_{D4} = \frac{1+n}{1-D} V_1 = \frac{1}{2}\left(V_O + nV_1\right) \tag{14}$$

$$V_{D2} = \frac{n}{1-D} V_1 = \frac{n}{2+2n}\left(V_O + nV_1\right) \tag{15}$$

According to Fig. 4, the average value of input current can be achieved as follows when switch is turned on/off:

$$I_{in(on)} = \left(n+1\right) I_{D3} + I_{L_m} \tag{16}$$

$$I_{in(off)} = I_O \tag{17}$$

From (16) and (17), the average current value of magnetizing inductor can be obtained as follows:

$$I_{L_m} = \frac{\left(M_{CCM} - 2 - n\right) I_O}{D} = \frac{2\left(n+1\right)}{1-D} I_O \tag{18}$$

The integral form of the current equation of magnetizing inductor can be written as

$$i_{L_m}\left(t\right) = i_{L_m}\left(t_o\right) + \frac{1}{L_m}\int_{i0}^{i} v_{L_m}\left(\tau\right) d\tau \tag{19}$$

Substituting (16) into (19), and for k = 1, t = DT, and $t_0 = 0$, yields

$$\Delta i_{L_m} = \frac{DV_{in}}{L_m f_s} \tag{20}$$

According to Fig. 3 and applying the ampere–second balance principle on capacitors, the average current values of diodes are equal to I_o . Therefore, the peak values of diodes D_3 and D_4 can be obtained as

$$i_{D3(peak)} = \frac{2I_O}{D} \tag{21}$$

$$i_{D4(peak)} = \frac{2I_O}{1-D} \tag{22}$$

$$i_{s(peak)} = i_{D1(peak)} = \left(\frac{2+n+nD}{D\left(1-D\right)}\right) I_O + \frac{DV_{in}}{L_m f_s} \tag{23}$$

Neglecting modes I and III, the time interval of modes IV and V are given as

$$d_4 = \frac{2I_O}{i_{D1(peak)}} = \frac{1-D}{n+1} \tag{24}$$

$$1 - D - d_1 = d_5 \tag{25}$$

From equation (25), the peak value of diode D_2 is obtained as

$$i_{D2(peak)} = \frac{2\left(n+1\right) I_O}{n\left(1-D\right)} \tag{26}$$

CAPACITORS AND INDUCTANCE CALCULATION:

The minimum value of the magnetizing inductance can be calculated as follows:

$$L_{m\min} = \frac{D(1-D)^2 R_L}{8 f_s \left[n^2 (1+D) + n(3+D) + 1 \right]} \tag{27}$$

According to, the magnetizing inductance should be more than 148 μH. A coupled inductor with the magnetizing inductance of the 300 μH is employed to guarantee the CCM operation of the implemented converter.

In order to design the size of the capacitors, it should be followed four conditions regarding the ripple in the output voltage. The conditions are ripple of the capacitor current, ripple due to the equivalent series resistance (ESR) of the capacitor, ripple due to the equivalent series inductance (ESL) of the capacitor, and the hold-up time requirement for load step response which the last condition is for the output capacitor. First, the design is started by considering only the first condition which ESRs and ESLs are not known before selecting the capacitor. Then, ESRs and ESLs are obtained from the capacitors' datasheets. The total output voltage ripple is checked to make sure that it is below the admissible value by considering ESRs and ESLs. In addition, the ripple of the capacitor currents are calculated and compared to the value mentioned in datasheet to make sure that the selected capacitors are in consistent with the practical conditions. In order to calculate the voltage ripple of a capacitor ESR and ESL, the following equation is used:

$$V_C(t) = V_C(t_0) + \frac{1}{C}\int_{t0}^{t} i(t)dt \tag{28}$$

Since the average currents through capacitors C_1, C_2 , $C_3$and C_O are zero under steady state, the average current values of diodes are equal to I_O . Therefore, according to the CCM operation modes shown in Fig. 3 and (31), the voltage ripple of all capacitors can be given as follows:

$$\Delta V_{C1,2,3} = \frac{V_O}{R_L C}, \Delta V_{CO} = \frac{D V_O}{R_L C_O f_s} \tag{29}$$

The peak-to-peak voltage across ESR of a capacitor can also be considered as follows:

$$\Delta V_C^{ESR} = r_C \Delta I_C \tag{30}$$

According to equations (21)–(23), (26) and (30), the peak-to peak voltages across the capacitors ESR are expressed below

$$\Delta V_{C1}^{ESR} = r_{C1}\left[\left(\frac{4+n+(n-2)D}{D(1-D)}\right) I_O + \frac{D V_{in}}{L_m f_s}\right]$$

$$\Delta V_{C2}^{ESR} = r_{C2}\left[\left(\frac{2+n+nD+\dfrac{2D(n+1)}{n}}{D(1-D)}\right) I_O + \frac{D V_{in}}{L_m f_s}\right]$$

$$\Delta V_{C3}^{ESR} = r_{C3}\frac{2I_O}{D(1-D)}$$

$$\Delta V_{CO}^{ESR} = r_{CO}\frac{2I_O}{1-D} \tag{31}$$

The peak-to-peak voltage across ESL of a capacitor can also be considered as follows:

$$\Delta V_C^{ESL} = L_C \frac{di_C}{dt} \tag{32}$$

According to equations (21)–(23), (26) and (32), the peak-to peak voltages across ESL of the capacitors are expressed below

$$\Delta V_{C1}^{ESL} = L_{C1}\left[\frac{(n+1)\left[\left(\frac{2+n+nD}{D(1-D)}\right)I_O + \frac{DV_{in}}{L_m f_s}\right]}{(1-D)T_S} + \frac{2I_O}{D^2 T_S}\right]$$

$$\Delta V_{C_2}^{ESL} = L_{C_2}\left[\frac{(n+1)\left[\left(\frac{2+n+nD}{D(1-D)}\right)I_O + \frac{DV_{in}}{L_m f_s}\right]}{(1-D)T_S} + \frac{2(n+1)^2 I_O}{n^2(1-D)^2 T_S}\right]$$

$$\Delta V_{C3}^{ESL} = L_{C3}\left(\frac{2I_O}{(1-D)^2 T_S} + \frac{2I_O}{D^2 T_S}\right) \qquad (33)$$

$$\Delta V_{CO}^{ESL} = L_{CO}\left(\frac{2I_O}{(1-D)^2 T_S}\right)$$

By imposing a certain ripple value, the sizes of the capacitors are calculated using equation (29). Then, by knowing ESRs and ESLs of the chosen capacitors, the total voltage ripple, $\Delta V_C + \Delta V_C^{ESR} + \Delta V_C^{ESL}$, have to be checked to be less than the desired proportion of capacitor voltages. An important condition in the design of the output capacitor in any converter is the hold-up time requirement for step-load response. A load variation, ΔI_{out}, in the load current causes a load voltage change, ΔV_{CO}. It takes a short non zero time, τ, until the feedback loop responds to bring back the load voltage to its steady-state value. According, this duration is usually approximated as $1/(0.1 f_S)$. During the time τ, the capacitor must hold the load voltage, such that ΔV_{CO} remains under the acceptable ripple value, usually 1% of V_{out}. This means that the capacitor value has to be at least

$$C_{O\min} = \frac{\Delta I_{out}}{0.01 V_{out}}\tau \qquad (34)$$

IV SIMULATION RESULTS:

The performance of the presented converter is assessed using these specifications given in Table

Specifications	Values
Input dc voltage	40V
Output dc voltage	600V
Coupled Inductor	L_K:1µH,Lm:300µH
CapacitorsC_1,C_2,C_3.C_O	(47,47,100,220)µF
Switching Frequency	60KH_Z

Table 1: SIMULATION PARAMTERS

The results verify the analysis of the steady state operation. The voltage on the switch (V_{DS}) during the turn-off state is clamped. Therefore, a low-voltage-rated switch can be used to improve the efficiency of the converter. Fig. 5 shows the simulation circuit of the converter Fig.6 shows the output of the converter, Fig. 7 depicts the voltage stresses on the diodes, fig 8 shows that the energy stored in the leakage inductance is recycled to capacitor $C1$ through diode D_1, and magnetizing inductor current. Fig 9 shows diode currents.Fig.10 shows capacitors voltages.

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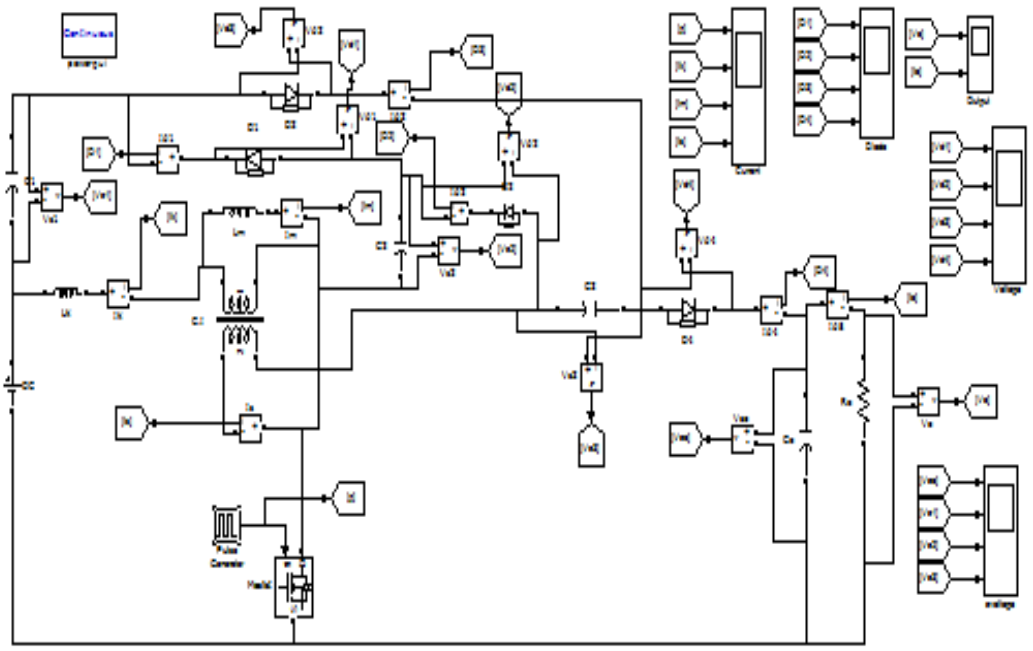

Fig5 **:** Simulation circuit for proposed system

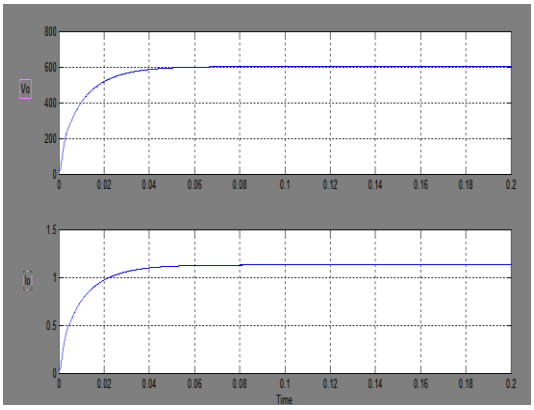

Fig6: Output voltage and current

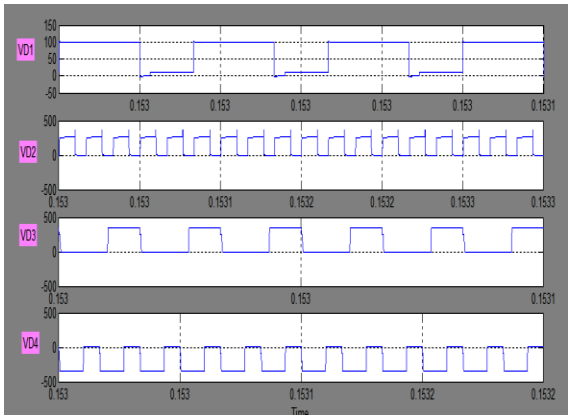

Fig7: Diode voltages V_{D1},V_{D2},V_{D3},V_{D4}

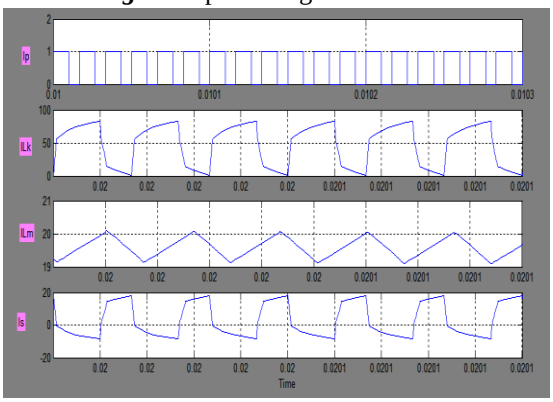

Fig 8: Pulse,Leakage inductor ,Magnetizing inductor, Secondary currents

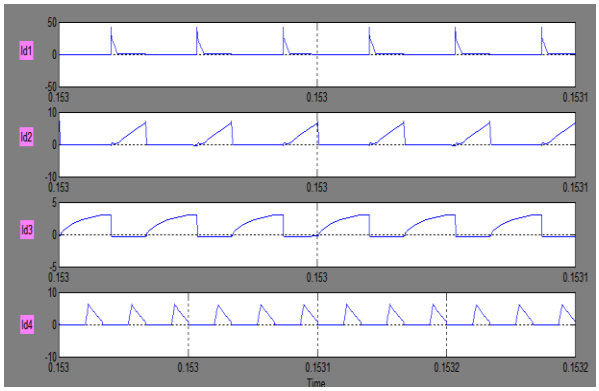

Fig 9**:** Diode currents I_{D1},I_{D2},I_{D3},I_{D4}

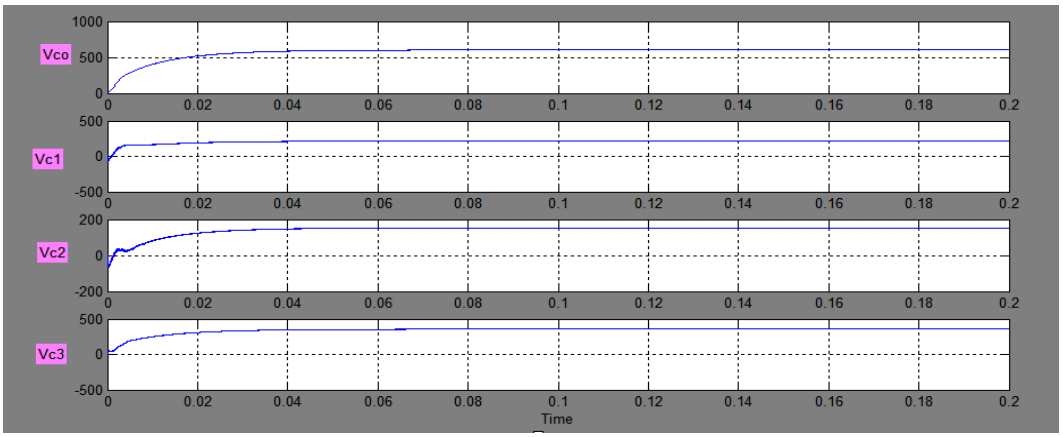

Fig 10: Voltages of capacitors V_{CO},V_{C1},V_{C2},V_{C3}

The current waveforms of the diodes and the coupled inductor (i_{LK}) shown in validate the analysis and the feasibility of the proposed converter. The input current ripple is as much as other proposed high-step-up converters. However, a low-pass filter can be used to reduce the input current ripple. The results show the high conversion efficiency of the presented converter

V. CONCLUSION

This paper concentrated on the high step up dc-dc converter for non-conventional energy sources. The converter is flexible for distributed generations based on the non-conventional energy resources, which has to be performing with high voltage gain transfer functions. The energy stored under the leakage inductance is given back to multiplier module which wills leads to enhance the system performance. The voltage imbalances in the main power switch related losses were minimized by the presence of low resistance utilization. The implemented model has produced less steady state error which improves the behaviour of the system. The capacitances are utilized to charge under turned off conditions. The designed simulink models are tested and verified within the simulation.

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