Simulation of High Step-Up Resonant Parallel LC Converter for Grid Connected Renewable Energy Sources

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Abstract:- With the rapid improvement of large-scale renewable energy sources and HVDC grid, it is a capable alternative to connect the renewable energy sources to the HVDC grid with a pure dc system, in which high-power high-voltage step-up dc–dc converters are the key equipment to transmit the electrical energy. This paper presents a High step up LC converter it can achieve high voltage gain using an *LC* parallel resonant tank. Also provided zero voltage switching (ZVS) technology under switch turn-On condition also at turn-Off conditions at main power switches by rectifying diodes to reduce the conduction losses. The operation principle of the converter and its resonant parameter selection is presented in this paper. The operation principle of the converter has been successfully verified with the help of MATLAB/SIMULINK.

Keywords — Renewable energy, resonant converter, soft switching, voltage step-up, voltage stress.

I.INTRODUCTION

The development of renewable energy sources is crucial to relieve the pressures of exhaustion of the fossil fuel and environmental pollution. At present, most of the renewable energy sources are utilized with the form of ac power. The generation equipments of the renewable energy sources and energy storage devices usually contain dc conversion stages and the produced electrical energy is delivered to the power grid through dc/ac stages, resulting in additional energy loss. Moreover, the common problem of the renewable energy sources, such as wind and solar, is the large variations of output power, and the connection of large scale of the renewable sources to the power grid is a huge challenge for the traditional electrical equipment, grid structure, and operation. DC grid, as one of the solutions to the aforementioned issues, is an emerging and promising approach which has drawn much attention recently [1]–[4]. At present, the voltages over the dc stages in the generation equipments of the renewable energy sources are relatively low, in the range of several hundred volts to several thousand volts hence, high-power high-voltage step-up dc–dc converters are required to deliver the produced electrical energy to the HVDC grid. Furthermore, as the connectors between the renewable energy sources and HVDC grid, the step-up dc–dc converters not only transmit electrical energy, but also isolate or buff kinds of fault conditions; they are one of the key equipments in the dc grid [5]. As of late, the powerful high-voltage step up dc–dc converters has been concentrated broadly [6]-[9]. The transformer is an advantageous way to deal with acknowledge voltage step up. The excellent full-connect (FB) converter, single dynamic extension (SAB) converter, what's more, LCC full converter are concentrated on and their execution is looked at for the offshore wind farm application[6].

The three-stage topologies, for example, three-stage SAB converter, arrangement resonant converter, and double dynamic extension converter, which are more suitable for high-control applications because of reduced current anxiety of every scaffold, are additionally contemplated furthermore, intended for high-control high-voltage step up applications [10]. The rising particular dc–dc converter, which utilizes two secluded multilevel converters connected by a medium frequency transformer, is appropriate for the application in the HVDC matrix [11]. For these disengaged topologies, the primary deterrent is the creation of the powerful high-voltage medium-recurrence transformer and there is no report about the transformer model yet. Multiple small-capacity isolated converters connected in series and/or parallel to form a high-power high-voltage converter is an effective means to avoid the use of single large-capacity transformer [12]–[14]. For the application where galvanic isolation is not mandatory, the use of a transformer would only increase the cost, volume, and losses, especially for high-power high-voltage applications [15]. Several nonisolated topologies for high-power high-voltage applications [16]–[17]. A boost converter is adapted by the researchers of Converteam company to transmit energy from \pm 50 to \pm 200 kV [18]. To obtain the higher voltage gain, Enjeti *et al.* proposed a multiple-module structure, which consists of a boost converter and

a buck/boost converter connected in input parallel output-series [19]. The output power and voltage are shared by the two converters and the voltage and current ratings of switches and diodes are correspondingly reduced. However, the efficiency of a boost or buck/boost converter is relatively low due to the hard switching of the active switch and the large reverse recovery loss of the diode. The soft-switching technology is critical to improve the conversion efficiency,



Fig.1 Proposed resonant step-up converter

Especially for high-voltage applications .Recently, several soft-switching topologies for high power high-voltage applications have been proposed. In the converter topologies based on resonant switched capacitor (RSC) are proposed with reduced switching loss and modular structure.

The shortage of the RSC-based converter is the poor voltage regulation and the requirement of a large number of capacitors. Jovcicet al. proposed a novel type of resonant step-up converter with potentially soft-switching operation, which utilizes thyristors as switches and does not suffer from excessive switch stresses and reverse recovery problems; moreover, a large voltage gain is easily obtained [18]–[19]. Similarly, in [20], a new family of resonant transformer less modular dc– dc converters is proposed and the main feature of the proposed converters is that the unequal voltage stress on semiconductors of thyristor valve is avoided with the use of active switching network, which is composed of an ac capacitor and four identical active switches. Thyristors have large voltage and current ratings; however, the use of thyristor limits the switching frequency of the converters are unidirectional magnetized in [22]–[24], leading to lower utilization of the magnetic core, which means that a great volume of core is required.

II.CONVERTER STRUCTURE AND OPERATION PRINCIPLE

The proposed resonant step-up converter is appeared in Fig. 1. The converter is made out of a FB switch system, which comprises Q_1 through Q_4 , a LC parallel resonant tank, a voltage double rectifier, and two info blocking diodes, D_{b1} and D_{b2} . The consistent state working waveforms are appeared in Fig. 2 and point by point operation methods of the proposed converter are appeared in Fig. 3. For the proposed converter, Q_2 and Q_3 are tuned on furthermore, off at the same time; Q_1 and Q_4 are tuned on and off all the while. Keeping in mind the end goal to rearrange the investigation of the converter, the taking after suspicions are made:

1) All switches, diodes, inductor, and capacitor are perfect segments;

2) Yield channel capacitors C_1 and C_2 are equivalent and huge enough so that the yield voltage V_o is viewed as consistent in an exchanging period T_s .

A. Mode 1 [t₀, t₁] [See Fig. 3.3(a)]

During this mode, Q_1 and Q_4 are turned on resulting in the positive input voltage Vin across the LC parallel resonant tank, i.e., $v_{Lr}=v_{Cr}=V_{in}$. The converter operates similar to a conventional boost converter and the resonant inductor L_r acts as the boost inductor with the current through it increasing linearly from I_0 .

The load is powered by C_1 and C_2 . At t1, the resonant inductor current i_{Lr} reaches I_1

$$I_{1} = I_{o} + \frac{V_{in}T_{1}}{L_{r}} \tag{1}$$

Where T1 is the time interval of t_0 to t_1 .

In this mode, the energy delivered from V_{in} to L_r is

$$E_{in} = \frac{1}{2} L_r \left(I_1^2 - I_0^2 \right)$$
 (2)



B. Mode 2 [t₁, t₃] [See Fig.3. 3(b)]

At t_1 , Q_1 and Q_4 are turned off and after that L_r resonates with C_r , v_{Cr} decreases from V_{in} and i_{Lr} increases from I_1 in resonant form. Taking into account the parasitic output capacitors of Q_1 through Q_4 and junction capacitor of D_{b2} , the equivalent circuit of the converter after t_1 is shown in Fig. 4(a),in which CD_{b2} , CQ_1 , and CQ_4 are charged, CQ_2 and CQ_3 are discharged. In order to realize zero-voltage switching (ZVS) for Q_2 and Q_3 , an additional capacitor, whose magnitude is about ten times with respect to CQ_2 , is connected in parallel with D_{b2} . Hence, the voltage across D_{b2} is considered unchanged during the charging/discharging process and Db2 is equivalent to be shorted. Due to C_r is much larger than the parasitic capacitances, the voltages across Q_1 and Q_4 increase slowly. International Journal on Recent and Innovation Trends in Computing and Communication Volume: 4 Issue: 3



(b) Fig 4.Further equivalent circuits of Mode 2. (a) [t₁,t₂]. (b) [t₂,t₃].







Fig. 3 Equivalent circuits of each operation stages. (a) [t0,t1]. (b) [t1,t3]. (c) [t3,t4]. (d)[t4,t5]. (e) [t5,t6]. (f) [t6,t8].(g)[t8,t9].(h)[t9,t10].

As a result, Q_1 and Q_4 are turned off at almost zero voltage in this mode. When v_{Cr} drops to zero, i_{Lr} reaches its maximum magnitude. After that, v_{Cr} increases in negative direction and i_{Lr} declines in resonant form. At t_2 , $v_{Cr} = -V_{in}$, the voltages across Q_1 and Q_4 reach V_{in} , the voltages across Q_2 and Q_3 fall to zero and the two switches can be turned on under zero-voltage condition. It should be noted that although Q_2 and Q_3 could be turned on after t_2 , there are no currents flowing through them. After t_2 , *Lrcontinues* to resonate with C_r , v_{Cr} increases in negative direction from $-V_{in}$, i_{Lr} declines in resonant form. D_{b2} will hold reversed-bias voltage and the voltage across Q_4 continues to increase from V_{in} .

The voltage across Q_1 is kept at V_{in} . The equivalent circuit of the converter after t_2 is shown in Fig. 4(b),in which D_2 and D_3 are the antiparallel diodes of Q_2 and Q_3 , respectively. This mode runs until v_{Cr} increases to -Vo/2 and i_{Lr} reduces to I_2 , at t_3 , the voltage across Q_4 reaches Vo/2 and the voltage across D_{b2} reaches $Vo/2 - V_{in}$.

It can be seen that during t_1 to t_3 , no power is transferred from the input source or to the load, and the whole energy stored in the *LC* resonant tank is unchanged, i.e.,

$$\frac{1}{2}L_r I_1^2 + \frac{1}{2}C_r V_{in}^2 = \frac{1}{2}L_r I_2^2 + \frac{1}{2}C_r \left(\frac{V_0}{2}\right)^2$$
(3)

We have

$$i_{L_r}(t) = \frac{V_{in}}{Z_r} \operatorname{Sin}\left[\omega_r(t-t_1)\right] + I_1 \operatorname{COS}\left[\omega_r(t-t_1)\right]$$
(4)

$$V_{C_r}(t) = V_{in} \operatorname{COS}\left[\omega_r(t-t_1)\right] - I_1 Z_r \operatorname{Sin}\left[\omega_r(t-t_1)\right]$$
(5)

$$T_{2} = \frac{1}{\omega_{r}} \left[\arcsin\left(\frac{V_{in}}{\sqrt{V_{in}^{2} + \frac{L_{r}I_{1}^{2}}{C_{r}}}}\right) + \arcsin\left(\frac{V_{0}}{2\sqrt{V_{in}^{2} + \frac{L_{r}I_{1}^{2}}{C_{r}}}}\right) \right]$$
(6)

where

$$\omega_r = 1/\sqrt{L_r C_r}, Z_r = \sqrt{L_r/C_r},$$
 and T_2 is the time interval of t_1 to t_3 .

C. Mode 3 [t3, t4] [See Fig. 3.3(c)]

At t_3 , $v_{Cr} = -Vo/2$, D_{R1} conducts naturally, C_1 is charged by i_{Lr} through D_{R1} , v_{Cr} keeps unchanged, and i_{Lr} decreases linearly. At t_4 , $i_{Lr} = 0$. The time interval of t_3 to t_4 is

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$$T_3 = \frac{2I_2L_r}{V_2} \tag{7}$$

The energy delivered to load side in this mode is

$$E_{out} = \frac{V_o I_2 T_3}{4} \tag{8}$$

The energy consumed by the load in half-switching period is

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$$E_R = \frac{V_o I_o T_s}{2} \tag{9}$$

Assuming 100% conversion efficiency of the converter and according to the energy conversation rule, in half-switching period

$$E_{in} = E_{out} = E_R \tag{10}$$

Combining (7), (8), (9), and (10), we have

$$I_2 = V_o \sqrt{\frac{I_o T_s}{V_o L_r}} \tag{11}$$

$$T_3 = 2\sqrt{\frac{T_s I_o L_r}{V_o}}$$
(12)

D. Mode 4 [t₄, t₅] [See Fig. 3.3(d)

At t_4 , i_{Lr} decreases to zero and the current flowing through D_{R1} also decreases to zero, and D_{R1} is turned off with zero current switching (ZCS); therefore, there is no reverse recovery.

After t_4 , Lr resonates with C_p , C_r is discharged through L_p , v_{Cr} increases from -Vo/2 in positive direction, and i_{Lr} increases from zero in negative direction. Meanwhile, the voltage across Q_4 declines from Vo/2. At t_5 , $v_{Cr} = -V_{in}$, and $i_{Lr} = -I_3$. In this mode, the whole energy stored in the *LC* resonant tank is unchanged, i.e.

$$\frac{1}{2}C_r \left(\frac{V_o}{2}\right)^2 = \frac{1}{2}L_r I_3^2 + \frac{1}{2}C_r V_{in}^2$$
(13)

We have

$$I_o = I_3 = \frac{1}{2} \sqrt{\frac{C_r (V_o^2 - 4V_{in}^2)}{L_r}}$$
(14)

$$i_{L_r}(t) = -\frac{V_o}{2\omega_r L_r} \operatorname{Sin}\left[\omega_r \left(t - t_5\right)\right]$$
(15)

$$v_{c_r}(t) = \frac{-V_o COS\left[\omega_r\left(t - t_5\right)\right]}{2}$$
(16)

$$T_4 = \frac{1}{\omega_r} \arccos\left(\frac{2V_{in}}{V_o}\right) \tag{17}$$

Where T_4 is the time interval of t_4 to t_5 .

E. Mode 5 [t₅, t₆] [See Fig 3.3(e)]

If Q_2 and Q_3 are turned on before t_5 , then after t_5 , L_r is charged by V_{in} through Q_2 and Q_3 , i_{Lr} increases in negative direction, and the mode is similar to Mode 1. If Q_2 and Q_3 are not turned on before t_5 , then after t_5 , L_r will resonate with C_r , the voltage of node $A v_A$ will increase from zero and the voltage of node $B v_B$ will decay from Vin zero-voltage condition will be lost if Q_2 and Q_3 are turned on at the moment. Therefore, Q_2 and Q_3 must be turned on before t_5 to reduce switching loss. The operation modes during $[t_6, t_{10}]$ are similar to Modes2–4, and the detailed equivalent circuits are shown in Fig. 3.3(f) to (h). During $[t_6, t_{10}]$, Q_2 and Q_3 are turned off at almost zero voltage, Q_1 and Q_4 are turned on with ZVS, and D_{R2} is turned off with ZCS.

III.ANALYSIS AND DESIGN OF THE CONVERTER

A. Voltage Rating and DC Fault Response

According to the analysis of Section II, the voltage stresses of Q_1 and Q_2 are the input voltage Vin , the voltage stresses of Q_3 and Q_4 are half of the output voltage, i.e., Vo/2, the voltage stresses of D_{b1} and D_{b2} are $Vo/2-V_{in}$. The total voltage stress of the primary semiconductor devices is $2V_{o}$, which is half of that. It implies that much less semiconductor devices are required in the proposed step-up converter, resulting in low conduction and switching losses and low cost. Moreover, the peak voltages across

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the resonant inductor and resonant capacitor are Vo/2, which is also half of that. Lower peak voltage indicates that the insulation is easy to be implemented, leading to the reduction of the size of the resonant tank.

B. Voltage Balance between C1 and C2

The previous analysis is based on the assumption that voltages across C_1 and C_2 are, respectively, half of output voltage. Provided that $Vc_1 = Vc_2$, for example, $Vc_1 > Vo/2 > Vc_2$, according to the operation principle of Fig. 2, the peak current of i_c at t_3 will be smaller than that at t_8 , which means that the average current flowing into C_1 will be smaller than the average current flowing into C_2 . Due to C_1 and C_2 power the same load, therefore, Vc_1 decreases and Vc_2 increases, and finally they share the same output voltage. Vice versa, i.e., Vc_1 increases and Vc_2 decreases under the presumption that $Vc_1 < Vo/2 < Vc_2$.

C. Analysis of the Converter

From Fig. 2, we have

$$T_1 + T_2 + T_3 + T_4 = \frac{T_s}{2} \tag{18}$$

Combining (1), (2), and (14) yields

$$V_o I_o T_s = \frac{V_{in}^2 T_1^2}{L_r} + V_{in} T_1 \sqrt{\frac{C_r \left(V_o^2 - 4V_{in}^2\right)}{L_r}}$$
(19)

$$T_{1} = \frac{\sqrt{\frac{C_{r}\left(V_{o}^{2} - 4V_{in}^{2}\right) + 4V_{o}I_{o}T_{s}}}{L_{r}} - \sqrt{\frac{C_{r}\left(V_{o}^{2} - 4V_{in}^{2}\right)}{L_{r}}}{2\frac{V_{in}}{L_{r}}}$$
(20)

From (17), the gain of V_o/V_{in} is expressed as

$$\frac{V_o}{V_{in}} = \frac{2}{\cos(\omega_r T_4)} \tag{21}$$

Substituting (20) into (1) yields

$$I_{1} = \sqrt{\frac{C_{r} \left(V_{o}^{2} - 4V_{in}^{2}\right) + 4V_{o}I_{o}T_{s}}{4L_{r}}}$$
(22)

Substituting (22) into (3) yields

$$I_2 = \sqrt{\frac{V_o I_o T_s}{L_r}}$$
(23)

Substituting (22) into (6) yields

$$T_{2} = \frac{1}{\omega_{r}} \left[\arcsin\left(\frac{2V_{in}}{\sqrt{V_{o}^{2} + \frac{4V_{o}I_{o}T_{s}}{C_{r}}}}\right) + \arcsin\left(\frac{V_{0}}{\sqrt{V_{o}^{2} + \frac{4V_{o}I_{o}T_{s}}{C_{r}}}}\right) \right]$$
(24)

Combining (12), (17), (18), (20), and (24), we have

$$\frac{\sqrt{\frac{C_r \left(V_o^2 - 4V_{in}^2\right) + 4V_o I_o T_s}{L_r}} - \sqrt{\frac{C_r \left(V_o^2 - 4V_{in}^2\right)}{L_r}}}{\frac{2V_{in}}{L_r}} + \frac{1}{\omega_r} \left[\arcsin\left(\frac{2V_{in}}{\sqrt{V_o^2 + \frac{4V_o I_o T_s}{C_r}}}\right) + \arcsin\left(\frac{V_0}{\sqrt{V_o^2 + \frac{4V_o I_o T_s}{C_r}}}\right) \right] + 2\sqrt{\frac{T_s I_o L_r}{V_o}} + \frac{1}{\omega_r} \arccos\left(\frac{2V_{in}}{V_o}\right) = \frac{T_s}{2}$$
(25)

From (25), we can obtain the following equation under unloaded condition (Io = 0):

$$f_s = f_r \left(I_o = 0 \right) \tag{26}$$

Where f_s is the switching frequency and f_r is the resonant frequency of Lr and Cr, *i.e.*

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$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{27}$$

It can be seen that the switching frequency is equal to the resonant frequency under unloaded condition. Actually, it can be seen from Fig. 2 that T1 = T3 = 0 under unloaded condition because there is no energy input and output if the converter is assumed to be lossless. And if Io > 0, then both T1 and T3 are larger than zero; thus, the switching frequency is lower than the resonant frequency; the heavier the load, the lower the switching frequency. Therefore, the maximum switching frequency of the converter is

$$f_{s\max} = f_r \tag{28}$$

From the analysis of Section II, it can be seen that to realize zero-voltage turn-on of the switches, the minimum duty cycle of the converter is

$$D_{\min} = \frac{T_1}{T_s}$$
(29)

As shown in Fig.2 and the previous analysis, the minimum duty cycle also is the effective duty cycle of the converter, during which the primary current flows through the main switches .According to (5), the time interval ΔT of t1 to t2 is

$$\Delta T = \frac{2}{\omega_r} \arcsin\left(\frac{2V_{in}}{\sqrt{V_o^2 + \frac{4V_o I_o T_s}{C_r}}}\right)$$
(30)

The maximum duty cycle of the Converter is

$$D_{\max} = \frac{\frac{T_s}{2} - \Box T}{T_s}$$
(31)

D. Design of the Converter

A 12 MW, 4 kV (\pm 10%)/80 kV step-up converter is taken as an example to design the parameters. Insulated-gate bipolar transistors (IGBTs) are taken as the main switches and fs_{max} is set to be 5 kHz. From (25), one can obtain the expression of *Ts* associated with *Lr* under full-load condition. However, (25) indicates that *Ts* is an implicit function associated with *Lr* and the concrete analytic solution of *Ts* cannot be obtained.

Hence, there is a tradeoff when designing the resonant parameters. The final selection of Lr is 100 μ H, Cr is 2.86 μ F, and the minimum switching frequency is 2.8 kHz, and the peak current of the semiconductor devices is 2890 A, which is about two times of the average input current. Here both D_{min} and D_{max} depend on the output power, the maximum of Dmin is 0.2, and the minimum of Dmax is 0.4. Thus, to realize ZVS for the switches, the duty cycle can be the any value in the range of 0.2–0.4. Therefore, the control of the proposed converter is very simple with constant duty cycle and variable switching frequency.

IV.SIMULATION RESLTS

In order to verify the operation principle and the theoretical analysis, a converter is simulated with MATLAB simulation software and the detailed parameters are listed in Table. All switches used in MATLAB simulation are ideal switches and 15 nF capacitance is added in parallel with Db1 and Db2. Fig.5 shows the simulation results at the output power of 12 MW (Vin = 4 kV), respectively.

Item	Symbol	Value
In Put Voltage	V _{in}	4 KV
Out Put Voltage	V _{out}	80 KV
Resonant Inductance	L _r	100 µH
Switching frequency	f _s	5 KHZ
Resonant Capacitance	Cr	2.86 µF
Filter Capacitance	C _{1,} C ₂	22 µF
Duty Cycle	D	40%

SMULATION PARAMTERS

Fig. from 6 to 10 illustrates the measured waveforms of Vq1,Vq4,Vq2,Vq3,Vdb1, Vdb2,Vcr,Ilr,Ic,Vc1,Vc2,Vo,Io at Po=12MW. the measured waveforms are consistent with the steady-state analysis. As the fig.7 shows, the voltage stress of Q1 and Q2 is 4 kV, the voltage stress of Q3 andQ4 is 40 kV.

Fig.8 and Fig.9..shows voltage stress of Db1 and Db2 is 36 kV, and the peak voltage across the *LC* resonant tank is 40 kV. *Q*1 through *Q*4 are turned on under zero-voltage condition and when they are turned off, the voltage across the device increases slowly from zero. The switching frequencies of the converter at 5 are 2.3 and 5 kHz, respectively. Fig.11 shows simulation results of output power.



Fig.5. simulink model of step up LC resonant converter



6. Gate pulses across Q1Q4,Q2Q3



Fig.7. voltage across the switches Vq1,Vq2,Vq3,Vq4



Fig.8.voltage across the diodes Vdb1,Vdb2



Fig.9. voltage across the resonant &filtering capacitance Vcr,Vc1,Vc2



Fig.10. currents across the resonant tank Iab ,IIr, Ic



Fig.11. output voltage and output current

V.CONCLUSION

A novel High step up LC resonant dc–dc converter is proposed in this paper, which can achieve very high step-up voltage gain and it is suitable for high-power high-voltage applications. The converter utilizes the resonant inductor to deliver power by charging from the input and discharging at the output. The resonant capacitor is employed to achieve zero-voltage turnon and turn-off for the active switches and ZCS for the rectifier diodes. The analysis demonstrates that the converter can operate at any gain value (> 2) with proper control; however, the parameters of the resonant tank determine the maximum switching frequency, the range of switching frequency, and current ratings of active switches and diodes. The converter is controlled by the variable switching frequency. Simulation results verify the operation principle of the converter and parameters selection of the resonant tank

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