Performance Comparision between Capacitor Clamped and Hybrid Multi Level Inverters

T. Murali Krishna Dept of EEE Chaitanya Bharathi Institute of Technology Hyderabad, INDIA *tmurali5@gmail.com*

Abstract— The ability to operate at medium and high voltages with reduced dv/dt across the switches, multi level inverters has given more interest in industrial applications. For the realization of multilevel inverters conventionally various topologies have been proposed. In order to minimize switching elements, losses, size and cost, different hybrid structures have been introduced. In this paper the operation performance of traditional capacitor clamped (Flying Capacitor) and hybrid topology of five level multi level inverters are compared. The results reveal that the total harmonic distortion in the stator current, phase voltage and line voltage is less in hybrid topology than capacitor clamped topology. The simulation is done in MATLAB-Simulink.

Keywords - flying capacitor; multilevel inverter; hybrid; topology.

I. INTRODUCTION

The advancement in the field of power electronics has increased the usage of high power medium voltage drive applications in the industrial arena [1]. In order to get better performance of medium voltage and high power electric drives, the dv/dt and harmonics should be minimized by the introduction of more levels in the output voltage [2]. This has initiated the theory of multilevel inverters for industrial drives to overcome the above said disadvantages [3]. The most famous conventional multilevel inverter topologies proposed are Neutral Point Clamped (NPC), Capacitor Clamped (Flying Capacitor) and cascaded topology [4]. These traditional topologies are frequently preferred for three level inverters realization where as the number of levels required in the output voltage is more than three, then hybrid topologies are introduced [5]. In the flying capacitor model the number of capacitors required is more than hybrid multilevel inverter [6]. In order to improve the power quality by the reduction of harmonic content in the output voltage, to reduce the dv/dt across the switching devices, to decrease the size of the inverter and to minimize the electromagnetic compatibility, hybrid multilevel inverters are preferred [7]. This paper presents the design of capacitor clamped and hybrid five level inverter modeling and the comparison between their performances.

II. CAPACITOR CLAMPED INVERTER

The design of different levels in the output voltage of multi level inverter can also be obtained by connecting number of capacitors in series as shown in figure 2. The figure 1 shows the three phase circuit diagram of five level inverter. Figure 2 shows the single phase circuit of capacitor clamed five level inverter. The capacitors are so chosen to share the voltage equally among them. The number of switches required is given by 6(N-1) where N is the number of levels in the output voltage. In this five level inverter totally 24 IGBTs are required. As the requirement of number of capacitors is more, this topology is more bulky and costly.



Figure 1. Three phase ciruit diagram of capacitor clamed five level inverter.



Figure 2. Single phase circuit of capacitor clapmed five level inverter

		LANOTTITTTODAL	
TIMULULUMAT		TRALLULUART	
TILLIA		TRULLLILLINGT	
ee-	TIMULULUUMT		רתעננוננו
06-	TRALLLEADT		TRILLIULIUM
0	LUNITETTTINUL		
(1)			
1 14 1	a also have	A UM I	a 100 1

Figure 3. Control signals(per phase) for fivelevel capacitor clamped topology.



Figure 4. Phase Voltage of Flying capacitor five level inverter.



Figure 5. FFT of phase voltage of Capacitor clamped five level inverter.

The control circuit output signals required to provide a five level output is shown in figure 3. The phase output voltage of capacitor clamped five level inverter is depicted in figure 4. The Fast Fourier Transform(FFT) gives the information about the fundamental and harmonic content present in the phase voltage which is shown in figure 5. The harmonic distortion present is around 40 percent of the fundamental.

III. HYBRID MULTILEVEL INVERTER

The circuit diagram of a hybrid multilevel inverter for providing five level output is shown in figure 6. The base inverter is a conventional two level three phase inverter and is cascaded with conventional two level single phase inverter.



Figure 6. Circuit diagram of five level Hybrid multilevel inverter.



Figure 7. Single phase euqivalent circuit of hybrid multi level inverter.



Figure 8. Control signals (per phase)for fivelevel hybrid multi level inverter.



Figure 9. Phase Voltage of hybrid five level inverter.



Figure 10. FFT of Phase Voltage of hybrid five level inverter.

The design of hybrid five level inverter requires six switching devices per phase. The number of capacitors required per phase can be minimized. Hence the size and cost of the inverter is less. Figure 7 shows the per phase circuit of hybrid multilevel inverter. The control signals required per phase is shown in figure 8. The phase voltage of the hybrid five level inverter is shown in figure 9. The frequency spectrum of this phase voltage is depicted in figure 10.

IV. FLYING CAPACITOR VS HYBRID MULTI LEVEL INVERTER

The simulation is carried out in MATLAB Simulink environment for modeling the capacitor clamped and hybrid five level inverter topologies. The performance is tested on a 4pole, 220V, 50 Hz squirrel cage induction motor delivering a mechanical torque of 11.9 Nm. The simulation diagrams of these topologies are shown in figures 11 and 12 respectively. From the results it can be concluded that the fundamental component in the phase voltage is more in case of hybrid topology than the capacitor clamped topology. The harmonic content is more in capacitor clamped than hybrid topology. The figure 13 represents the comparison of phase voltages of both topologies.

The stator current of the induction motor when delivering the same load is shown in figure 14. From figure 14 it is observed that the capacitor clamped topology provides more harmonic content in the stator current than hybrid topology.



Figure 11. Simulink model of capacitor clamped topology.



Figure 12. Simulink model of hybrid multi level inverter topology.



Figure 13. Comparison of phase voltages.



Figure 14. Stator current.



Figure 15. FFT of stator current in capacitor clamped topology.



Figure 16. FFT of stator current in hybrid topology.



Figure 17. Electro magnetic Torque developed.

The frequency spectrum of stator current in both the topologies is shown in figures 15 and 16. The harmonic content in the stator current is more in case of flying capacitor topology than hybrid topology. The electromagnetic torque developed is shown in figure 17. It can be concluded that the capacitor clamped inverter provides less ripple torque with high

frequency where as the hybrid multilevel inverter provides torque with more ripple with low frequency.

V. CONCLUSIONS

This paper presents the comparison of the performance of capacitor clamped and hybrid multilevel inverters. The simulation results reveal that the number of switching devices and capacitors required per phase is less in hybrid multilevel inverter than capacitor clamped topology. Hence hybrid multilevel inverter is less weight, less switching losses and cheaper than flying capacitor inverter. The output phase voltage in case of hybrid topology is having fewer harmonic than capacitor clamped topology. The capacitor clamped topology provides high slip than hybrid topology.

REFERENCES

- L. G. Franquelo, J. L. Rodriguez, J. Leon, S. Kouro, R. Portillo, and M. A. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol.2, no. 2, pp. 28-39, Jun. 2008.
- [2] M. Zahra, M. Jafari, Md. R. Islam and J. Zhu, "A comparative study on characteristics of major topologies of voltage source multilevel inverters," *IEEE Innovative Smart Grid Tech.*, pp. 612-617, 2014.
- [3] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electro.*, vol. 54, no. 6, pp. 2930-2945, Dec. 2007.
- [4] P. Thongprasri, "A 5-level three-phase cascaded hybrid multilevel inverter," *IJCEE*, vol. 3, no. 6, pp. 789-794, Dec. 2011.
- [5] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electro*, vol. 49, no. 4, pp. 724-738, Aug. 2002.
- [6] E. Najafi, and A. H. Md. Yatim, "Design and implementation of a new multilevel inverter topology," *IEEE Trans. Ind. Electr.* vol. 59, no. 11, pp. 4148-4154, Nov. 2012.
- [7] T. Murali Krishna, C. Bhargav, A new hybrid Multi Level Inverter to improve the performance of induction motor, IEEE International Conference on Computation of Power, Energy Information and Communication (ICCPEIC), pp.264-268, Apr. 2015.