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# Design and Analysis of 1-Bit Full Adder and Logic Gates

M. K. Musale,
P.G. Student, Department of Electronics & Telecommunication Engineering,Pravara Rural Engineering College, Loni, Maharashtra, India

Prof. S. M. Turkane
Associate Professor, Department of Electronics & Telecommunication Engineering,Pravara Rural Engineering College, Loni, Maharashtra, India

***Abstract***:The scaling of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) are commonly used in high speed integrated circuits, yield smaller and faster more functions at lower cost. Various problems exist with scaling of MOSFET devices i.e. short channel effects (SCE), drain induced barrier lowering, velocity saturation which limits the performance of MOSFETs. Scaling limitations of MOSFET devices leads to lower ON to OFF current ratio limited by 60mV/dec sub threshold slope.A new type of device called "Tunnel FET" is used to overcome these difficulties. TFET can beat 60mV/dec sub-threshold swing of MOSFETs. In Tunnel FET the carrier are generated by band-to-band tunneling and OFF current is low. Tunnel FET have energy barrier in OFF state, which avoids application where leakage is concern of interest. In this Project sub-threshold swing and low OFF current is simulated and its power is analyzed.Basically in VLSI circuit like design of IC we have to simulate all the parameters of the devices & circuit regarding of that IC or any devices like FET, MOSFET, CMOS etc. In device simulation we are most widely use software named as "HSPICE". We are doing analysis of full bit adder. We are going to compare different characteristics.

***Keywords*** :*MOSFET,TFET, HSPICE.*

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## I. Introduction

The Tunnel Field Effect Transistors (TFET) are one of the most promising successors of Metal Oxide Semiconductor Field Effect Transistors (MOSFET) due to their potential for sub-60mV/decade sub-threshold swing. Such a reduced swing is a necessary requirement for ultra low power, ultra low voltage and high speed operation of next generation VLSI circuits. According to the scientific report-2010 of IMEC , TFET is the most promising device due to its strong similarity with the MOSFET configuration, which allows significant use of the existing MOSFET expertise in fabrication of VLSI chips using TFETs.

TFET can be a 3-terminal or a 4-terminal device built in silicon. The gate-controlled band to band tunneling is the working principle of this transistor [12] and its basic structure is a gated P-I-N diode. Compared to MOSFET, TFET has several advantages [12, 3]: i) suitable for low power applications due to lower leakage current, ii) better immunity to short channel effects, iii) subthreshold swing (SS) is not limited to 60mV/decade, iv) enhanced operating speed due totunneling, v) much smaller threshold voltage (VTH) roll-off, vi) low off current and vii) higher on/off current ratio. Thus TFET can be thought as a promising alternative to the MOSFET for low power and high-speed applications.

The Tunnel Field Effect Transistor (TFET) had been chosen before as the most promising device to respond to the demanding requirements of future technology nodes. Tunnel FET use electric field control of band to band tunnelling as the current gating mechanism [1,2]. The benefits of the TFET are especially linked to its potential for sub-60mV/decade sub-threshold swings [4], a pre-requisite for scaling the supply voltage well below 1V. Furthermore, the TFET has reduced short-channel effects compared to the MOSFET.

Tunnelling is a quantum mechanical phenomenon with no analog in classical physics. It occurs when an electron passes to a potential barrier without having energy to do. Tunneling is so great i.e., lower sub-threshold swing can allow lower operating voltages to be used [5]. It leads to chips that consume less power. Electrons tunnel from valence band to conduction band to conduction band where they readily transport to drain terminal. Holes on drain side will tunnel into valence band and transport into floating body. In scaling, TFET do not suffer from short channel effects. Power dissipation of TFETs can beat 60mV/dec sub-threshold swing of MOSFETs [4,9].

In most of the literature published so far, the experimentally shown ON-currents are unacceptably low for a technology that would like to replace the MOSFET. While OFF-currents are in the range of femtoamperes or microamperes, ON-currents for applied drain and gate voltages of 2 V are still limited to the nanoamperes range. Furthermore, in order to have a CMOS-compatible technology, voltages should be limited even more, to about 1.2 V [9].

## II. RELATED WORK

Over the last five decades, transistor scaling has driven the tremendous gains seen in the performance and power of integrated circuits.The scaling of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) are commonly used in high speed integrated circuits, yield smaller and faster more functions at lower cost. Various problems exist with scaling of MOSFET devices i.e. short channel effects(SCE), drain induced barrier lowering, velocity saturation which limits the performance of MOSFETs. Scaling limitations of MOSFET devices leads to lower ON to OFF current ratio limited by 60mV/dec sub threshold slope.

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A new type of device called "Tunnel FET" is used to overcome these difficulties. TFET can beat 60mV/dec sub-threshold swing of MOSFETs. In Tunnel FET the carrier are generated by band-to-band tunneling and OFF current is low. Tunnel FET have energy barrier in OFF state, which avoids application where leakage is concern of interest. In this Project sub-threshold swing and low OFF current is simulated and its power is analyzed.

Due to the technology scaling CMOS size is shrinking, performance is improved but new problems aroused that is short channel length effects which causes more leakage currents and hence more power dissipation. To avoid this problem researcher have found new device structure or technology which is Tunnel FET. They both are designed to overcome the short channel length effects of CMOS. And these devices are now becoming more advanced and better than CMOS.

1. To study the different characteristics of TFET.
2. Design TFET referring latest IEEE paper in HSPICE.
3. Optimize TFET for best performance in HSPICE.
4. Design different energy efficient circuit using CMOS, TFET and Optimized Tunnel-FET for 32nm technology in HSPICE.
   - Inverter.
   - Ripple Carry Adder.
   - Gates.
   - Full adder.
5. Compare different parameters of CMOS, TFET and Optimized Tunnel-FET to improve the performance of different energy efficient circuits.
6. To study the comparative characteristics of CMOS, TFET & Optimized TFET.

## III. OVERVIEW OF TFET

The simulated crosssection of a p-type TFET is shown in fig. 1. The channel widthand length of the device is taken as 60nm and 30nmrespectively. The device structure of TFET resembles that ofthe MOSFET with one exception. In the MOSFET, source anddrain are doped with the same type of dopants and the dopanttypes are opposite to that of substrate, while in a TFET, sourceand drain are of opposite doping types and the drain region hasa doping type same as that of substrate with highconcentration. According to structural configuration, TFET isa combination of several devices [19]: 1) the reversed P-I-Ndiode at the off state, 2) Esaki tunnel diode at the on state, 3)the MOS diode to form the inversion or accumulation layer when gate voltage is applied. In an NTFET, the substrate is lightly doped with n-type dopants.

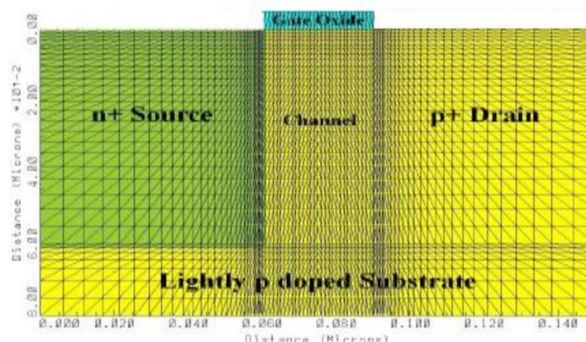


Figure1. Basic structure of PTFET

Source and drain are heavily doped p and n typeregions respectively. In case of PTFET, the substrate is lightly doped p-type while source and drain are heavily doped with ntype and p-type dopants respectively. The doping concentration of source and drain are about 1020 cm-3 and for substrate and channel, the doping concentration is 1015 cm-3 so that the channel behaviour is intrinsic. Channel doping concentration (NCH) is varied later to study the effect of channel concentration on device performance.

## IV. GATE VOLTAGE VS DRAIN CURRENT (IDS-VGS) CHARACTERISTICS:

The gate voltage-drain current (IDS–VGS) characteristics of theNTFET and PTFET are shown in fig. 3. In the case of NTFET,the drain current increases with increasing gate voltage. Ifnegative gate voltage is applied, the NTFET will show a weakPTFET behaviour.In case of PTFET, the drain current increases with decreasingthe gate voltage. The weak NTFET behaviour can also beobserved here when positive gate voltage is positive. It is clearfrom the fig. 3 that, for PTFETs, the current value is less whenpositive gate voltage is applied as compared to the currentvalues of NTFET when negative voltage is applied. This isdue the facts that the threshold voltage of PTFET is more thanthat of NTFET and large effective mass of carriers in thePFET which reduces the tunnelling probability.

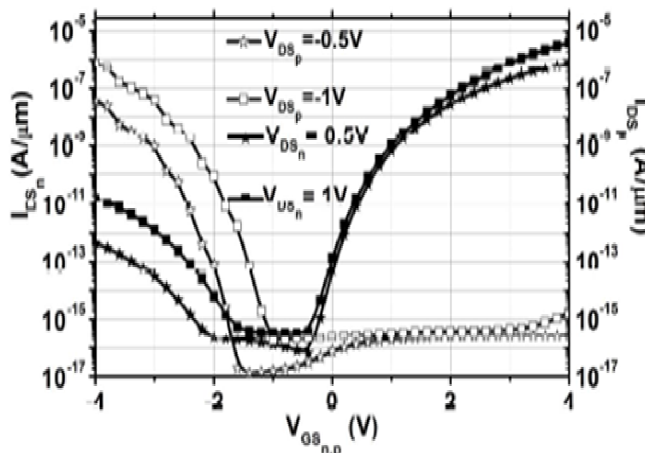


Figure 3. Ids- Vgs characteristicsof a 30nm NTFET and PTFET

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As already mentioned in the model calibration part, that using Energy Balance Transport for simulations does not bring a significant change in the device characteritics. In this context, Fig. 3(a) (inset) compares the current voltage characteristics obtained from DD and EBT model and they are found to be similar and in close proximity to each other and thus validates the choice of Drift Diffusion model. compares the TFET architectures for their Ids-Vgs chracteristics. The On current (ION) for a p-n-p-n architecture is enhanced in comparison to p-i-n due to a heavily doped n+ pocket region present at the source channel junction, which helps in improving the lateral electric field appearing at the tunneling junction and hence the drive current. It has been observed that the p-i-n and HG p-i-n stucture and similarly p-n-p-n and HG p-n-p-n structure have identical I ds-Vgs and Ids-Vds characteristics.

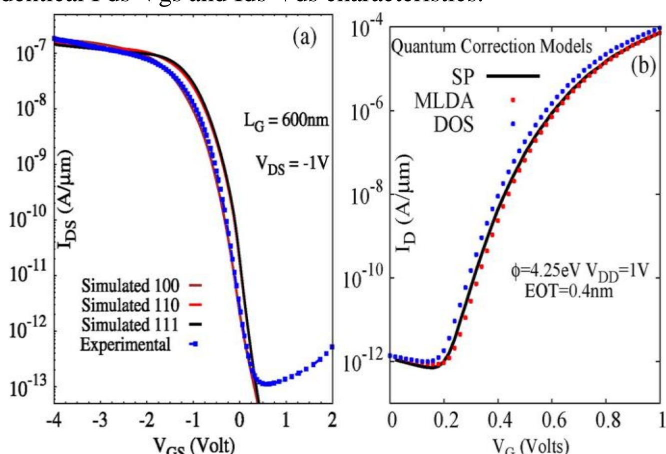



Figure 3(a) TFET transfer characteristics ($I_{DS}$ VS $V_{GS}$)

## V. OVERVIEW OF RCA

RippleCarryAdder (RCA) is a basicadder which works on basic addition principle. Thearchitecture of RCAis shown in Fig4.

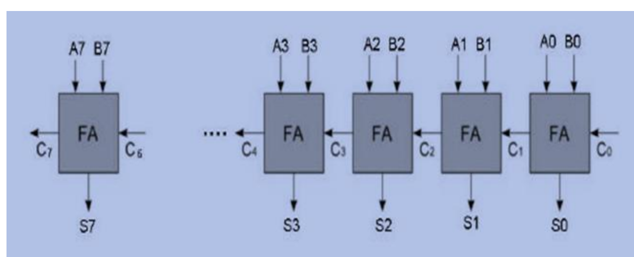



Fig.4 Block diagram of RCA

RCAcontainsseriesstructureofFullAdders(FA),eachFAisusedtoaddtwobitsalongwithcarrybit.Thecarrygenerated from eachfulladderisgivento nextfulladderandso on.Hence,thecarryispropagatedin a serialcomputation.Hence,delayismoreas thenumberofbitsisincreasedinRCA.
Assumeyou want to addtwo operands Aand B where

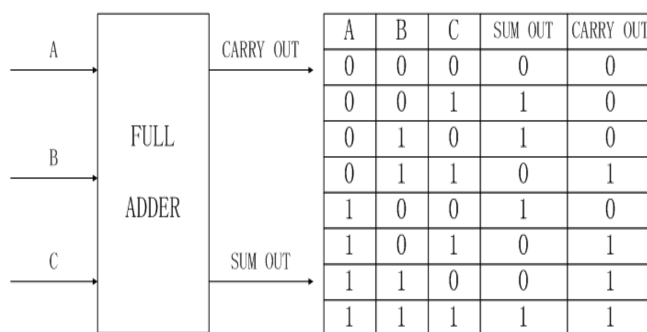
A=A3 A2 A1A0

B=B3 B2B1 B0

A+B=11 0 0 0 =$C_{out}S_3S_2S_1S_0$

From the example above it can be seen that we are adding 3 bits at a time sequentially until all bits are added. Afull adder is a combinational circuit that performs the arithmeticsum of threeinput bits:augends Ai, addend Bi andcarryin$C_{in}$ fromthe previous adder.Its results contain the sum Si and the carryout,$C_{out}$ tothenextstage.

So to design a 4-bit adder circuit we start by designing the 1–bit full adder then connecting the four 1-bit full adders to get the 4-bit adder as shown in the diagram above. Forthe 1-bitfulladder, thedesignbegins bydrawingthe Truth Tableforthethreeinputand the correspondingoutput SUM and CARRY.TheBoolean Expression describingthe binaryadder circuit is then deduced. The binaryfulladder is athreeinput combinational circuitwhich satisfies thetruth tablebelow.




| A | B | C | SUM OUT | CARRY OUT |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Fig.5 Diagram and Truth Table ofFullAdder

TheBoolean equations of a fulladder aregiven by:

$S_{out}$ =ABC +AB'C' +A'B'C +BA'C'

$S_{out}$ =A ⊕ B ⊕ C

$C_{out}$ =AB +AC +BC

$C_{out}$ =AB +C(A ⊕ B)

The circuitdiagram is shown in Fig.6.

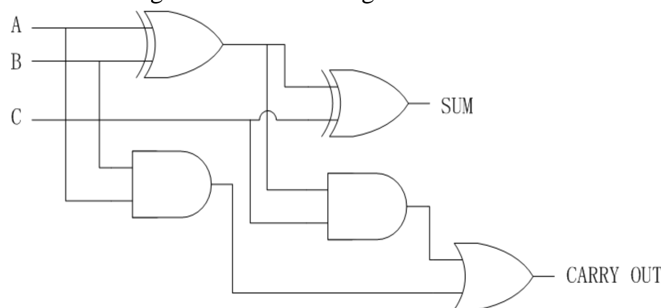



Fig. 6.TheGate level Diagram ofFullAdder

## VI. EXPERIMENTAL RESULTS

**NOT**

| VDD | Avgpwr | Peakpwr | PDP | EDP | tpdd |
|---|---|---|---|---|---|
| 0.2 | 5.32E-11 | 1.03E-08 | 9.15E-20 | 1.57E-28 | 1.72E-09 |
| 0.3 | 1.43E-10 | 2.33E-07 | 2.67E-20 | 5.00E-30 | 1.87E-10 |
| 0.4 | 3.33E-10 | 2.33E-06 | 9.40E-21 | 2.66E-31 | 2.83E-11 |
| 0.5 | 7.37E-10 | 8.97E-06 | 6.77E-21 | 6.23E-32 | 9.19E-12 |
| 0.6 | 1.58E-09 | 1.88E-05 | 8.48E-21 | 4.56E-32 | 5.37E-12 |
| 0.7 | 3.32E-09 | 2.91E-05 | 1.32E-20 | 5.26E-32 | 3.98E-12 |
| 0.8 | 6.94E-09 | 6.94E-09 | 2.24E-20 | 7.20E-32 | 3.22E-12 |
| 0.9 | 1.46E-08 | 4.17E-05 | 4.07E-20 | 1.14E-31 | 2.79E-12 |

**XOR**

| VDD | Avgpwr | Peakpwr | PDP | EDP | tpdd |
|---|---|---|---|---|---|
| 0.2 | 2.84E-10 | 2.09E-08 | 5.59E-18 | 1.10E-25 | 1.97E-08 |
| 0.3 | 7.49E-10 | 4.37E-07 | 2.08E-18 | 5.76E-27 | 2.77E-09 |
| 0.4 | 1.73E-09 | 4.96E-06 | 7.82E-19 | 3.53E-28 | 4.51E-10 |
| 0.5 | 3.81E-09 | 2.32E-05 | 4.28E-19 | 4.80E-29 | 1.12E-10 |
| 0.6 | 8.17E-09 | 5.34E-05 | 3.87E-19 | 1.83E-29 | 4.73E-11 |
| 0.7 | 1.73E-08 | 8.69E-05 | 4.97E-19 | 1.43E-29 | 2.87E-11 |
| 0.8 | 3.65E-08 | 1.20E-04 | 7.59E-19 | 1.58E-29 | 2.08E-11 |
| 0.9 | 7.75E-08 | 1.51E-04 | 1.29E-18 | 2.15E-29 | 1.67E-11 |

**AND**

| VDD | Avgpwr | Peakpwr | PDP | EDP | tpdd |
|---|---|---|---|---|---|
| 0.2 | 6.84E-11 | 5.22E-09 | 7.69E-19 | 8.66E-27 | 1.13E-08 |
| 0.3 | 1.78E-10 | 1.01E-07 | 2.84E-19 | 4.55E-28 | 1.60E-09 |
| 0.4 | 4.08E-10 | 7.59E-07 | 1.06E-19 | 2.77E-29 | 2.61E-10 |
| 0.5 | 8.86E-10 | 2.71E-06 | 5.78E-20 | 3.77E-30 | 6.52E-11 |
| 0.6 | 1.89E-09 | 6.51E-06 | 5.32E-20 | 1.50E-30 | 2.82E-11 |
| 0.7 | 3.95E-09 | 1.41E-05 | 6.90E-20 | 1.21E-30 | 1.75E-11 |
| 0.8 | 8.24E-09 | 2.21E-05 | 1.05E-19 | 1.34E-30 | 1.28E-11 |
| 0.9 | 1.73E-08 | 3.45E-05 | 1.78E-19 | 1.83E-30 | 1.03E-11 |

**OR**

| VDD | Avgpwr | Peakpwr | PDP | EDP | tpdd |
|---|---|---|---|---|---|
| 0.2 | 9.93E-11 | 1.62E-08 | 1.18E-18 | 1.40E-26 | 1.19E-08 |
| 0.3 | 2.63E-10 | 3.67E-07 | 4.66E-19 | 8.26E-28 | 1.77E-09 |
| 0.4 | 5.99E-10 | 3.73E-06 | 1.78E-19 | 5.26E-29 | 2.97E-10 |
| 0.5 | 1.28E-09 | 1.42E-05 | 9.41E-20 | 6.92E-30 | 7.35E-11 |
| 0.6 | 2.63E-09 | 2.81E-05 | 8.24E-20 | 2.58E-30 | 3.13E-11 |
| 0.7 | 5.35E-09 | 4.04E-05 | 1.00E-19 | 1.87E-30 | 1.87E-11 |
| 0.8 | 1.07E-08 | 5.12E-05 | 1.42E-19 | 1.89E-30 | 1.33E-11 |
| 0.9 | 2.13E-08 | 6.72E-05 | 2.22E-19 | 2.31E-30 | 1.04E-11 |

## VII. CONCLUSION

In this work performance of TFET is discussed. We propose and discussed the basic static operation, and studied by simulation the characteristics of tunnel FET as a better than 60mV/dec current switch. TFET has lower sub-threshold slop than MOSFET. Tunnel FET isapplicable for low power devices as it gives lower off current. It is difficult achieve high$I_{ON}$ degrading $I_{OFF}$ ,and sub-threshold slop below 60mV/dec.TFET is one of the promising device. The power of TFET is very low. The gate has been implementedusing TFET the observed in shows TFET is low power as compared to conventional MOSFET.

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