Minimum Component Based Sinusoidal Oscillator Using Single OTRA

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Abstract— In this paper a new Operational transresistance amplifier (OTRA) based sinusoidal oscillator is proposed. It uses two resistors, two capacitors and a single OTRA. Sensitivity analysis and non-ideality analysis behavior of OTRA on oscillator operation is also investigated. The proposed oscillator circuit is designed using PSPICE simulation and 0.18µm AGILENT CMOS process parameters. PSPICE simulation results agree well with the theoretical analysis of the proposed circuit.

Keywords- OTRA, sinusoidal oscillator, oscillator, analog circuit.

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I. INTRODUCTION

In electronic signal processing, control system and communication sinusoidal oscillators has gained attention. Using op-amp there are a verity of oscillators and these oscillators suffer from gain bandwidth product, limited slew rate [1]. In the literature there is also a verity of sinusoidal oscillators using current mode building blocks such as: Differential difference current conveyor (DDCC) [2-3], Current differencing buffered amplifier (CDBA) [4-6], operational transconductance amplifier (OTA) [7-11], second generation current conveyor (CCII) [12-14], current feedback operational amplifier (CFOA) [15-16], Four terminal floating nullator (FTFN) [17-18] etc. These oscillators suffer from large number of active and passive components.

In analog IC design OTRA has received considerable attention in last decade. It has high gain current input and voltage output. OTRA can be commercially available by the name NORTON amplifier but it has current input in one direction and it does not have ground in the input terminal. These can be eliminated by CMOS realization of OTRA [19-21]. There are various circuits which have been designed using OTRA [22-26].

This paper is organized as follows in section II fundamentals of OTRA and the proposed oscillator circuit is given, section II gives non-ideality analysis, sensitivity analysis w.r.t passive components are discussed in section III, simulation results using PSPICE are given in section IV. Finally conclusion is given in section V.

II. OTRA FUNDAMENTAL

Block diagram, equivalent circuit diagram and CMOS circuit diagram of OTRA are given in Fig.1, Fig.2 and Fig.3 respectively. It is a three terminal device with two input and one output terminal.
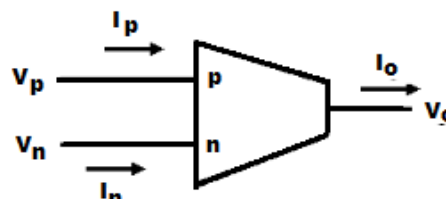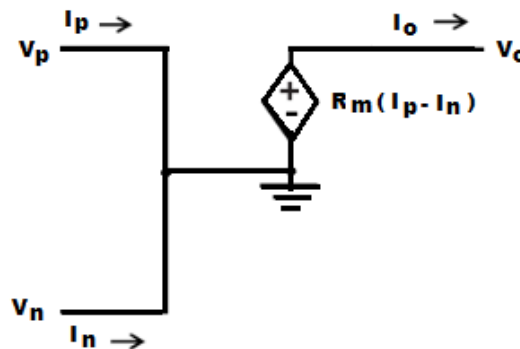

Fig.1:Block diagram of OTRA
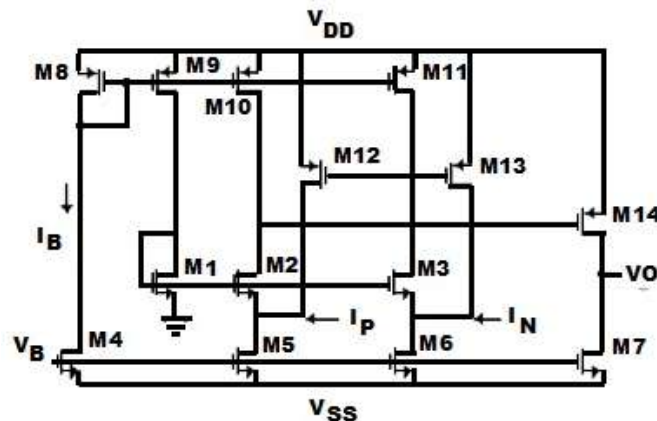

Fig.2:Equivalent circuit diagram of OTRA

Fig.3:CMOS circuit diagram of OTRA

Input and output relation of OTRA can be given by the following matrix:

$$\begin{bmatrix} V_p \\ V_n \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_P \\ I_n \\ I_o \end{bmatrix} \qquad (1)$$

$$V_p = V_n = 0 \qquad (2)$$

$$V_0 = R_m(I_p - I_n) \qquad (3)$$

III. PROPOSEDE OSCILLATOR CIRCUIT

The proposed sinusoidal oscillator circuit is shown in Fig.4. It uses one OTRA, two resistors and two capacitors. Routine analysis of the circuit gives the characteristics equation:

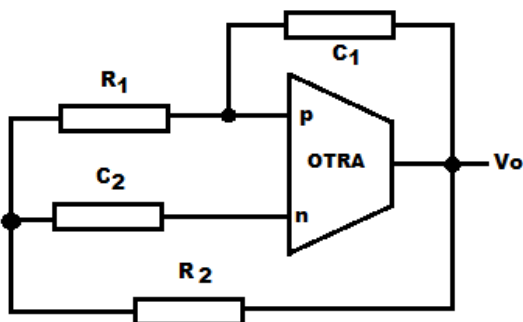$$s^2 c_1 c_2 + s[c_1(G_1 + G_2) - c_2 G_2] + G_1 G_2 = 0 \qquad (4)$$

Fig.4: Proposed oscillator circuit

From the characteristics equation the condition of oscillation and frequency of oscillation can be derived as

CO: $c_1(G_1 + G_2) = c_2 G_2$ $\qquad (5)$

FO: $f = \dfrac{1}{2\Pi} \sqrt{\dfrac{G_1 G_2}{c_1 c_2}}$ $\qquad (6)$

IV. NONIDEALITY & SENSITIVITY ANALYSIS

In ideally the transresistance gain (R_m) approaches to infinity but practically R_m has finite value and its effect is to be considered. In single pole model of OTRA the transresistance gain can be expressed as

$$R_m(s) = \dfrac{R_0}{1 + \dfrac{s}{\omega_0}} \qquad (7)$$

Where R_0 = DC transresistance gain. For high frequency the transresistance gain ($R_m(s)$) reduces to

$$R_m(s) = \dfrac{1}{s c_p} \qquad (8)$$

$$c_p = \dfrac{1}{R_0 \omega_0} \qquad (9)$$

The output of oscillator can be deviated from its ideal value due to non ideality of OTRA. Considering non-ideality the characteristics equation (4) changes to equation (10)

$$s^2 c_1 c_2 + s[c_1(G_1 + G_2) - c_2 G_2] + G_1 G_2 = 0 \qquad (10)$$

The modified condition of oscillation and frequency of oscillation are:

CO: $c_1(G_1 + G_2) = c_2 G_2$ $\qquad (11)$

FO: $f = \dfrac{1}{2\Pi} \sqrt{\dfrac{G_1 G_2}{c_1 c_2}}$ $\qquad (12)$

SENSITIVITY ANALYSIS:

In analog circuit sensitivity can be defined as small changes in the parameters of the circuit due to mathematical variation of performance characteristics. Sensitivity can be defined as

$$\left| s_x^f \right| = \dfrac{f}{x} \dfrac{\partial f}{\partial x} \qquad (13)$$

Where x= different circuit parameters

Sensitivity of f w.r.t C_1, C_2, R_1, R_2 are

$$\left| s_{C_1}^f \right| = \left| s_{C_2}^f \right| = \dfrac{1}{2} \qquad (14)$$

$$\left| s_{R_1}^f \right| = \left| s_{R_2}^f \right| = -\dfrac{1}{2} \qquad (15)$$

V. SIMULATION RESULTS

The proposed circuit is simulated in PSPICE design environment using CMOS based schematic of OTRA and 0.18µm MOSIS (AGILENT) process parameter. The supply voltage used here is ±1.5v. Simulation is performed by selecting R_1=10KΩ, R_2=1KΩ, C_1=100pf, C_2=1pf. The corresponding transient response and frequency spectrum are shown in Fig.5, Fig.6 and Fig.7 respectively. Theoretical oscillation frequency calculated as 15.92MHz and from simulation we obtained the practical frequency 15.27 MHz
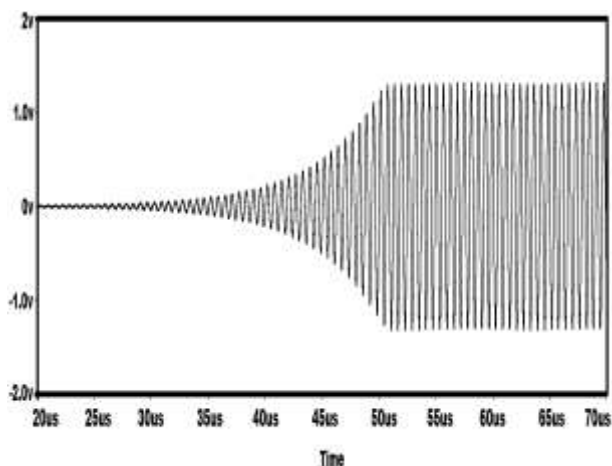
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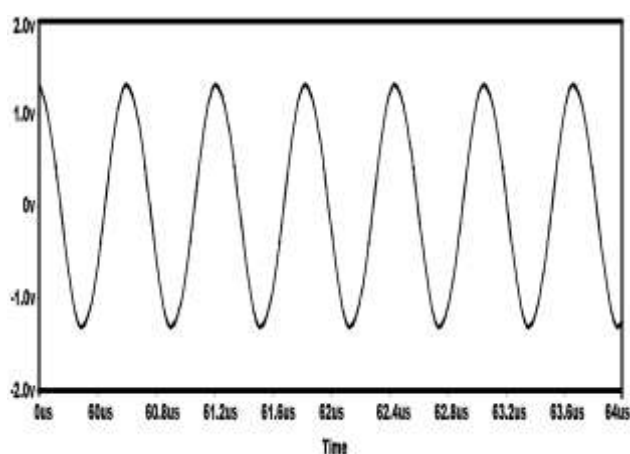Fig.5.Simulated output of oscillator

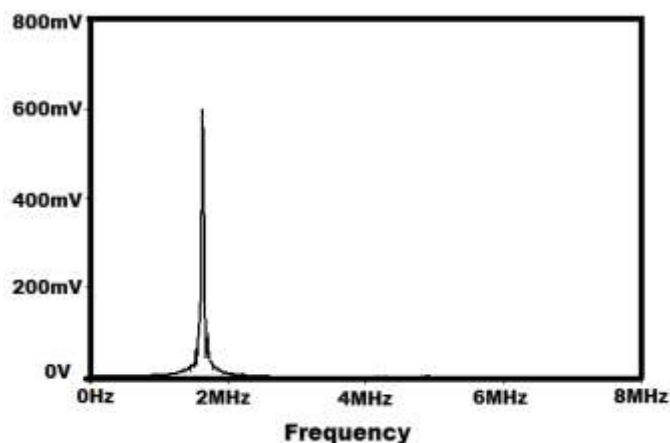Fig.6. Simulated output of oscillator

Fig.7.Frequency spectrum of oscillator

VI. CONCLUSION

In this paper a new sinusoidal oscillator using OTRA is presented. The proposed circuit uses only two resistors, two capacitors and a single OTRA. The proposed circuit posses a minimum number of passive components. The non-ideality analysis and sensitivity analysis are also carried out here. The

circuit is simulated using PSPICE software and 0.18μm MOSIS (AGILENT) process parameter.

REFERENCES

[1] A. Budak, Passive and Active Network Analysis and Synthesis (Houghton Mifflin, Boston, 1974).

[2] Chiu, W., Liu, S.l., Tsao, H. W. and Chen. J.J. "CMOS differential difference current conveyors and their applications", lEE Circ. Dev. & Syst, 1996, vol. 143, no. 2, pp. 91-96.

[3] Kumngern, M. and Dejhan, K. "DDCC-based quadrature oscillator with grounded capacitors and resistors", Active and Passi. Electron. Compon, 2009, vol. 2009, pp. 1-4.

[4] S. Qzcan, A Toker, C. Acar, H. Kuntman and O.Cicekoglu, "Single resistance-controlled sinusoidal oscillators employing current differencing buffered amplifier," Microelectronics Journal, 2000, vol.31, no.3, pp.169-174.

[5] J.W. Horng, "Current differencing buffered amplifiers based single resistance controlled quadrature oscillator employing grounded capacitors", IEICE Tran. on Fundamental of Electron., Communications and Computer Sciences , 2002, vol. E85-A, pp. 1416-1419.

[6] A Toker, S. OzoguZ, O. Cicekoglu, C. Acar, "Current-mode all-pass filters using current differencing buffered amplifier and a new high-Qband pass filter configuration," IEEE Trans.Circuits Syst. II, 2000, vol.47, no. 9, pp. 34-38.

[7] Singh. "Equivalent forms of dual-OTA RC oscillators with application to grounded-capacitor oscillators," lEE Proceedings-Circuits, Devices and Systems, 2006, voU53, no.2, pp.95-99.

[8] P. Prommee and K. Dejhan, "An integrable electronic-controlled quadrature sinusoidal oscillator using CMOS operational transconductance amplifier, " Int. J. ElectroniCS, 2002, vol. 89, pp. 365-379.

[9] Y. Tao, J. Kel Fidler, "Electronically tunable dual-OT A second-order sinusoidal oscillators/filters with Non-interacting controls: A systematic synthesis approach," IEEE Trans.Circuits Systems, 2000, vol. 47, no. 2, pp.117-129.

[10] Singh. "Equivalent forms of dual-OT A RC oscillators with application to grounded-capacitor oscillators", lEE Circ. Dev. & Syst, 2006, voU53, no.2, pp. 95-99.

[11] Y. Tao and J. Kel Fidler, "Electronically tunable dual-OTA secondorder sinusoidal oscillators/filters with non-interacting controls: A systematic synthesis approach", IEEE Trans. Circuits. Syst, 2000, vol. 47, no. 2, pp. 117-129.

[12] Srinivasulu, Avireni. "A novel current conveyor-based Schmitt trigger and its application as a relaxation oscillator", Int. J. Circuit TheolY Applic, 20 I 0, vo1.39, no. 6, pp. 679- 686.

[13] D. Pal, Avireni Srinivasulu, B. B. Pal, A Demosthenous and B. N. Das. "Current conveyor-based square/triangular waveform generators with improved linearity", IEEE Trans. Instrum. Meas, 2009, vol. 58, no.7, pp. 2174-2180.

[14] J. W. Horng, C. L. Hou, C. M. Chang, W. Y. Chung, H. W. Tang, and Y. H. Wen, "Quadrature oscillators using CClls," Int. J. of ElectroniCS, 2005, vol. 92, pp. 21-31.

[15] S. S. Gupta, R. K .. Sharma, D. R. Bhaskar and R. Senani "Sinusoidal oscillators with explicit current output employing current-feedback op-amps", Int. J. Circuit TheolY Applic, 2010, vol. 38, no. 2, pp. 131-147.

[16] D. R. Bhaskar, S. S. Gupta, R.Senani and A.K.Singh, "New CFOAbased sinusoidal oscillators retaining independent control of oscillation frequency even under the influence of parasitic impedances", Analog IntegI'. Circuits Signal Process, 2012, vol. 73, no. I, pp. 427-437.

[17] Abuelma'atti, M. T. and AI-Zaher, H. A. "Current-mode sinusoidal oscillators using single FTFN", IEEE Trans. Circuits Syst.-/J, 1999,vo1.46, no.l, pp. 69-74.

[18] S. I. Liu, "Single-resistance-controlled sinusoidal oscillator using two FTFNs", Electron. Lett, 1997, vol. 33, no. 14, pp. 1185-1186.

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[19] K. N. Salama, A M. Soliman, "CMOS operational transresistance amplifier for analog signal processing applications," Microelectronic Journal, 1999, vol. 30, no. 3, pp.235-245.

[20] Chen, J.J., Tsao, H.W., Liu, S.l. and Chiu, W. "Parasitic-capacitance insensitive current-mode filters using operational transresistance amplifiers", 2001, IEE Circ. Dev. & Syst, vo1.l42, no. 3, pp.186-192.

[21] J.J. Chen, H.W. Tsao, C.C. Chen, "Operational transresistance amplifier using CMOS technology," Electron. Lett., 1992, vol. 28, no. 22, pp.2087-2088.

[22] G. Ashish, S. Raj, D.R. Bhaskar, AK. Singh, "OTRA-based Grounded FDNR and Grounded- Inductance Simulators and Their Applications," Circuits Syst Signal Process, 2012, vol. 31, no. 2, pp.489-499.

[23] Y. K. Lo, and H. C. Chien, "Switch controllable OTRA based square/triangular waveform generator", IEEE Trans.Circuits Syst.- 11, 2007, vol. 54, no. 12, pp. 1110-1114.

[24] R. Pandey, N. Pandey, R. Mullick, S. Yadav and R. Anurag, "All Pass Network Based MSO Using OTRA". Advances in Electronics, 2015, vol. 2015, pp. 1-7.

[25] Ghosh, Mourina, and Sajal K. Paul. "Design of loss less grounded negative inductance simulator using single operational transresistance amplifier." Electrotechnique Et Energetique, 2014, vol. 59, no.4, pp. 381-390.

[26] A Gupta, R. Senani, D. R. Bhaskar, and A K. Singh, "New OTRABased Generalized Impedance Simulator " Ism Electronics, 2013, vol. 2013, pp.l-lO.

[27] M Bothra, R. Pandey, N. Pandey and S. K. Paul, "Operational TransResistance Amplifier Based Tunable Wave Active Filter" Radioengineering, 2013, vol. 22, no. I, pp.159-166.

[28] G. Kapur, S. Minai, C. M. Markana and V. P. Pyara, "Design of Fieldprogrammable Operational Transresistance Amplifier using Floatinggate MOSFETs " Microelectronics and Solid State Electronics, 2013, vol. 2, no.2, pp.1 1-23.