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# Design and Implementation of Optimized 32-Bit Reversible Arithmetic Logic Unit

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**Abstract***:* With the growing advent of VLSI technology, the device size is shrinking and the complexity of the circuit is increasing exponentially. Power dissipation is considered as one of the most important design parameter. Reversible logic is an emerging and promising technology that provides almost zero power dissipation. Power consumption is also considered as an important parameter in digital circuits. In this paper, an efficient fault tolerant 32-bit reversible arithmetic and logic unit is designed and implemented using some parity preserving gates. The proposed design is better in terms of quantum cost and power dissipation. The number of garbage outputs are reduced by using them as an arithmetic or logical operation. The design can perform three arithmetic operations: Adder, Subtractor, Multiplier and four logical operations: Transfer A, Transfer B, Bitwise AND, XOR operation. The results of the proposed design are then compared with the existing design.

***Keywords:*** *Reversible logic, ALU, Fault tolerant, Parity Preserving gates, Quantum cost, Garbage Outputs.*

*****

## I. INTRODUCTION

### *A. Principles of Reversible Logic*

The classical computational process which is irreversible, one bit of information is lost for each logical operation carried out by it. But in 1961, Rolf Landauer's principle states that for each bit of information lost K.T.ln2 Joules of energy is dissipated in the form of heat (where K is the Boltzmann's constant i.e. 1.38 × 10−23 J/K and T is the absolute temperature)[1]. However, this loss of energy is neglible for simple circuits and become significant for complex circuits. At room temperature T, the amount of heat dissipation is small (i.e. 2.9×10 -21 joule), but not negligible. In 1973, Bennet showed that there would be no energy dissipation if computations are done in the reversible way[2]. Resultantly, a new paradigm in circuit design evolved with the aim of reducing the entropy increase and energy dissipation[3]. Further, such a logical structure must possess the same number of inputs and outputs and a one-to-one mapping between the input and output states. Any device designed according to the above constraints is known as a reversible logic device[3].

Reversibility becomes an essential parameter for the future computer designs[4]. Reversible gates or circuits allow the reconstruction of the inputs from the observed outputs. Reversible logic is applicable to the research areas such as low power CMOS design, optical computing, quantum computing, bioinformatics, thermodynamic technology, DNA computing and nanotechnology[4]. A reversible circuit should be designed using minimum number of reversible logic gates.

### *B. Parameters of Reversible Logic*

There are many parameters for determining the complexity and performance of circuits in reversible logic circuit design. The following parameters should be reduced for the efficient reversible circuit design[5].

**Gate count (N)**: This refers to the number of reversible gates used in circuit.

**Constant inputs (CI):** The number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function[5].

**Garbage outputs (GO):** The number of unused outputs present in a reversible logic circuit. Garbage outputs can't be avoided as these are essential to achieve reversibility.

**Quantum cost (QC):** This refers to the cost of the circuit in terms of the cost of a primitive gate.

**Gate levels (GL):** The number of levels in the circuit which are required to realize the given logic functions[5].

## II. REVERSIBLE LOGIC GATES

### A. *Basic Reversible gates*

In classical irreversible gates, input states cannot be reconstructed from its outputs states[5]. Therefore, reversible gates are used in which input states can be reconstructed from the output states. The various reversible gates used in the proposed design are 3*3 Peres gate depicted in Fig. 1(a), 4*4 MHNG gate depicted in Fig. 1(b), 4*4 HNG2 gate depicted in Fig. 1(c).

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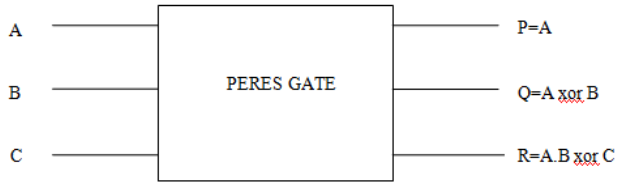


Fig 1(a): Peres gate

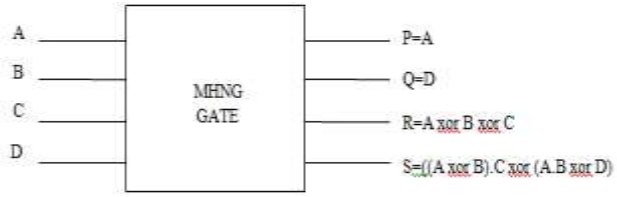


Fig 1(b): MHNG gate

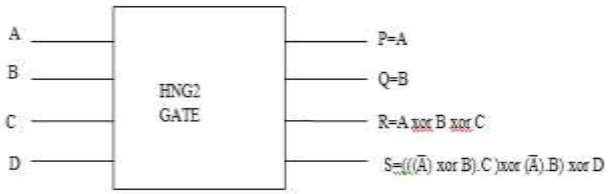


Fig 1(c): HNG2 gate

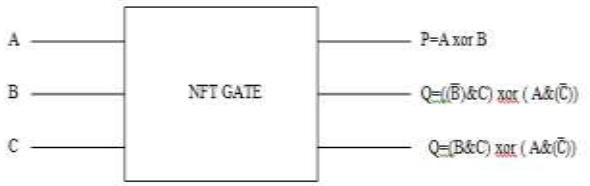


Fig 1(c): HNG2 gate

*B. Fault Tolerant and Parity Preserving Reversible Gates*

Fault tolerance is the property that allows a system to operate appropriately in the situation of failure of some of its components[5]. In fault tolerant systems, the detection and also correction of faults become easier and simple. Parity is used for fault tolerance in many systems. The basic fault tolerant gate is 3*3 NFT (New Fault Tolerant) gate depicted in Fig. 2(a). The various parity preserving gates used in the design are 3*3 F2G (Double Feynman Gate) gate depicted in Fig. 2(b) and IG (Islam Gate) gate depicted in Fig. 2(c).

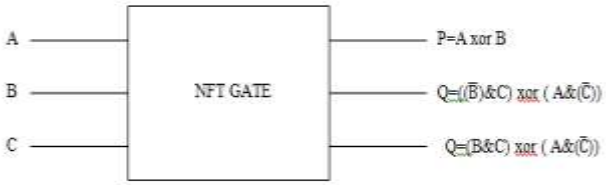


Fig 2(a): NFT gate

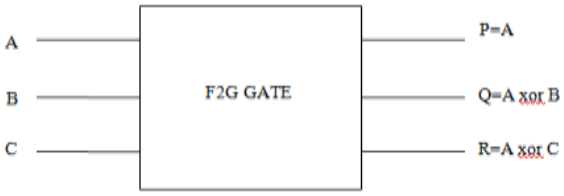


Fig 2(b): F2G gate

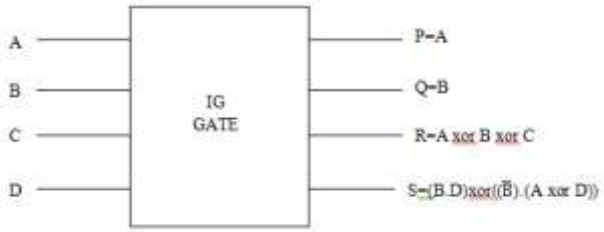


Fig 2(c): IG gate

Fig 2: Fault tolerant and Parity Preserving gates

## III. ARITHMETIC LOGIC UNIT PROPOSED DESIGN

ALU is a multi-operation, combinational logic digital function generator[6]. ALU is an integral part of any computing system and provides many arithmetic and logical operations such as addition, subtraction, multiplication, AND, XOR, TRANSFER of inputs etc. The proposed design of ALU performs 7 different arithmetic and logical operations. Depending upon the select lines, the ALU design selects the operation to be performed[7]. The selection procedure of the proposed ALU design is shown in Fig 3.

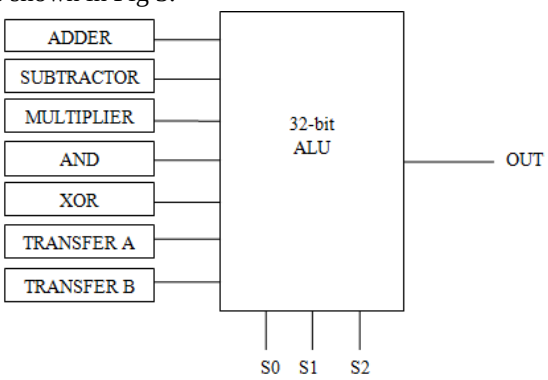


Fig 3: ALU design

| S0 | S1 | S3 | OPERATIONS PERFORMED |
|---|---|---|---|
| 0 | 0 | 0 | ADDER |
| 0 | 0 | 1 | SUBTRACTOR |
| 0 | 1 | 0 | MULTIPLIER |
| 0 | 1 | 1 | AND |
| 1 | 0 | 0 | XOR |
| 1 | 0 | 1 | TRANSFER A |
| 1 | 1 | 0 | TRANSFER B |

Table 1: OPERATIONS PERFORMED BASED ON THE CONTROL SIGNAL

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The ALU design inhibits the function generator property to process the input signals A and B under the control of control signals s0, s1 and s2[8]. The operations performed based on the control signals are shown in Table 1. Total seven arithmetic and logical operations are performed by the ALU.

*A. 32-BIT FULL ADDER*

The proposed ALU design consists of a 32-bit reversible full adder shown in Fig 4. The adder design consists of 32 MHNG (Modified HNG) gate. In each MHNG gate, first two bits carries the input bits, the third bit carries the initial carry and the last bit is maintained as zero i.e. constant input. The third and fourth output of the MHNG gate indicates the sum and output carry respectively and the second output is unused i.e. garbage output. The first output acts as the logical operation to transfer the first input vector A which reduces the garbage outputs of the proposed ALU design. The proposed adder is efficient in terms of quantum cost as compared to the existing design[7].

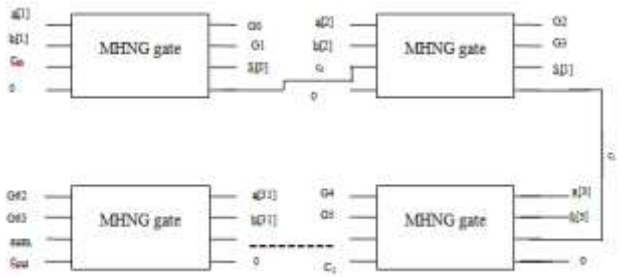


Fig 4. 32-bit Reversible Full Adder Design

*B. 32-BIT FULL SUBTRACTOR*

The proposed ALU design consists of a 32-bit reversible full subtractor shown in Fig 5. The subtractor design consists of 32 HNG2 gate. In each HNG2 gate, first two bits carries the input bits, the third bit carries the initial borrow and the last bit is maintained as zero i.e. constant input[7]. The third and fourth output of the HNG2 gate indicates the difference and output borrow respectively and the first output is unused i.e. garbage output. The second output acts as the logical operation to transfer the first input vector B which reduces the garbage outputs of the proposed ALU design.

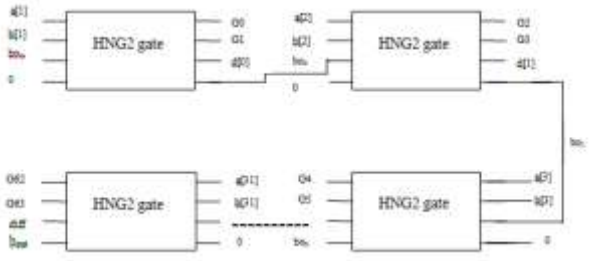


Fig 5. 32-bit Reversible Full Subtractor Design

*C. 32-BIT MULTIPLIER*

The 2-bit multiplier design is shown in Fig. 6 which comprises of 4 F2G gate, 4 Peres gate and 2 IG gate. By using this 2 bit multiplier, 4 bit multiplier is designed and further the 4 bit multiplier is used to design 8 bit multiplier and so on[7]. Thus a 32-bit multiplier is constructed using four 16 bit multipliers. The proposed multiplier design is better than the existing design in terms of quantum cost.

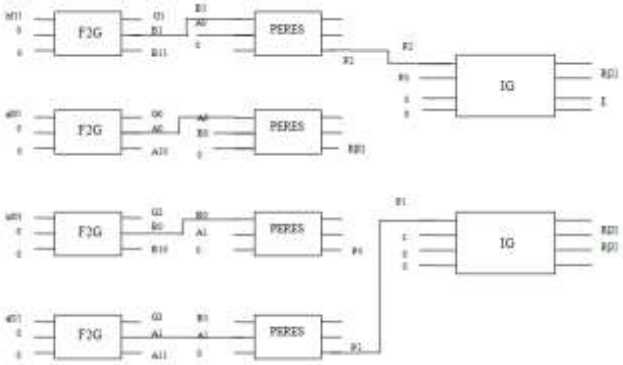


Fig 6. 2-bit Reversible Multiplier

*D. LOGICAL UNIT*

The proposed ALU performs four logical operations namely AND, XOR, TRANSFER A, TRA[ G2 ]. The 32-bit AND and XOR operations are performed using Peres gate and Transfer of input vectors are obtained by utilizing the garbage outputs of 32 bit full adder and full subtractor design. This will reduce the overall garbage outputs of the ALU design, thus, optimizing the design. The 32-bit AND and XOR operation design is shown in Fig.7.

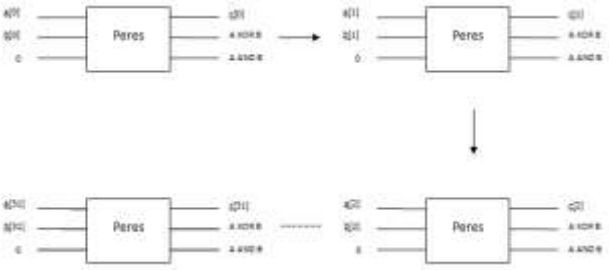


Fig 7. 32-bit AND and XOR design

## IV. SIMULATION AND SYNTHESIS RESULTS

The proposed 32-bit ALU design is simulated using MODELSIM ALTERA 6.4a version and synthesized using XILINX ISE SUITE 13.2 version. VERILOG HDL is used for simulation and synthesis purpose. The various results of the ALU design are shown in the figures below.

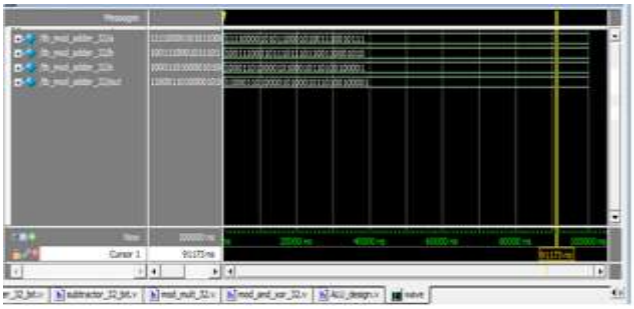

Fig 8(a). Simulation result of 32-bit Full Adder

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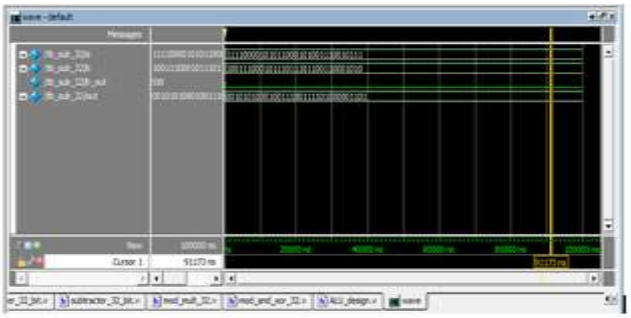

Fig 8(b). Simulation result of 32-bit Full Subtractor

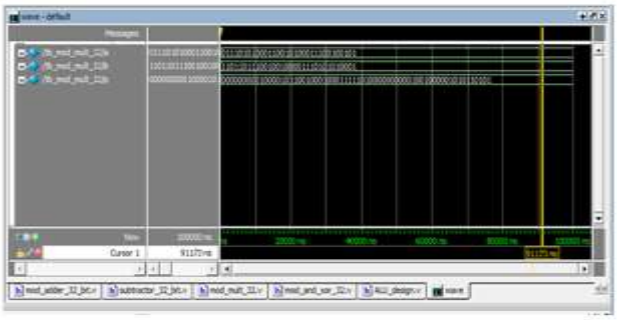

Fig 8(c). Simulation result of 32-bit Multiplier

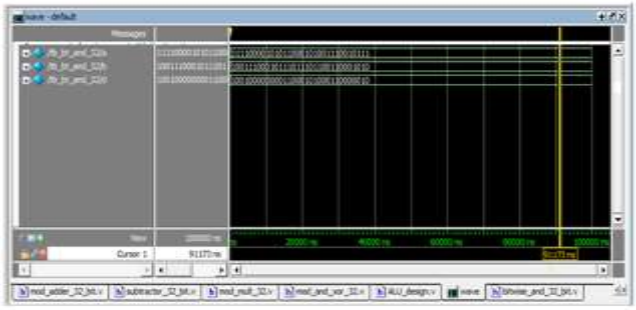

Fig 8(d). Simulation result of 32-bit AND operation

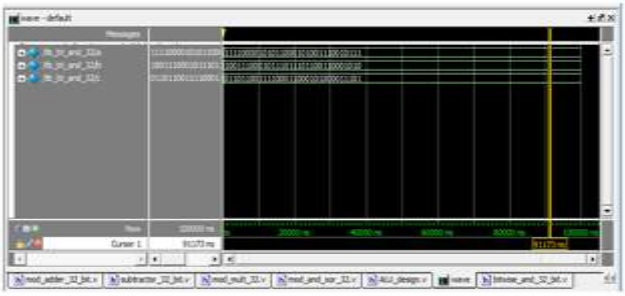

Fig 8(e). Simulation result of 32-bit XOR operation

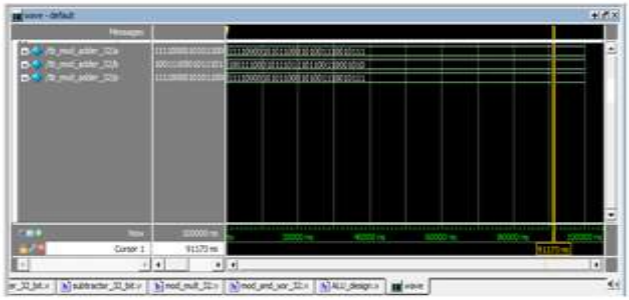

Fig 8(f). Simulation result of Transfer of A input vector

Fig 8(g). Simulation result of Transfer of B input vector

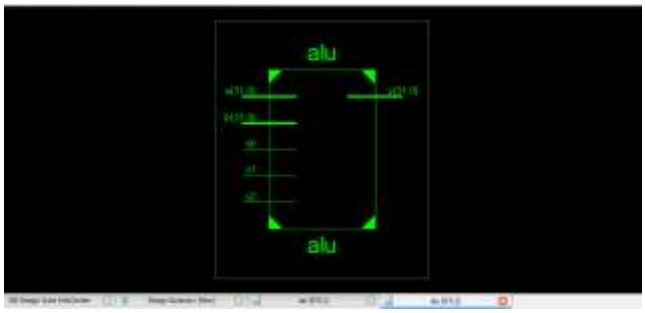


Fig 8(h). RTL1 schematic of ALU design

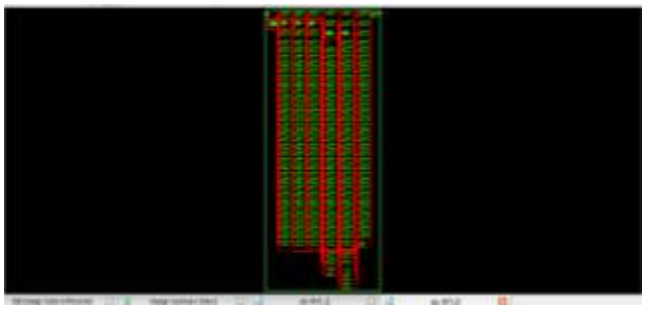

Fig 8(i). RTL2 schematic of ALU design

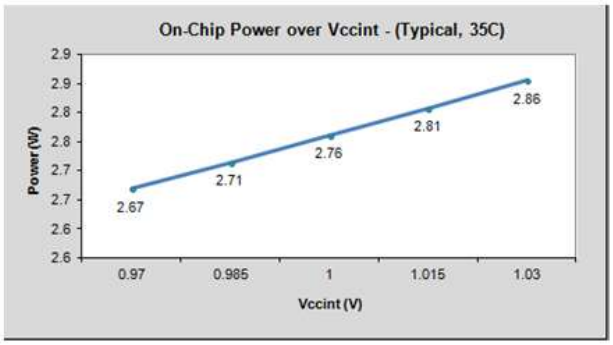


Fig 8(j). Graph showing power consumption of proposed ALU design

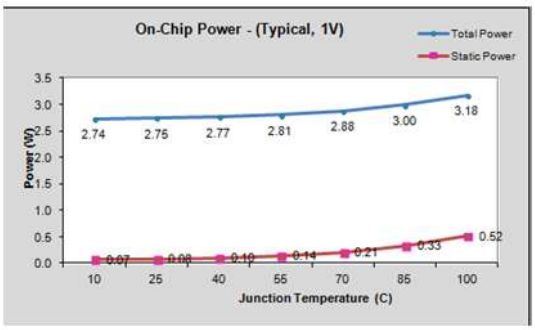


Fig 8(j). Graph showing power consumption of proposed design w.r.t. junction temperature

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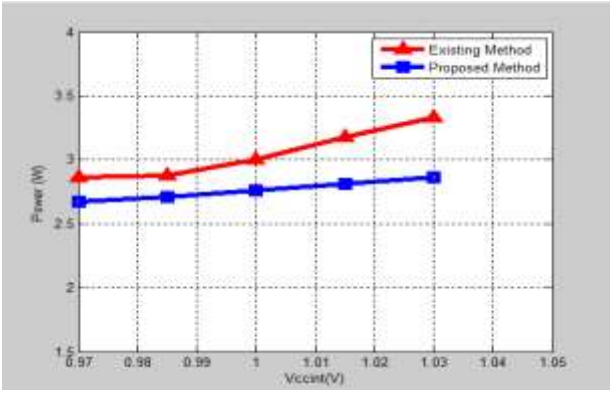


Fig 8(i). Graph showing comparison of power consumption of existing design[7] and proposed design

## V. COMPARISON

The proposed ALU design is compared with the existing design in terms of quantum cost, power consumption and number of garbage outputs. The comparison results are shown in table 2 below.

| PARAMETERS | PROPOSED WORK | EXISTING WORK |
|---|---|---|
| QUANTUM COST | 2672 | 2960 |
| POWER CONSUMPTION (WATTS) | 2.761 W | 3.329 W |
| GARBAGE OUTPUTS | 1328 | 1376 |

Table 2: Comparison results for proposed design and existing design[7]

## VI. CONCLUSION

The results of the existing ALU and the proposed ALU design are verified using Modelsim Simulator and synthesized using Xilinx ISE Design Suite 13.2. The power consumption is calculated using Xilinx Power Estimator(XPE)-2017.2. The proposed design is better in terms of Quantum cost and Power consumption when compared to other conventional ALU designs and can be used in Low power Applications. The size of the design is also improved. The proposed design is 32 bit in size as compared to the design given in [7] which is 16 bit in size.

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