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Modified Gating Techniques for Power and Speed Optimization in Arithmetic Circuits

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Abstract: As the threshold voltage is reduced due to voltage scaling in CMOS technology, it leads to increase in sub-threshold leakage current and hence static power dissipation. In this paper a power reduction technique named high speed drain gating is proposed to yield high speed, low power consumption and fast discharge. In these techniques two sleep transistors are employed, one to conserve leakage power and the other to reduce propagation delay. Simulations are performed using Tanner EDA tool in 90nm process technology. Comparative analysis of the present techniques is tabulated using 4x2 encoder and NAND gate.

Key Words: *leakage power, sleep mode, active mode, drain gating, power gating,Encoder.*

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I INTRODUCTION

As we move on to finer MOSFET technologies, transistor delay has decreased remarkably which helped in achieving higher performance in CMOS VLSI processors. With technology scaling, it is required to reduce the threshold and power supply voltages. As square of power supply voltage is directly proportional to dynamic power dissipation, to achieve less consumption of power, supply voltage has to be reduced. Static power and dynamic power are two main components of total power dissipation. Static power dissipation occurs due to continuously ON /OFF transistors when there is no change in input pattern. The components of static power dissipation are sub threshold leakage current, junction leakage current, gate oxide leakage current, gate induced drain leakage, pinch through leakage. Substantial increase has been observed in sub threshold leakage current with scaling of threshold voltage [1].

To counter the unwanted leakage in CMOS circuit, many techniques have been proposed over the years. Power gating [2] and stacking effect [3] are two well known techniques for reducing leakage power dissipation. Power gating normally makes use of sleep transistors that are connected either between the power supply and the pull-up network (PUN) or between the pull-down network (PDN) and ground. Sleep transistors are switched on when the circuit is evaluating and they are switched off in standby mode to conserve the leakage power in the logic circuit.Multi-threshold-CMOS (MTCMOS) [4] technique is also an effective way to achieve considerable decline in leakage power consumption. In MTCMOS technique, high *V*th sleep transistors are added in the circuit whereas PUN and PDN use low *V*th devices. In dual threshold circuits [5], low *V*th devices are used in the delay critical sections and high *V*th devices are used to reduce the leakage current in the circuitry. Stacking of transistor in series reduces the sub threshold leakage current when one transistor is in the off state. Stacking effect is used in sleepy stack technique [6] and force stack technique [7]. Sleepy stack technique provides better results than forced stack technique. In forced stack, an extra sleep an additional sleep transistor is connected in parallel with the transistor stack. This reduces the leakage current but at the same time delay in the circuit is increased. LECTOR and GALEOR are also two leakage tolerant techniques. LECTOR makes use of two leakage control transistors (LCTs) that are connected between the PUN and PDN. In the same time GALEOR technique makes use of gated leakage transistors (GLTs). Both LCTs and GLTs reduce leakage by increasing the resistance between supply voltage and ground.

Another efficient technique to overcome the leakage current problem is drain gating, and its variation and the modified circuits are proposed in detail in Section 2. The modified drain gating or the High Speed Drain Gating circuits are proposed in section 3. Simulation results taking NAND gate, 4x2decoder are enumerated in Section 4 and Section 5 provides the final conclusion.

II DRAIN GATING TECHNIQUES

In drain gating techniques, extra transistors are added in the between VDD and ground in four different configurations. Depending upon the position of the extra transistors these techniques are classified into four different methods. 1. Drain gating 2. Power gating 3. Drain-header and power-footer gating (DHPF) 4. Drain-footer and power-header gating (DFPH). The circuit topologies are shown in below figure. These techniques operate in two modes, active

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mode and sleep mode, During the active mode (high gate input in case of NMOS and low gate input for PMOS), these sleep transistors are turned ON, which results in a reduction of resistance of the conducting path from power supply to ground, thereby avoiding performance degradation. Alternatively, during the standby mode (low gate input for NMOS and high gate input for PMOS), the sleep transistors are turned off, resulting in an increase in resistance of the conducting path which results in a subsequent and desired reduction in the leakage current and thus the leakage power.In drain gating PMOS transistor with sleep input **(s)** is connected between PUN and output node, whereas NMOS transistor with sleep input **(S')** is inserted between the output node and PDN. In sleep mode s=1 and sbar=0 so that both sleep transistors are turned off to produce stacking effect which reduces leakage current by increasing resistance of the path from power supply to ground. During active mode, s=0 and sbar=1 both sleep transistors are turned on to reduce the resistance of the conducting paths from power supply to ground, thereby reducing performance degradation.

In power gating technique, PMOS sleep transistor with input **(S)** added between the power supply and the PUN, whereas NMOS sleep transistor with input **(S**bar**)** is added between the PDN and ground. As the name suggests, in DHPF, a PMOS sleep switch is inserted between PUN and output node and an NMOS sleep switch is inserted between the PDN and ground rail so called drain header power footer. In DFPH, an NMOS sleep switch between output node and PDN so called drain footer and a PMOS sleep switch between the power supply and the PUN hence power header.

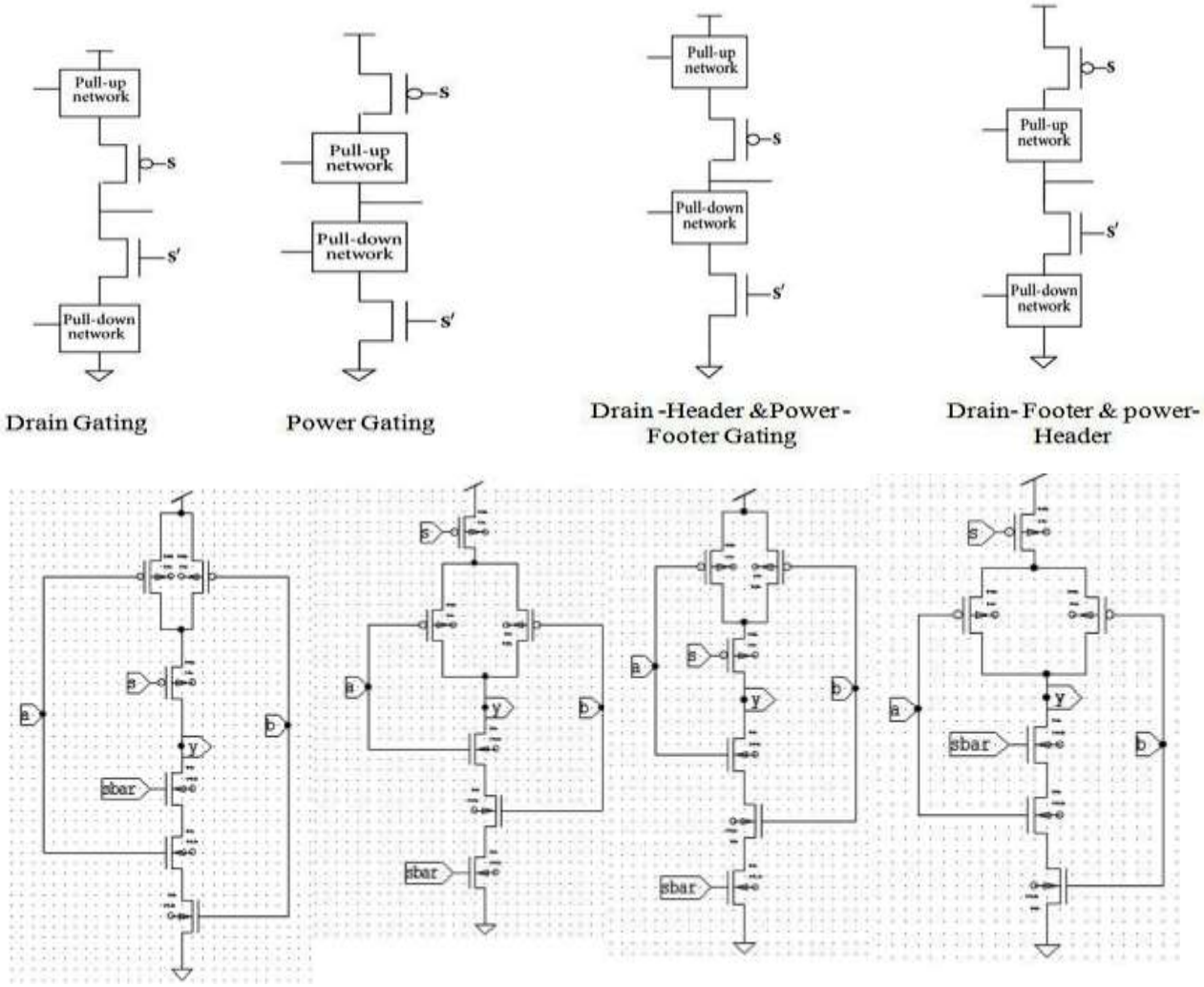

Fig: a) NAND using drain gating b) NAND using power gating c) NAND using DHPF d) NAND using DFPH

During active mode, s=0 and sbar=1 both sleep transistors are turned on and applying different combinations of inputs for a, b NAND logic will be satisfied. For eg. When a=0 and b=0 pmos 'a' will be ON (pmos 'b' is ON) and nmos 'b' will be OFF (nmos 'a' is OFF) and PDN is disconnected and output from the PUN is drawn to maximum value i.e. vdd. The function tabular forms of the above shown nand gates is given below for sleep mode and active mode.

2.1 Tabular form for nand gate using drain gating technique for SLEEP MODE

A	B	S	SBAR	T1	T2	T3	T4	T5	T6	Y
0	0	1	0	ON	ON	OFF	OFF	OFF	OFF	0
0	1	1	0	ON	OFF	OFF	OFF	OFF	ON	0
1	0	1	0	OFF	ON	OFF	OFF	ON	OFF	0
1	1	1	0	OFF	OFF	OFF	OFF	ON	ON	0

2.2 Tabular form for nand gate using drain gating technique for ACTIVE MODE

A	B	S	SBAR	T1	T2	T3	T4	T5	T6	Y
0	0	0	1	ON	ON	ON	ON	OFF	OFF	1
0	1	0	1	ON	OFF	ON	ON	OFF	ON	1
1	0	0	1	OFF	ON	ON	ON	ON	OFF	1
1	1	0	1	OFF	OFF	ON	ON	ON	ON	0

III THE PROPOSED HIGH SPEED(HS) GATING TECHNIQUES

In High Speed Drain Gating techniques an additional sleep transistor with sleep input (S) is connected at the output node parallel to the NMOS sleep transistor **(S**bar**)** and PDN. This added NMOS sleep transistor **(S)** provides an additional discharging path in the circuit and thus helps in speedy evaluation. Four different high speed circuit techniques are

1. High Speed drain gating
2. High Speed power gating
3. High Speed DHPF
4. High Speed DFPH

HS-gating circuits operate in two modes, namely standby mode and active mode. When the circuit is in active mode, sleep input **(S)** is in low state, and output node gets charged to power supply voltage. Both NMOS and PMOS sleep transistors connected between PUN and PDN are turned on and output is evaluated. In standby mode, sleep signal **(S** = 1, Sbar=0**)**,both PMOS and NMOS sleep transistors between PUN and PDN network turn off and additional NMOS sleep transistor is turned on, discharging the output node to ground thereby resulting in higher performance. A trade-off is achieved between power and delay so as to maintain high speed in the proposed circuits. The general topology of HS-gating techniques and their implementation using 4x2 encoder are shown below.

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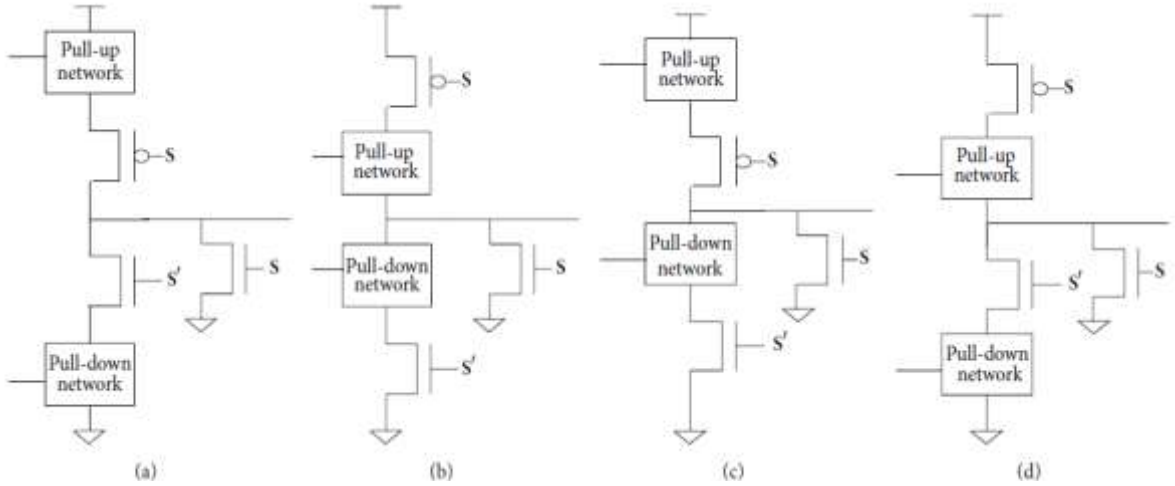

Fig: a) HS drain gating b) HS power gating c) HS- DHPF d) HS- DFPH

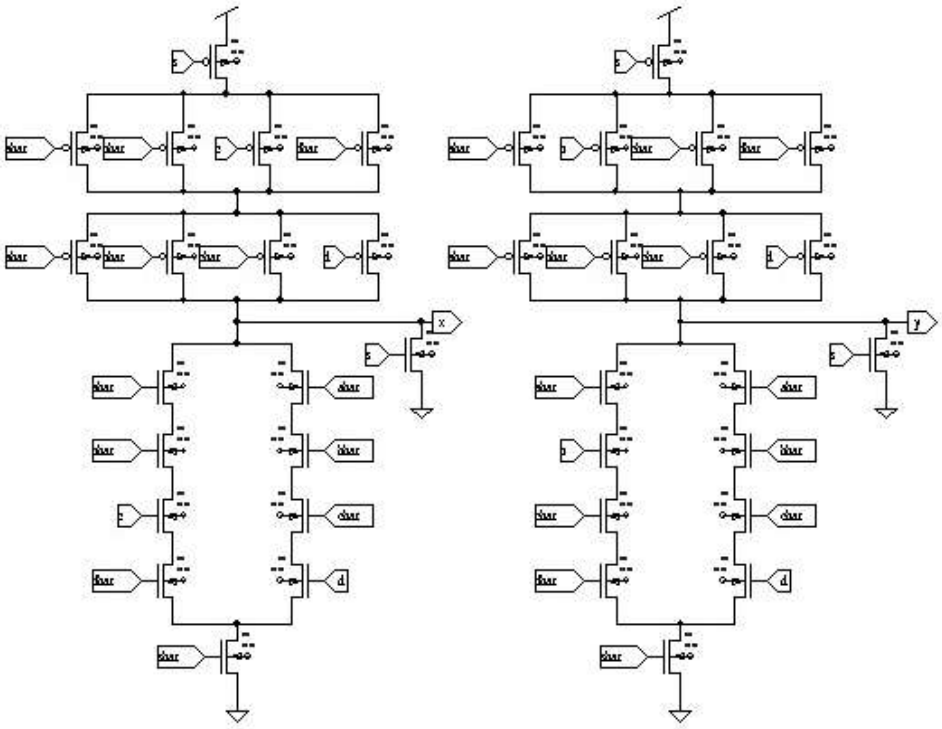

Fig: circuit diagram of 4x2 encoder using HS gating technique

IV SIMULATION AND RESULTS

The 2- input NAND gate and 4x2 Encoder are designed in all four different methods using Drain gating and HS- gating techniques. The circuits are simulated in Tanner EDA tool and the comparison table is shown below. In drain gating technique we observe delay is reduced but total power increases, in power gating technique power is reduced but delay increase. This is due to both the sleep transistors are placed either to drain terminals or at the power rails. In order to optimize both delay and power the sleep transistors are kept alternatively one at the drain region of PUN or PDN, and the other sleep transistor is placed at the power rails alternatively at VDD or GND. The HS-gating techniques further increase the speed of the circuit by providing a low resistive discharging path at the output node.

Table 4.1 Delay comparison between gating techniques and HS-gating techniques

	NAND			ENCODER		
CIRCUIT TECHNIQUES	**DYNAMIC POWER**	**RISE TIME**	**FALL TIME**	**DYNAMIC POWER**	**RISE TIME**	**FALL TIME**
DRAIN	2.37mw	910.68ps	819.61ps	4.04mw	637.48ps	910.68ps
POWER	348.22pw	1.27ns	1.09ns	1.52mw	1.27ns	1.09ns
DHPF	526.01uw	637.48ps	728.55ps	3.67mw	910.68ps	819.61ps
DFPH	783.17uw	728.55ps	637.48ps	2.01mw	726.73ps	688.48ps
HS-DRAIN GATING	2.56mw	273.2ps	318.74ps	4.63mw	364.27ps	182.14ps
HS-POWER GATING	1.08mw	409.81ps	455.34ps	859.17pw	910.68ps	728.55ps
HS-DHPF	2.34mw	272.3ps	227.67ps	2.9mw	621.23ps	546.41ps
HS-DFPH	2.32mw	273.2ps	227.67ps	759.45pw	728.55ps	546.41ps

4.2 Comparison Table of Static Power Dissipation for all Gating Techniques realized on NAND & Encoder

CIRCUIT TECHNIQUES	**NAND**		**ENCODER**	
	Static power dissipation for logic 0	**Static power dissipation for logic 1**	**Static power dissipation for logic 0**	**Static power dissipation for logic 1**
DRAIN	293.61pw	578.93pw	303.88pw	220.99uw
POWER	184.5pw	439.21 pw	239.23pw	734.86pw
DHPF	293.01pw	579.03pw	374.2pw	1.17nw
DFPH	184.76pw	439.21 pw	886.63pw	739.03pw
HS-DRAIN GATING	293.15pw	322.41pw	5.08nw	2.78mw
HS-POWER GATING	187.03pw	532.72 pw	1.22nw	748.14pw
HS-DHPF	293.15pw	727.05 pw	2.31nw	1.17nw
HS-DFPH	725.93pw	725.85 pw	1.49nw	2.03nw

V CONCLUSION

In this paper, the total power consumption and the propagation delay for certain circuits using the existing low power and performance enhancing techniques and the newly proposed ones are tabulated. Also a comparative study of these techniques for the parameters like dynamic power dissipation and propagation delay is made. Simulation results show that the proposed circuits work effectively with low propagation delay and even for different transistor configurations. From the above mentioned experimental data, we observe that, by implementing the high speed modified designs for the drain gating technique and its variants, it is able to enhance the performance of the design at lower power consumption.

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