International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169
Volume: 5 Issue: 7 486 – 489

Design of suitable Magnitude Comparator Architecture for Big Data Analytics

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***Abstract*—** In today's digital era increasing use of portable devices forces electronic designer to concentrate on high speed and low power dissipation. As magnitude comparator is very basic arithmetic unit, to cope up with high speed and optimum power for big data, we need suitable magnitude comparator architecture, so this Paper presents different types of magnitude comparator architecture such as serial, parallel and tree structure. Proposed 64 bit magnitude comparator is designed with 1.8v voltage supply using in standard CMOS 180nm Technology using Cadence Virtuoso EDA tool. Simulation of all three architecture have been done using SPECTRE VIRTUOSO ADE tool.

***Keywords*—** *GDI technique, Logic shut down technique, Tree architecture.*

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I. INTRODUCTION

In digital system magnitude comparator is very useful and basic arithmetic component. In almost all hardware sorter comparator plays vital role. Sorting network using comparator plays important role in parallel computing, multiprocessing and multi-access memories. It can be used as error detector in optimized equality-only comparator. Comparator compares two n-bit numbers to produce three outputs whether 1st umber is greater than, less than or equal to 2nd number as shown below

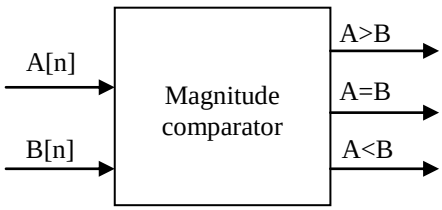

Fig.1. N-bit Magnitude comparator

To fulfill the demand of high speed and optimum power for big data we need suitable architecture. Logic style in logic gate and architecture mainly influences this characteristic, so

in this paper, GDI(Gate diffusion Input) technology based magnitude comparator is designed which provide optimum power, less propagation delay and less transistor count as compare to CMOS magnitude comparator.

This paper is organized in various parts. Part II presents the design of basic 4 bit magnitude comparator using GDI logic and power shut down technique [3]. Part III presents
Design of 64-bit magnitude comparator using serial, parallel and tree structure architecture. Part IV presents performance analysis and comparison of all these three structure.

II. 4-BIT MAGNITUDE COMPARATOR

A.Transistor level design:-

Logic style used to design gates in magnitude comparator is Gate Diffusion Input technique. With the help of GDI technique one can implement number of logic function using two transistors. With the help of this method we can design fast, low power dissipation circuits, as compared to CMOS and existing PTL techniques, while improving logic level swing and static Power characteristics [4]

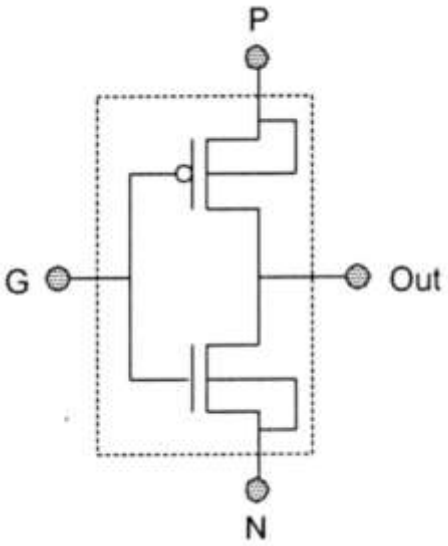

Fig. 2. GDI basic cell [4]

TABLE I.GDI Function [4]

N	*P*	*G*	*Out*	*Function*
1	*B*	*A*	*A+B*	*OR*
B	*0*	*A*	*AB*	*AND*
C	*B*	*A*	*A'B+AC*	*MUX*
0	*1*	*A*	*A'*	*NOT*

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All the gates XOR, AND and NOR in Fig 3 designed using GDI technique. This design is based on power shut down technique [3]

B. working of 4-bit comparator:

It consists three part as Logic shut down part, comparator part and Selection part.

In Logic shut down technique comparator first compare MSB bits of two inputs and whenever decision is made comparison logic for lower bits will be shut down to save power. Lower bits are compared only when decision can't be made from higher bits. In this way unnecessary comparison are avoided and power saving can be maximised [3].

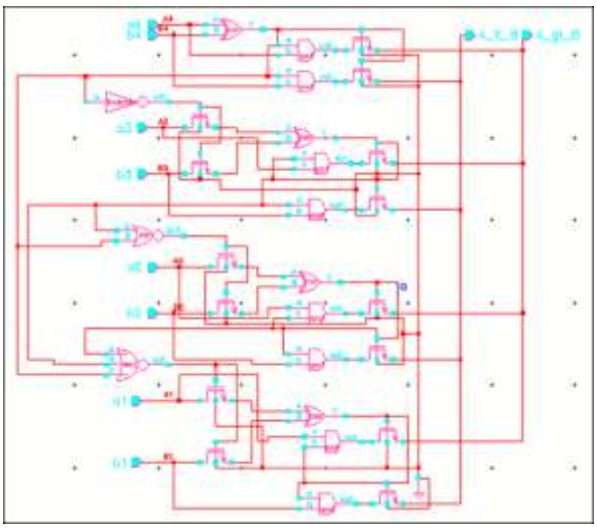

Fig. 3. 4-bit Magnitude comparator of Tree and Parallel architecture

In Fig.4 first MSB bits of two number is first compared, then cascading inputs (Ia_eq_b, Ia_gt_b and Ia_lt_b) are given to three AND gate along with result of MSB bit's comparison that is A_eq_b. Then result of respective AND gate is given to OR gate where 2nd inputs are A_lt_B and A_gt_B of MSB bits comparison. Now final result is given to cascaded input of 2nd comparator.

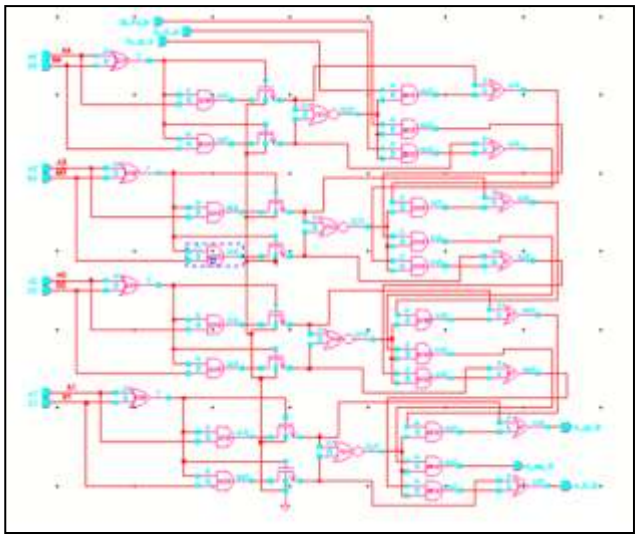

Fig. 4. 4-bit Magnitude comparator of series architecture

III. 64-BIT MAGNITUDE COMPARATOR

By using 4-bit magnitude comparator cell 64-bit magnitude comparator is designed using three architecture series, parallel and tree structure.

A. series architecture:

In serial architecture basic comparator module such as 4-bit magnitude comparator (Fig 4) are cascaded together, as shown in Fig.5, the outputs of the first comparator are connected to the cascade inputs of the second comparator and so on. The final result of the comparison appears on the three cascade outputs of the most significant 4-bit comparator.

For correct comparison, the cascade inputs of the first comparator should be connected as shown: "A<B" and "A>B" = logic 0. "A=B" = logic 1.

In series architecture first MSB bits of two inputs are compared then only lower bits are compared.

Fig. 5. 64-bit Magnitude comparator Serial Architecture

B. Parallel Architecture:

In this architecture all the bits are simultaneously compared thus reduces delay. But it requires more number of gates. 64-bit magnitude comparator parallel architecture is designed using 4-bit magnitude comparator shown in fig 3.

In parallel structure all 64 bits of two inputs is simultaneously applied to sixteen 4 bit magnitude comparator and then final result are carried out with the help of gates.

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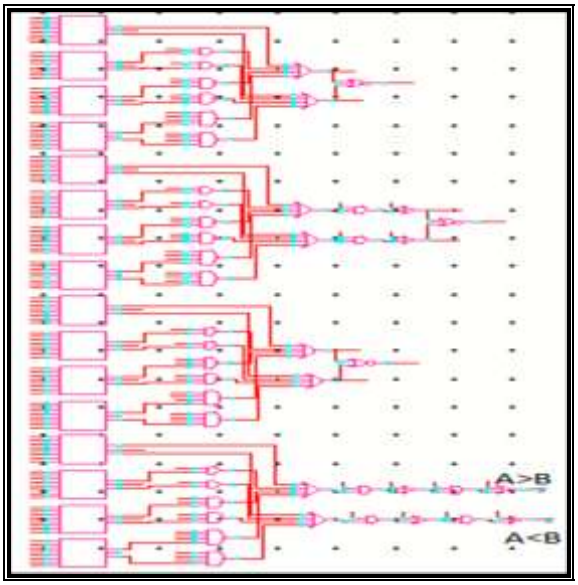

Fig. 6. 64-bit Magnitude comparator Parallel Architecture

C. Tree Architecture:

Tree architecture is type of parallel architecture, here instead of gates to compute final result, 1st result is given to comparator module in 2nd stage and thus delay reduces.

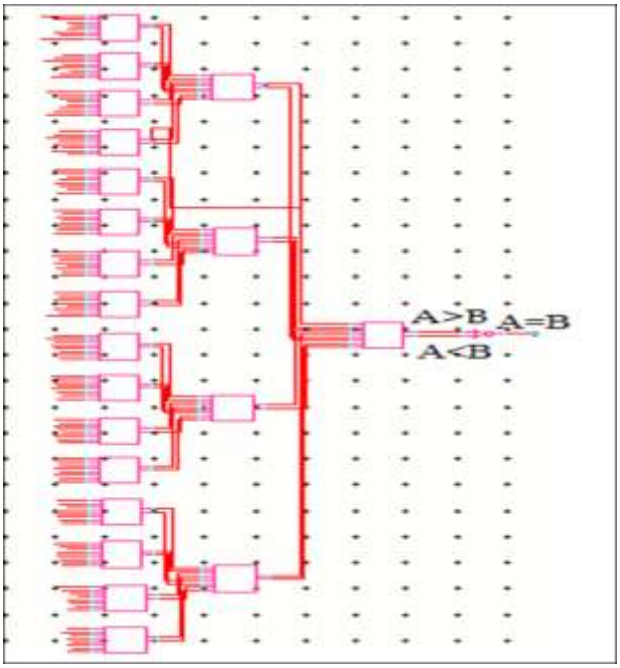

Fig. 7.64-bit Magnitude comparator Tree Architecture

IV. SIMULATION RESULTS AND PERFORMANCE ANALYSIS

All the three comparator architecture Series, Parallel and Tree structure and Anjuli's design [1] are compared in terms of delay, power and no. of Transistor, and result is tabulated in Table 2

In Series structure input A_{64} to A_1 and B_{63} to B_0 are given as pulse with pulse width 5ns and pulse period as 10ns, whereas for B_{64} pulse width is 5ns and pulse period is 15ns.all the inputs are having 1.8 v peak voltages.

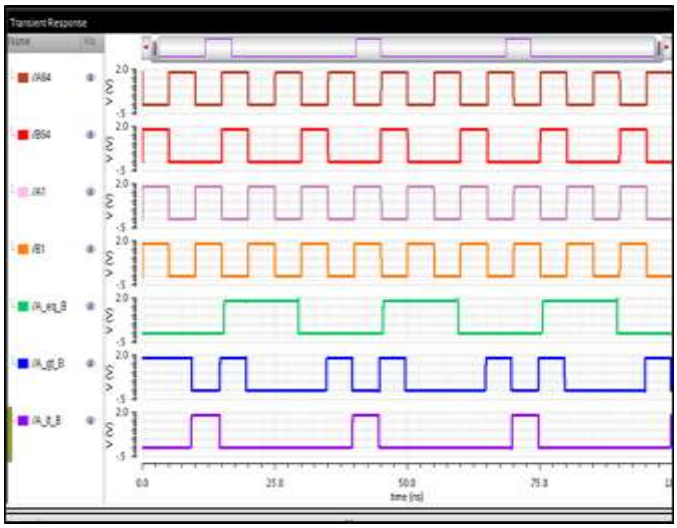

Fig.8. 64-bit Magnitude comparator Serial Architecture

In Parallel structure input A_{63} to A_1 and B_{64} to B_0 are given as pulse with pulse width 5ns and pulse period as 10ns, whereas for A_{64} same pulse of width 5ns and period 10ns is given as inverted. After simulating in virtuoso following waveform of 64-bit magnitude comparator using Parallel structure is observed.

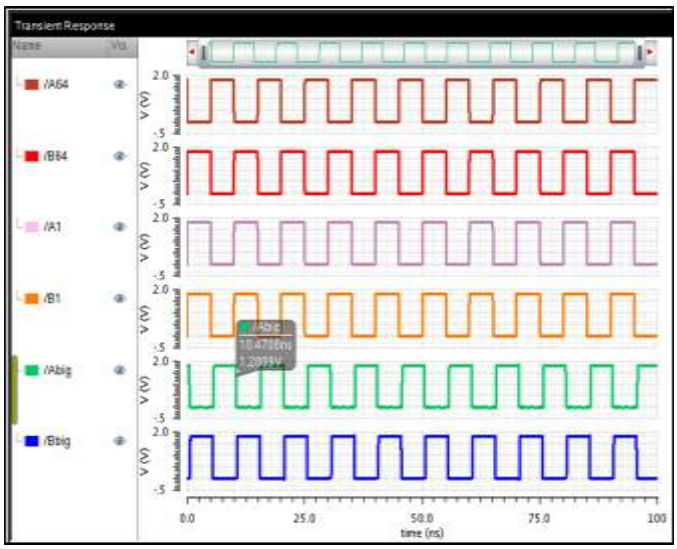

Fig. 9. 64-bit Magnitude comparator Parallel Architecture

In Tree structure input A_{63} to A_1 and B_{64} to B_0 are given as pulse with pulse width 5ns and pulse period as 10ns, whereas for A_{64} same pulse of width 5ns and period 15ns is given as inverted. After simulating in virtuoso following waveform of 64-bit magnitude comparator using tree structure is observed.

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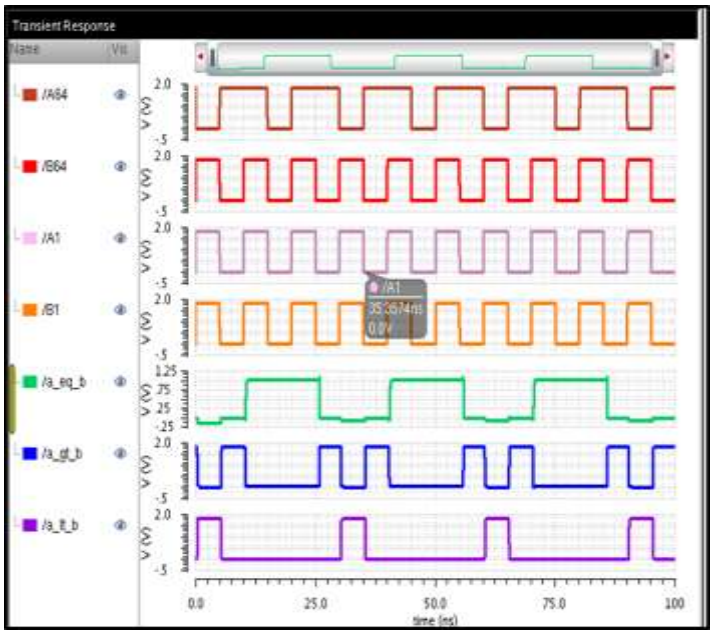

Fig. 10.64-bit Magnitude comparator Tree Architecture

TABLE 2.Performance Analysis

64 bit architecture	Delay (ns)		Avg.Power (mW)	No. of transistor
Serial Structure (180 nm)	A_gt_B	9.38	1.727	3328
	A_lt_B	9.28		
Parallel Structure (180 nm)	A_gt_B	0.55	0.418	2172
	A_lt_B	0.71		
Tree Structure (180 nm)	A_gt_B	0.39	0.439	1730
	A_lt_B	0.41		
Anjuli's design[1] (90 nm)	A_eq_B	0.59	0.008	1236
	A_lt_B	4.24		

CONCLUSION

64-bit magnitude comparator Tree structure architecture is faster with delay is 0.39ns for A_gt_B and 0.41ns for A_lt_B. Power dissipation observed is 0.456mW. Logic style GDI helps to reduce transistor count. In 64 – bit magnitude comparator design using Tree structure there is a decrease in power consumption and delay so 64 – bit magnitude comparator design using Tree structure is used for the better performance applications.

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