Simulation of Five Level Diode Clamped Multilevel Inverter

P.Anil Kumar[*1] K.Kartheek[2] B.Madhukar[3]
Assistant Professor[*1,2,3]
Matrusri Engineering College[*1,2,3], Saidabad
Hyderabad
e-mail: anilkumar.palarapu@gmail.com, kkartheek19@gmail.com, madhukarouce@gmail.com

Abstract—The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as inverter. The voltage source inverters produce an output voltage or a current with levels either 0 or +ve or-ve V dc. They are known as two-level inverters. Multilevel inverter is to synthesize a near sinusoidal voltage from several levels of dc voltages. Multilevel inverter has advantage like minimum harmonic distortion. Multi-level inverters are emerging as the new breed of power converter options for high power applications. They typically synthesize the stair-case voltage waveform (from several dc sources) which has reduced harmonic content. Multi-level inverters have many attractive features, high voltage capability, reduced common mode voltages near sinusoidal outputs, low dv/dt, and smaller or even no output filter; sometimes no transformer is required at the input side, called the transformer-less solution, making them suitable for high power applications

In this paper a 5-level Diode clamped multilevel inverter is developed by IGBTS using Simulink. Gating signals for these IGBTS have been generated by designing comparators. In order to maintain the different voltage levels at appropriate intervals, the conduction time intervals of IGBT have been maintained by controlling the pulse width of gating pulses[6] (by varying the reference signals magnitude of the comparator). The simulation results for 5-level and THD for the output have been identified by MATLAB/SIMULINK.

Keywords-MLI, THD,SPWM,PD,POD,APOD

*****

I. INTRODUCTION

Multilevel Inverters (MLI) include an array of power semiconductor devices and capacitor voltage sources, the output of which generates stepped voltage waveforms. The commutation of switches permits the addition of voltages, which results as high voltage at output, while the power semiconductor must withstand only reduced voltages. However, as the number of levels increases, the control complexity increases.

There are several SPWM Techniques such as (i) In Phase Disposition PWM (IPDPWM); (ii) Phase Opposition Disposition PWM (PODPWM); (iii) Alternate Phase Opposition Disposition PWM (APODPWM); (iv) Alternate Phase Opposition Disposition and Alternate Phase Shift PWM (APODAPSPWM); (v) Phase Shift PWM (PSPWM); (vi) Alternate Phase Shift PWM (APSPWM), (vii) Carrier Overlap PWM (COPWM); (viii) Variable Frequency PWM (VFPWM); and (ix) Alternate Variable Frequency PWM (AVFPWM)

In this Paper, five-level MLI SIMULINK model is designed using MATLAB software. The first four 'phase disposition' methods are considered.

II. MULTILEVEL INVERTER

By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion [7]. However, a high number of levels increases the control complexity and introduces voltage imbalance problems. Fig 2.1 represents a one leg model of multilevel inverter. In this schematic diagram operations of semiconductors are shown by an ideal switches with several states [7].

An inverter is a device that converts dc input power to ac output power at desired output of voltage and frequency.

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM)[7]. The attractive features of a multilevel converter can be briefly summarized as follows.

Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced[7].

- Common-mode (CM) voltage: Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies such as that proposed in.
- Input current: Multilevel converters can draw input current with low distortion.
- Switching frequency: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

The three different major multilevel converter structures have been reported in the literature:

•Cascaded H-bridges converter with separate dc sources,
•Diode clamped (neutral-clamped), and
•Flying capacitors (capacitor clamped).

Moreover, abundant modulation techniques and control paradigms have been developed for multilevel converters such as

•Sinusoidal pulse width modulation (SPWM),
•Selective harmonic elimination (SHE-PWM),
•Space vector modulation (SVM)

III. DIODE CLAMPED MULTI LEVEL INVERTER

The main concept of this inverter is to use diodes and provides the multiple voltage levels through the different phases to the capacitor banks which are in series. A diode transfers a limited amount of voltage, thereby reducing the stress on other electrical devices[7]. The maximum output voltage is half of the input DC voltage. It is the main drawback of the diode clamped multilevel inverter. This problem can be solved by increasing the switches, diodes, capacitors. Due to the capacitor balancing issues, these are limited to the three levels[7]. This type of inverters provides the high efficiency because the fundamental frequency used for all the switching devices and it is a simple method of the back to back power transfer systems.

EX: 5 level diode clamped multilevel inverter,9 level diode clamped multilevel inverter

The 5 level diode clamped multilevel inverter uses switches, diodes. a single capacitor is used ,so output voltage is half of the input dc[7]

The 9 level diode clamped multilevel inverter uses switches, diodes; capacitors are two times more than the 5-level diode clamped inverters [7]. So out put more than the input

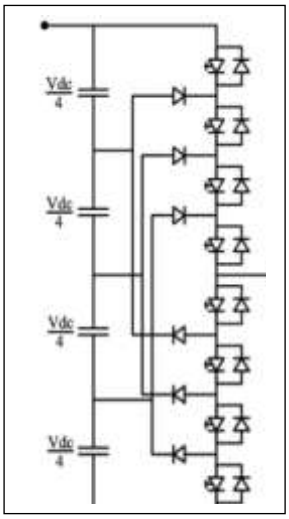

Fig 1:five level one Leg circuit of diode clamped MLI

IV. PULSE WIDTH MODULATION TECHNIQUES

A. *PWM Strategies With Differing Phase Relationships*

This section extends the principles of carrier-based PWM that are used for multilevel inverter. One of the most straightforward methods of describing voltage-source modulation is to illustrate the intersection of a modulating signal (duty cycle) with triangle waveforms. There are three alternative PWM strategies with differing phase relationships:

• Alternate phase disposition (APOD) – every carrier waveform is in out of phase with its neighbor carrier by 180.

• Phase opposition disposition (POD) – All carrier waveforms above zero reference are in phase and are 180 degree out of phase with those below zero.

• Phase disposition (PD)- All carrier waveforms are in phase

B. ***Alternate Phase Disposition (APOD):***

In case of alternate phase disposition (APOD) modulation, every carrier waveform is in out of phase with its neighbor carrier by 180 degree. Since APOD and POD schemes in case of three level inverter are the same, a five level inverter is considered to discuss about the APOD scheme.

The rules for APOD method, when the number of level N = 5, are

- The N – 1 = 4 carrier waveforms are arranged so that every carrier waveform is in out of phase with its neighbor carrier by 180.
- The converter switches to + Vdc/2 when the reference is greater than all the carrier waveforms.
- The converter switches to Vdc/4 when the reference is less than the uppermost carrier waveform and greater than all other carriers.
- The converter switches to 0 when the reference is less than the two uppermost carrier waveform and greater than two lowermost carriers.
- The converter switches to -Vdc/4 when the reference is greater than the lowermost carrier waveform and lesser than all other carriers.

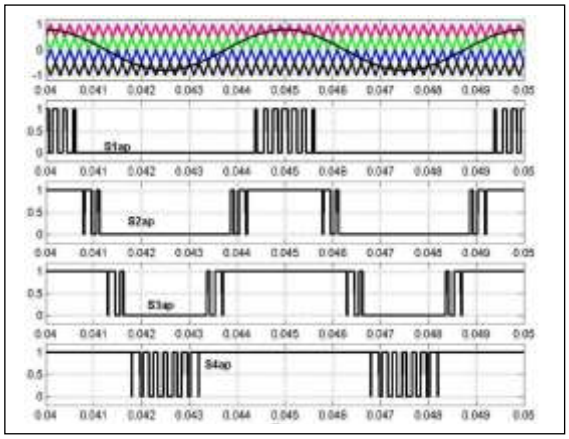

Fig 2:Switching pattern produced using the APOD carrier-based PWM scheme for a five-level inverter

I. Modulation signal and carrier waveforms

II. Phase “a” output voltage.

Above figure2 demonstrates the APOD scheme for a five-level inverter. The figure displays the switching pattern generated by the comparison of the modulation signals with the four carrier waveforms. Figure 2 Shows the output voltage waveform of phase "a" and it is clear the waveform has five steps.

C. *Phase Opposition Disposition (POD):*

For phase opposition disposition (POD) modulation all carrier waveforms above zero reference are in phase and are 1800 out of phase with those below zero. The rules for the phase opposition disposition method, when the number of level N = 3 are The N –1 = 2 carrier waveforms are arranged so that all carrier waveforms above zero are in phase and are 1800 out of phase with those below zero.

•The converter is switched to + Vdc / 2 when the reference is greater than both carrier waveforms.

•The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.

•The converter is switched to - Vdc / 2 when the reference is less than both carrier waveforms.

As seen from Figure, the figure illustrates the switching functions produced by POD carrier based PWM scheme. In the PWM scheme there are two triangles, upper triangle magnitude from 1 to 0 and the lower triangle from 0 to –1 and these two triangle waveforms are in out of phase. When the modulation signal is greater than both the carrier waveforms, S1ap and S2ap are turned on and the converter switches to positive node voltage and when the reference is less than the upper carrier waveform but greater than the lower carrier, S2ap and S1an are turned on and the converter switches to neutral point. When the reference is lower than both carrier waveforms, S1an and S2an are turned on and the converter switches to negative node voltage.

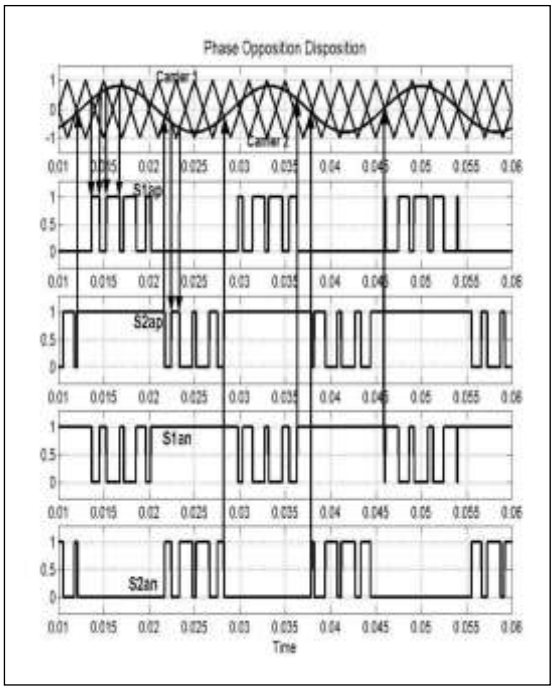

Fig: 3 Switching pattern produced using the POD carrier-based PWM scheme: (a) two triangles and the modulation signal (b) S1ap (c) S2ap (d) S1an (e)S2an

D. *Phase Disposition (PD):*

In the present work, in the carrier-based implementation the phase disposition PWM scheme is used.

Figure demonstrates the sine-triangle method for a three-level inverter. Therein, the a-phase modulation signal is compared with two (n-1 in general) triangle waveforms. The rules for the phase disposition method, when the number of level N = 3, are

• The N –1 = 2 carrier waveforms are arranged so that every carrier is in phase.

• The converter is switched to + Vdc / 2 when the reference is greater than both carrier waveforms.

• The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.

• The converter is switched to - Vdc / 2 when the reference is less than both carrier waveforms.

As seen from Figure, the figure illustrates the switching pattern produced by the carrier-based PWM scheme. In the PWM scheme there are two triangles, the upper triangle ranges from 1 to 0 and the lower triangle ranges from 0 to –1. In the similar way for an N –level inverter, the (N-1) triangles are used and each has a peak-to-peak value of 2/(N-1). Hence the upper most triangle magnitude varies from 1 to (1-2/(N-1)), second carrier waveform from (1-4/(N-1)), and the bottom most triangle varies from (2-2/(N-1)) to –1.

In Figure, the switching pattern of each device can be seen. It is clear from the figure that during the positive cycle of the modulation signal, when the modulation is greater than Triangle 1 and Triangle 2, then S1ap and S2ap are turned on and also during the positive cycle S2ap is completely turned on. When S1ap and S2ap are turned on the converter switches to the + Vdc / 2 and when S1an and S2ap are on, the converter switches to zero and hence during the positive cycle S2ap is completely turned on and S1ap and S1an will be turning on and off and hence the converter switches from + Vdc / 2 to 0. During the negative half cycle of the modulation signal the converter switches from 0 to -Vdc / 2. Thephase voltage equations for star-connected, balanced three-phase loads expressed in terms of the existence functions and input nodal voltage.

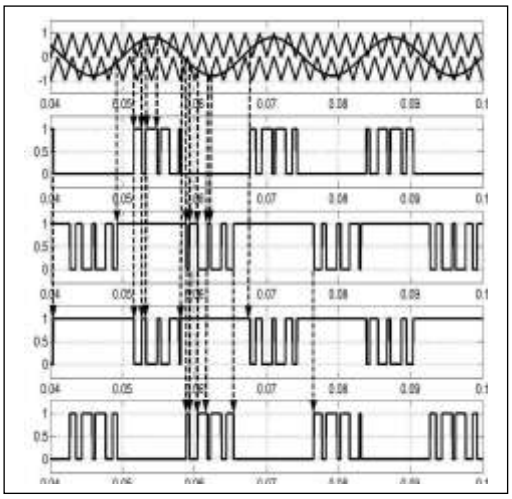

Fig:4 Simulation of carrier-based PWM scheme using the phase disposition (PD).

I. Modulation signal and in-phase carrier waveforms (II) Phase "a" output voltage.
II. Figure Shows the implementation of the phase disposition (PD) scheme.

Figure4 shows that two carrier waveforms are displaced in phase and compared with the sinusoidal modulation signal. Shows the phase "a" output voltage waveform

V. SIMULATION

Designing a SIMULINK model of 3-phnase 5 level DCMLI.As construction of 5 level three phase DCMLI is very complex .So we convert it into sub system models for easy way of understanding flow of operation. Below fig 5 represents sub system model of 5 level 3 phase subsystem model of diode clamped multi-level inverter.

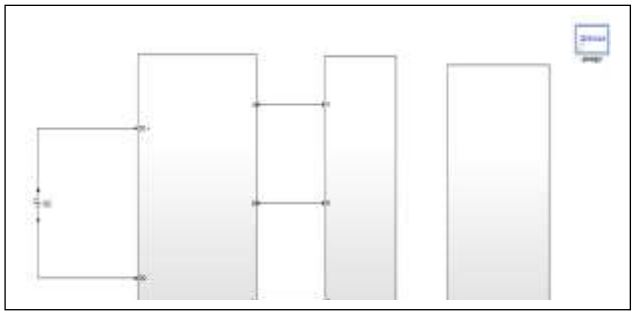

Fig 5: Sub System Model

As it is difficult and confusing to make the entire system in one single block the entire system is divided into three subsystems they are

As it is difficult and confusing to make the entire system in one single block the entire system is divided into three subsystems they are

1) Sub system model of DCMLI circuit.
2) Sub system model of SPWM providing gate signals for the power electronic switches which is again divided into three internal subsystems for each phase they are as follows:
- SPWM system for leg 1
- SPWM system for leg 2
- SPWM system for leg 3

3) Sub System circuit consisting load and measuring units

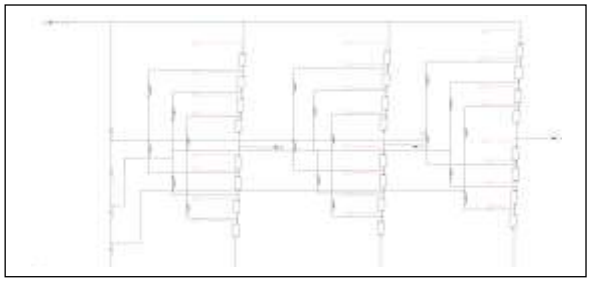

Fig6: Schematic SIMULINK circuit of DCMLI

As shown in the figure the circuit of DCMLI consists of
- 3 legs, each supplying 1 phase output
- Input DC supply

VI. PULSEWIDTH MODULATIONCIRCUIT:

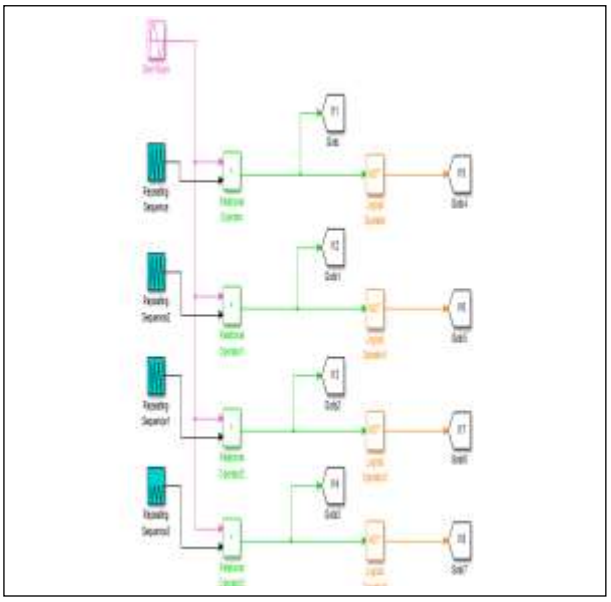

Fig 6: The SPWM Mechanism

The SPWM mechanism consists of a relational operator which compares four triangular waves and one reference wave and generates the gate pulses as discussed earlier

The generated pulses are given as gate input to the power electronic switches

There are eight outputs as shown in the fig in which four are directly given to the upper four switches and remaining are complimented and given to the lower portion of the circuit.

VII. MEASURING CIRCUIT WITH LOAD:

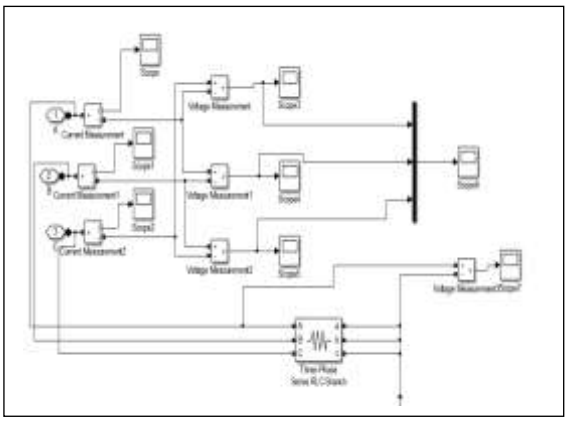

Fig 7: Measuring Unit with Load

The load and measuring unit mainly consists of Load connected to the output of 3 phase inverter.
Measuring unit for output of 3 phase inverter
Measuring unit for load.

Its measures load current and output voltage and waveforms can be seen in scope which is arranged at output

VIII. RESULTS AND CONCLUSION

Alternating Phase opposition Disposition (APOD)

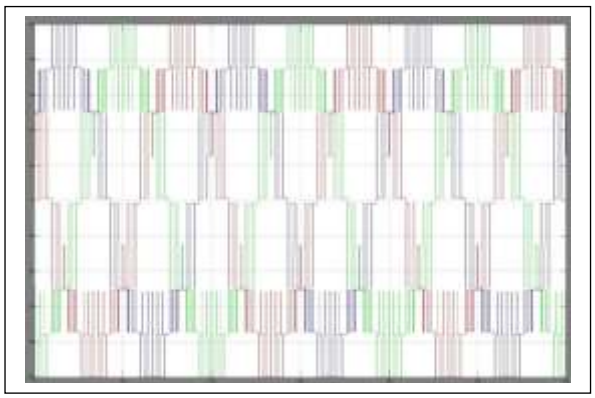

Fig 8: Three Phase Output Voltage Of DCMLI with APOD

As shown in figure 8 it represents output voltage waveform of three phase five level diode clamped multilevel inverter for alternate phase opposition disposition which is one of pulse width modulation technique.Above waveform can also be known as five stepped or nine level stair case waveform.The output voltage form is for a input source of 100 volts

THD analysis for output voltage with APOD technique:

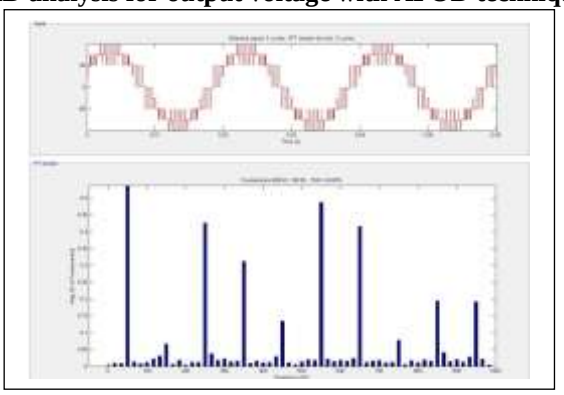

Fig 9: THD analysis of output voltage

As shown in the figure 9 it represents analysis of THD for output voltage using APOD technique.For input voltage of 100 voltage the output voltage has THD OF 24.69% for 3600HZ carrier frequency.

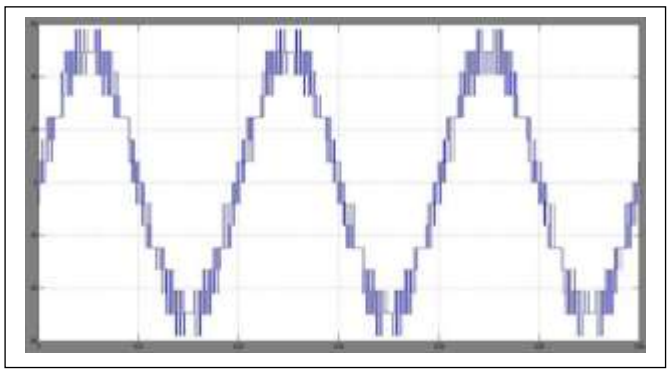

Fig 10: Load Current

THD Comparison for load current different carrier frequencies in APOD:

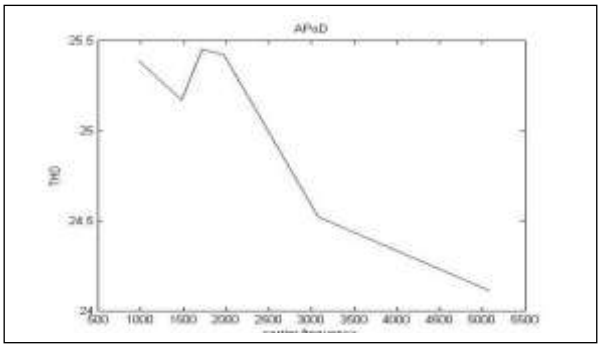

Fig 10:Variation of THD with APOD technique for different carrier frequencies for load current

As shown in figure 10 it represents a graph for THD analysis of load current with different carrier frequencies for APOD technique. Graph is plotted between THD and carrier frequency where x-axis represents carrier frequency and y-axis for THD.

THD comparison for output voltage with different carrier frequencies for APOD:

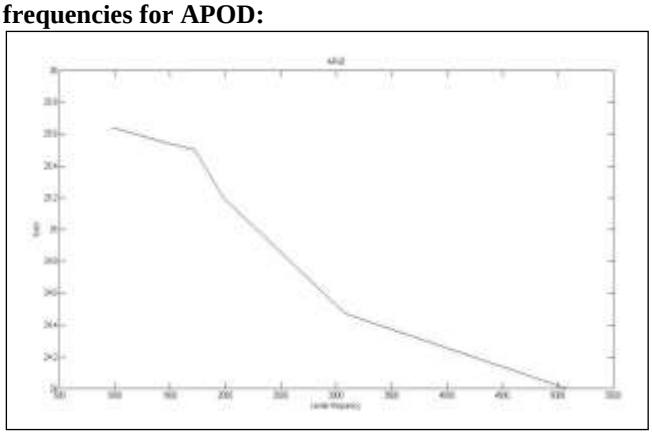

Fig 11:Variation of THD with APOD technique for different carrier frequencies for output voltage.

As shown in figure 11 it represents comparison of THD'S for different carrier frequencies for APOD technique for output voltage .Graph is plotted between THD and carrier frequencies where x-axis represents carrier frequency and y-axis represents THD.

Comparision of THD for all PWM techniques.

In this Paper first we are going to study the THD computations for different carrier frequencies and see the output of the DCMLI, and analyses other improvement study to the best THD result obtained**.**

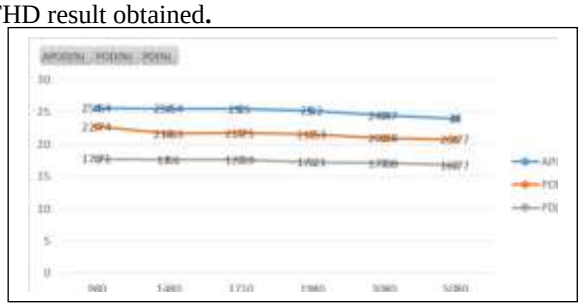

Fig 11: Comparison of output voltage THD by using APOD, POD and PD w.r.t change in career frequency

Output Voltage THD % analysis for different SPWM techniques

Carrier Frequency	APOD	POD	PD
980	25.39	21.89	17.19
1408	25.17	21.69	17.40
1720	25.45	21.58	17.42
1980	25.42	21.61	17.13
3080	24.52	20.77	16.88
5080	24.11	20.71	16.74

Table 1: **% THD analysis for different SPWM techniques**

From above analysis it can be observed that the THD of DCMLI mostly depends on the type of SPWM technique used and frequency of carrier wave will not show great change on the THD.

As we observed that minimum THD is obtained in PD technique let us observe the output voltage and current at this minimum THD value. Figure 6.14,6.15 represents THD comparision for different PWM techniques for output voltage and load current.

The minimum output THD is observed for PD technique as 16.77 for a carrier frequency of 5080HZ it is needed to observe the THD for varied modulation index for the minimum THD obtained.

REFERENCES

[1] P.S.Bimbhra, Power Electronics, Khanna Publishers, New Delhi, 2002.

[2] A. Nabae, I. Takahashi, and H. Akagi, “A neutral-point-Clamped PWM Inverter,” IEEE Trans. Ind. Appl., Vol. IA-17, pp. 518-523, 1981

[3] Multilevel inverter topology by andreasnordvail,chalmers university of Technology, sweden,2011.

[4] Xiaoming Yuan& Ivo Barbi, “Fundamentals of a New Diode Clamping Multilevel Inverter”, IEEE Trans. Industrial Electronics, Vol. 55, No.2,February 2008, pp. 21-26.

[5] Comparative analysis and simulation of diode Clamped an cascaded H-Bridge inverter using SPWM techniques--Mohit jain’.

[6] nalysis and Implementation of H-Bridge Multilevel Inverter. Tiwari,VivekShaikh, Mohammed Sadique Shaikh, Imran JainuddinShaikh, Ghulam,Shaikh, Arshad Ziyaul, Mujeebul

[7] https://www.elprocus.com/multilevel-inverter-types-advantages.