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Design of an Efficient Viterbi Decoder using Xilinx

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Abstract—The vision of wireless communication is to provide high-speed and high-quality exchange of information between two portable devices located anywhere in the world. In this hectic and unsecure world you need to be sure your data is not only safe and secure but that you are working with it at the highest possible speed. Convolutional encoding is a forward error correction technique that is used for correction of errors at the receiver end. The two decoding algorithms used for decoding the convolutional codes are Viterbi algorithm and Sequential algorithm. Sequential decoding has advantage that it can perform very well with long constraint length convolutional codes, but it has a variable decoding time. Viterbi decoding technique is used for decoding the convolutional codes but with the limitation to constraint length. It requires smaller constraint length. The Viterbi algorithm is the most extensively employed decoding algorithm for convolution codes. In digital communication and signal processing the estimation and detection of problems is done by using viterbi algorithm. The Viterbi decoding algorithm is widely used in radio communication, radio relay and satellite communication. This thesis represents the implementation of hard decision Viterbi decoding with constraint length 7 and code rate ½ and its algorithm. The decoder architecture is defined in VHDL and the circuit is simulated and synthesized on Xilinx 14.7.
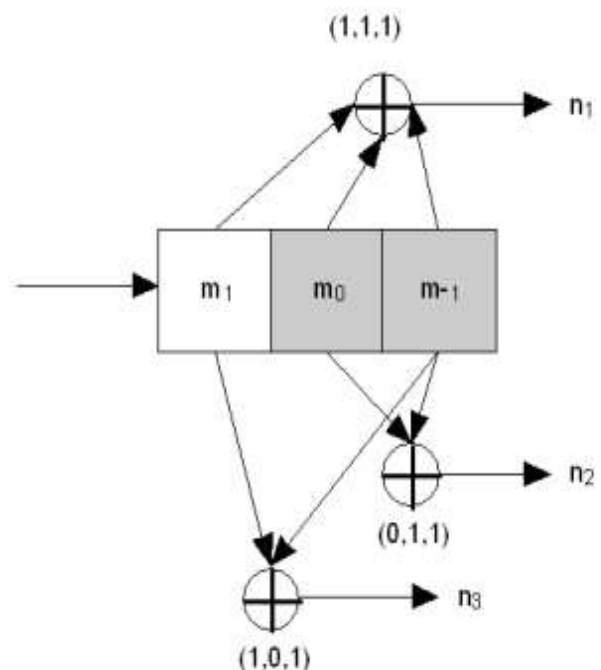
Keywords-Convolution codes, Viterbi algorithm, Path memory, Xilinx 14.7.

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I. INTRODUCTION

In the error correction field, there are various method proposed.The best known method is usingViterbi algorithm. Its entire error correction system consists of three important parts: theconvolution encoding, the error disturbance and the Viterbi decoding. The actual data isconvoluted using its convolution formula to develop codeword. Each codeword consist of twobits. Codeword is representation of original data and its redundant. If any error occurs in thetransmitted data, we can recover the original data using Viterbi algorithm.The basic building blocks of Viterbi decoder are branch metric unit, add compare and select unit and survivor memory management unit. The two techniques for decoding the data are traceback (TB) method and Register Exchange (RE) method. TB method is used for longer constraint lengths and it has fixed decodindg time. RE method is not appropriate for decoders with long constraint lengths.

II. CONVOLUTION ENCODER

A convolutional encoding is done by combining fixed number of input bits. The input bits are stored in the fixed length shift register and they are combined with the help of mod-2 adders. This operation is equivalent to binary convolution and hence it is called convolutional coding. The output from encoder is called code symbols.

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III. VITERBI DECODER

Viterbi decoder uses the Viterbi algorithm for decoding the data stream that has been encoded using convolutional encoder. Viterbi algorithm is used in communication and data storage application. The block diagram of Viterbi algorithm is shown in fig(b).
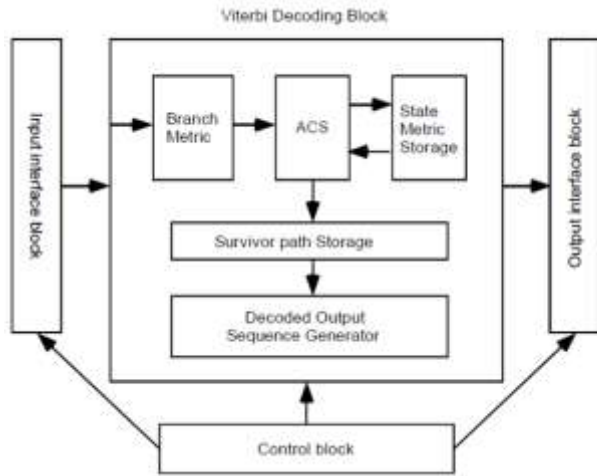
Fig(b)

It consists of the following modules:
Branch Metrics, ACS, State Metric Storage, Survivor Path Storage.
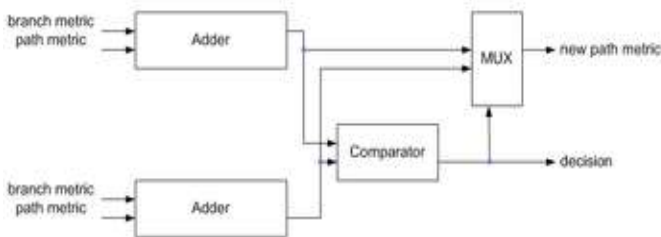
1.Branch Metrics
The branch metric block compares the received code with the expected code by using XOR operation and count the no of 1's. Figure (c) shows the block diagram of branch metrics.
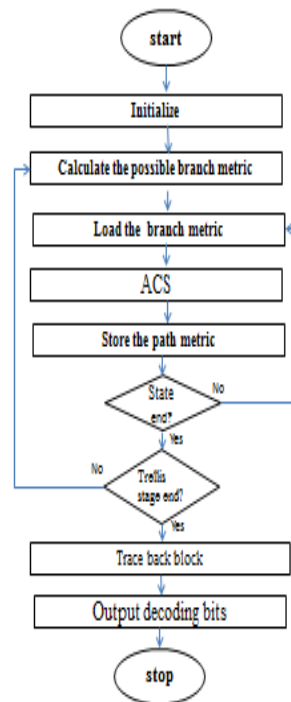

2. Add-Compare-Select(ACS)
The two adders calculate the partial path metric of each branch, comparator compares the metrics, and the selector selects an appropriate branch.

FLOW DIAGRAM:

IV.RESULTS

Simulation results for convolution encoder and Viterbi decoder.

V. CONCLUSION

An efficient Viterbi decoder using Xilinx is presented in this paper .This design is capable of doing error correction process and produce the original data transmitted by the transmitter. This design gives good synthesis results in speed and requires less power and cost is also reduced.

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