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VLSI Implementation of Modified Hamming Neural Network for non Binary Pattern Recognition

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***Abstract*—**Artificial intelligence is integral part of a neural network is based on mathematical equations and artificial neurons. The focus here is the implementation of the Artificial Neural Network Architecture (ANN) with on chip learning in analog VLSI for pattern recognition.
It is a maximum likelohood classifier which can be implemented using VLSI. Modified Hamming neural network architecture is presented.Thenew circuit is modified to accept real time inputs as well as to determine next close pattern with respect to input pattern.Modified digit recognition circuit was simulated using HSPICE level 49 model parameters with version 3.1180n at VDD of 3V. The circuit shows power consumption of 34mW and transient delay of 0.35nS.

Keywords-*VLSI, HSPICE, ANN, Hamming Neural Network, WTA*

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I. INTRODUCTION

Neural network is an interconnected group of natural or artificial neuron that uses a mathemetical or computational model for information processing[1].Artificial neural network is widely used in wide variety of problems in the area of patter recognition,signalprocessing,telecommunications,medical technical diagnosis,robotics and control systems. ANN are implemented in digital,analog or mixed system architecture.Though ANN can be implemented on software for real time application software based ANN are slower in execution in comparison to hardware based ANN[2].
Hardware implementation of ANN is more popular due to high speed of operation,low power. ANN has following features:

- Parallism: This makes neural network fast.
- Fault tolerent: The disrtributed data processing of ANN makes it easy to include necessary redundancy to implement a fault.
- Regular: ANN are composed of few different elements that are interconnected in a regular way. This makes the implementation easy[3].
- Adaptive: By programming neural network can be made adaptable to new working condition.
- Asynchronous: This is an advantage while implementing electrical circuitsbecause problem with spike on supply current worst case timing designs are eliminated[4].

Lippmann provides an introduction to the field of artificial neural networks by reviewing six important neural network models that can be used for pattern classification [5] as shown in figure 1.

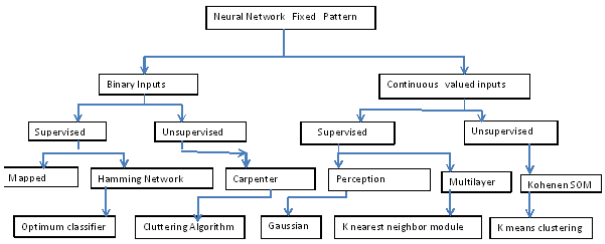

Figure 1 Neural Network models

II. HAMMING NEURAL NETWORK

It is a maximum likelohood classifier which selects from a group of exempler pattern the closest one to an input pattern[6].All patterns are presented in 1-D binary vector.When an input pattern P=(P1,P2,…Pn) is presented to the network,hamming network calculates matching score between input pattern and each exemplar pattern.

$$Wi=(Wi1,Wi2,\ldots Win) \text{ where } 1\leq i \leq M$$

which is defined as

$$Msi = N - HD(Pi,Wi) = N - \sum_{J=1}^{N} |Pj - Wij| \quad (1)$$

where HD(Pi,Wi) is the hamming distance between input pattern P and exemplar pattern Wi. Pj is jth element of input pattern $P(1\leq j \leq N)$ Wij is jth element of exemplar pattern Wi.After this WTA operation is done to the matching score where only one winner is indicated by high level output.

$$Vi = \begin{cases} 1 & i = 1 \\ 0 & i \neq 1 \end{cases} \quad (2)$$

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Advantages of hamming neural Network are number of connections required is less compared to other net as well as it

is acts as a minimum error classifier and Hamming net does not suffer from spurious outputs pattern which can produce 'no match' result[7]. Itdoes not require digital to analog converter. Thus it is most suitable to implement on CMOStechnology[8].

III. MODIFIED 0-9 DIGIT RECOGNITION CIRCUIT

The modified digit recognition is based on hamming neural network concept. In the modification part, initially the circuit is determining the winner pattern and the output will be high corresponding to that winning pattern whereas all other outputs will be inhibited to logic zero. When a trigger pulse is applied to circuit, the first winner output voltage will be inhibited to zero and the output voltage corresponding to second winner (i.e. the most similar pattern having least hamming distance with respect to winner pattern) will be incited to rise to logic high level. So, we will be able to determine the most similar pattern using the same basic circuitry. Further, the pattern recognition circuit is altered so as to recognizing the data from real time patterns which takes input in the form of intensities[11]. The block diagram is as shown in figure 2.

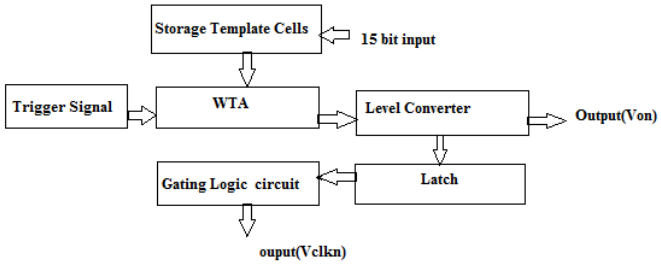

Figure 2 Block diagram of modified digir recogniiton circuit

Additional features in circuitry are triggering signal generation circuit, gating logic circuit, latch circuit.

Storage Template circuit:These are 10 template storage sub circuit each one stores a single digit (0-9). Each digit is represented by 5x3 matrix form. This requires 15 inputs (in1 to in15).Corresponding voltages are generated from the intensities of inputs under recognition [12]

Modified Winner Take all circuit (neuron cell): It determines the most close template pattern with respect to input pattern.. The circuit is modified with trigger signal generation circuit as shown in figure (1). A signal controlled NMOS is added in parallel to each neural cell which leads to inhibiting of that particular neural output when a triggering signal is applied across it. The triggering signal is applied when we want to determine the most similar pattern with respect to winning pattern.

Trigger signal Generation: The signal is generated when we want to determine the most similar pattern having least hamming distance.

Level Converter**:**This circuit converts neural output current in equivalent voltage. The operation is similar to old 0-9 level converter. It accepts input from WTA cells and converts in to equivalent voltage as Vo0 to Vo9[13].

Latch Circuit:It is mainly used to latch output. It accepts input from level converter in the form of Vo0 toVo9. Two complementary clock signals clkx and clkb are used to define the time at which input is to be latched. The outputs are V0, to V9.

Gating logic circuit: Logical ANDing is done between latch output and clock signal. The output signals are VCLK0 to VCLK9.

IV. SIMULATION AND RESULTS

Modified digit recognition circuit was simulated using HSPICE level 49 model parameters with version 3.1180n VDD of 3V.

DC Analysis for pattern 0 is as shown in table 1 where output voltage terminal Vo0 has voltage 2.63V showing HIGH status while all other output nodes are in nanovolts showing LOW status.When the input pattern perfectly match with stored template, maximum current flows showing maximum potential at that node and remaining node based on hamming distance, the potential value changes. Hencenode X which corresponds to output terminal of 0 storing template cell has potential of 1.9V while all other are low. DC analysis of level converter shows output terminal corresponding to 0 Vo0 has voltage 2.63V while all other has nanovolts.This shows modified circuit is able to recognize '0' pattern.

Transient analysis was done for 100nS. Figure 3 shows the response. For input pattern '0', Vo0 sets to 2.63V while remaining all is set to LOW.

Table 1 shows summary of modified digit recognition circuit.

Table 1 SUMMARY OF 0-9 DIGIT RECOGNITION

VDD	3V
Power consumption	34mW
Rise time Fall time delay	0.35nS
Operating frequency	100MHz
Technology	180nm
Advantage	Works with Real time data

SIMULATION FOR NON BINARY INPUT PATTERN (REAL TIME INPUT)

The circuit is simulated using Synopsys HSPICE version 3.1, level - 49 on 180nm technology with supply voltage of 3V at 100MHz for real time input ' 0' by capturing the input image using low intensity camera. The input image is converted into 5x3 matrix form.

TABLE 2 DC ANALYSIS of REALTIME DIGIT- 0

Rise Time and Fall Time delay	10Ps
Clk	100MHz

Transient Analysis for digit 0 shows input pattern 0 is recognized first making Vo0 high. Later this output goes lowas Vclk0 goes high. It determines next close pattern for

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digit 8 hence Vo8 goes high. Figure 4 shows the response. A delay of 0.35ns is observed to get second close pattern high.

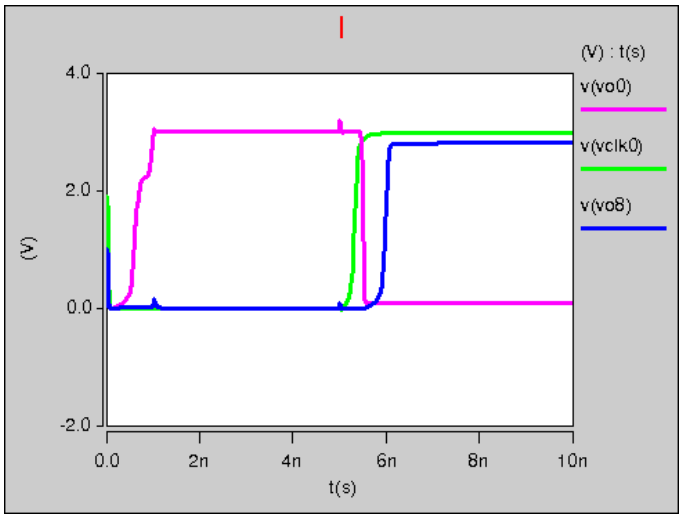

Figure 4 Transient Analysis of real time digit 0 and its close pattern digit 8

CONCLUSION

Modified Hamming neural network is used for 0-9 digit recognition. The circuit was modified to accept real time inputs as well as to determine next close pattern with respect to input pattern. This type of circuit can be utilized by visual tracking system providing them ability to have backup recognition utility in case first recognized pattern proves to be incorrect. The circuit shows power consumption of 34mW and transient delay of 0.35nS.

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REFERENCES

[1] Schmid ," Hardware Realization of a Hamming Neural Network with On-Chip Learning", Proceeding of the IEEE International Symposium on Circuits and Systems, May 1998, Vol. 3, , 1998pp. 191-194

[2] G. Cauwenberghs," Neuromorphic learning VLSI systems: A survey Neuromorphic Systems Engineering, 1998., pp 381–408

[3] Guoxing ," A Modified Current Mode Hamming Neural Network for Totally Unconstrained Handwritten Numeral Recognition", International Joint Conference on Neural networks,Vol 3,1998,pp 1857-1860

[4] SorinDraghici,"Neural Networks in analog hardware design and implementation issues", International Journal of Neural Systems Vol. 10, No. February, 2000,pp 19–42

[5] Huang," Neural Implementation of Fuzzy K-NN Classification for Seismic Pattern Recognition", IEEE International Conference on Neural Networks Vol 3 , 2002,pp 1588-1593

[6] B. Shi, Gu Lin Programmable and expandable hamming neural network circuit US patent 6341275B1,2002

[7] B Shi, Guoxing Li, "VLSI neural fuzzy classifier for handwriting recognition" Patent no. US 7146037 B2, Dec 5 2006

[8] Fengwei An, Hans Jürgen Mattausch, Tetsushi Koide An FPGA-implemented Associative-memory Based Online Learning Method Int.Journal of Machine Learning and Computing Vol.1,No. 1 April 2011

[9] P.Panddi, Selvi, Dr.T.Meyyappan ,"Recognizing handwritten numerals using multilayer feed forward backpropogation neural network" ,Computer Technology &Applications,Vol 3 (6), 1939-1944 ISSN:2229-6093, Nov-Dec 2012

[10] BehzadGhanavatiBehbodMashouf," Design of a VLSI Hamming Neural Network For arrhythmia classification", First Joint Congress on Fuzzy and Intelligent Systems Ferdowsi University of Mashhad, Iran 29-31 Aug 2007

[11] ArchanaSubhash ," VLSI Design Approach for Efficient Pattern Recognition Algorithms: Review ", IFRSA International Journal Of Electronics Circuits And Systems|Vol 1|issue 1| ISSN No(online) 2277-5870Feburary 2012

[12] S. Archana, Dr. B.K. Madhavi, Dr I V MuraliKrishna ," Current Mode Hamming Neural Network for 3 - Bit Pattern Recognition Using 180 nm CMOS Technology", Proceedings of the National Conference on Circuits, Signals and Systems (NCCSS-2015),MuffakhamJha College of Engineering and Technology, Hyderabad, TS. 22nd - 24thJanuary.pp.23-26.ISBN : 978-93-8257 0 -47 -9, 2015

[13] S. Archana, Dr. B.K. Madhavi, Dr I V MuraliKrishna,"Reliable Recognitionof Handwritten Digits Using Hamming Network" 6 thInternational Conference on Advanced Computing (IACC), 2016 Date of Conference: 27-28 Feb. 2016 Date Added to IEEE *Xplore*: 18 August 2016 ISBN Information: Electronic ISBN: 978-1-4673-8286-1 Print on Demand(PoD) ISBN: 978-1-4673-8287-8 INSPEC Accession Number: 16232624 DOI: 10.1109/IACC.2016.94Publisher: IEEE,2016

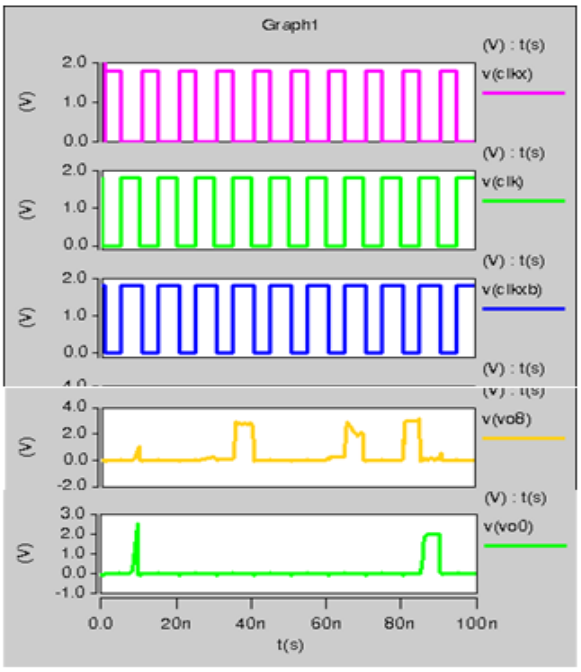

Figure 3: Transient analysis of level converter