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Design and Analysis of Current Mirror Circuits on HSPICE 180nm Technology

S. Archana,
ECE dept. BRECW
Hyderabad, India
archanasubhash2006@yahoo.co.in

Dr. B. K. Madhavi,
ECE dept, SWEC, Gandipet
Hyderabad, India
bkmadhavi2009@gmail.com

Dr. I V Murlikrishna
JNT University,
Hyderabad , India
iyyanki@gmail.com

***Abstract*—** Current mirrors are one of the most common buildings blocks both in analog and mixed-signal VLSI circuits. Current mirrors are very useful elements for performing current mode analog signal processing. It generated dc current in direct ratio with reference current.Thus used for biasing integratred circuits also as active load in amplifier design, scaling and replication purpose. This paper presents design and analysis of basic NMOS and PMOS current mirror with various conditions and also few concepts likecurrent steering and scaling, source degenerative circuit to improve output impedance.Synopsys HSPICE circuit simulator with Stanford NMOS and PMOS model at 180nm technology atV_{DD} of 1.8V is used for simulation of all circuit. Simulation result shows NMOS current mirror power consumption of 3.9µW while PMOS current mirror takes 25µW power. Source degenerative circuit shows output impedance of 1203MΩ.

Keywords*-VLSI,HSPICE,CM*

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I. INTRODUCTION

Transistors are frequently used active device in analog ICs. For operation of ICs, proper biasing is essential. A current mirror is an element with at least three terminalswhich can be used as source or sink as shown in figure 1. The common terminal is connected to a power supply or ground,The output current is equal to the input current multiplied by a desired current gain[1]. If the gain is unity, the input current is reflected to the output, leading to the name current mirror. Current mirrors are very useful elements for performing current mode analog signal processing.They are used in design of neural network based current mode winner take all circuit to determine min or max among n input signals.Therefore their designs must fulfill the following requirements [2]:

1. Input impedance should be zero
2. Output impedance should be infinite
3.Output current should be constant over wide swing of voltage
4. Accurate copy of input current.

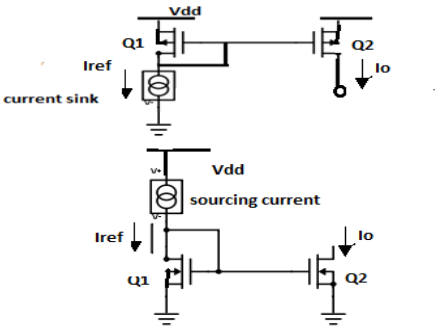

Figure 1NMOS andPMOS current source and sink

Neglecting channel length modulation,

$$Iref = \frac{\mu nCox}{2}\left(\frac{W}{L}\right)_1 (Vgs - Vt)^2 \quad (1)$$

where

$$R = \frac{VDD - Vgs}{\frac{\mu nCox}{2}\left(\frac{W}{L}\right)_1 (Vgs - Vt)^2} = \frac{VDD - Vth}{Iref} - \frac{1}{\sqrt{Iref\left(\frac{\mu nCox}{2}\left(\frac{W}{L}\right)_1\right.}}$$

If different W/L ratio transistors are used, current mirrors can be used as current multiplier as shownbelow.
From the figure 1

$$\frac{\mu nCox}{2}\left(\frac{W}{L}\right)_1 (Vgs - Vt)^2 = Iref$$

$$\frac{\mu nCox}{2}\left(\frac{W}{L}\right)_2 (Vgs - Vt)^2 = Iout$$

$$Iout = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}.Iref \quad (2)$$

II. SIMPLE NMOS CURRENT MIRROR

Current mirror acts as a resistor and its internal resistance is internal resistance of transistor M2. M1 is used to provide biasing[3].Figure2 is designed for reference current of 460µA.

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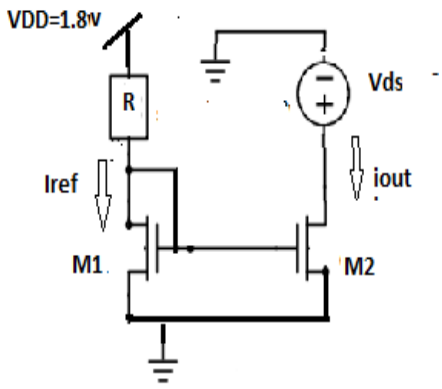

Figure 2 NMOS current mirror without VSS for Iref=460 µA

As shown in figure 2, reference current is copied in output transistor M2 after proper biasing. Based in the given data of reference current of 460µA, R= 2K,select appropriate value of W/L ratio for both transistors such that Iout will be same as that Iref by using standard current equation(2) DC analysis was done. Figure3 shows the response for output characteristics.

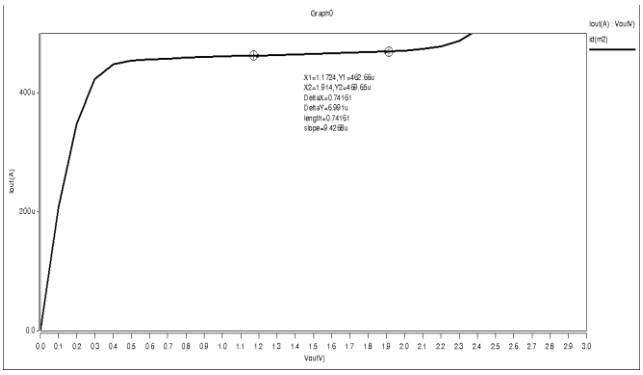

Figure 3 Output characteristics of basic NMOS CM

Analysis shows output current is almost equal to input current. Various parameters calculated are listed in table 1.Same circuit was simulated by applying VSS of -1.8V to improve output voltage swing at the cost of high power dissipation.. The DC simulated result is as shown in figure 4.

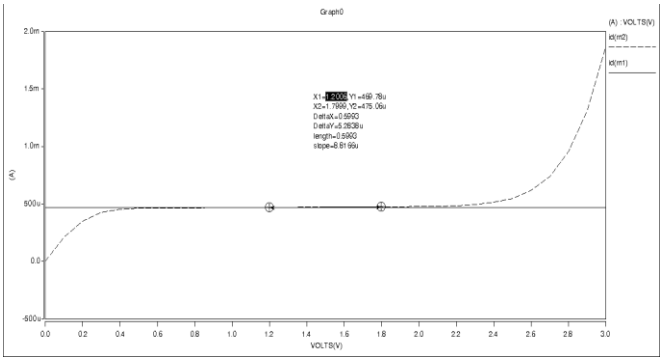

Figure 4 Output characteristics of basic NMOS CM with VSS

III. *NMOS CASCODE* CURRENT *MIRROR WITH VSS AND IREF=10 MA*

In our simulation we look at a 1/0.5 current mirror for 10 µ A where we load the mirror output with a voltage source. This voltage is dc sweeped and we look at the output current. We can get the perfect mirror output current, when we have VDS = VGS[3]. To achieve this we use a cascode to set VDS of the output transistor M3 to its VGS as shown in figure 5. Gate of transistor is biased properly which keeps the transistor in linear region. For this we need a cascode VGS voltage of twice the threshold voltage for the input current[4]. As we can see in the plot the current is more stable. This is because VDS of M3 is now fixed to a value where the early effect cancelled as a diode connected NMOS transistor has VGS = VDS so we see that the curve has a quadratic part and a linear part which is defined by the early voltage i.e. 1/vearly = lambda[5]. Power dissipation is reduced as compared to basic NMOS current mirror but gain is slightly reduced as shown in table 1.

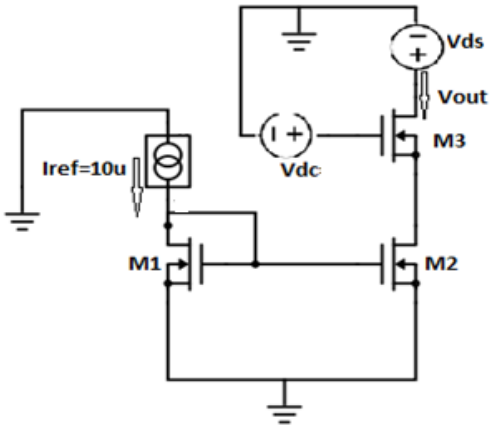

Figure 5 Cascode NMOS CM for Iref=10µA

DC Analysis shows output is stable for more duration compared to basic NMOS current mirror. Figure 6 shows output characteristics.

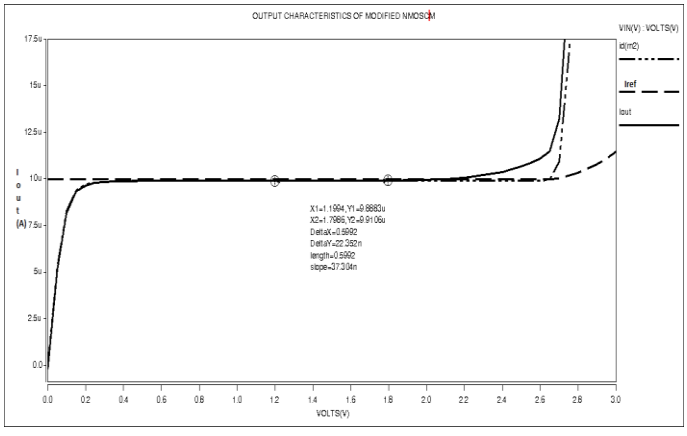

Figure 6 Output characteristics of cascode NMOS CM

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IV. SIMPLE PMOS CURRENT MIRROR

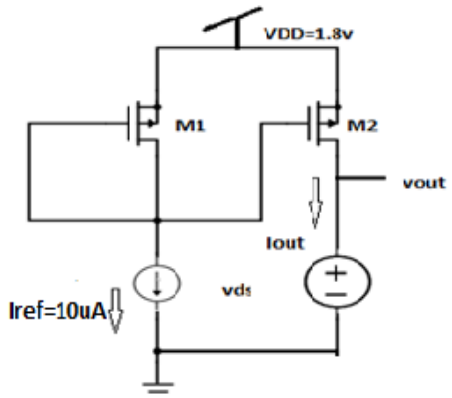
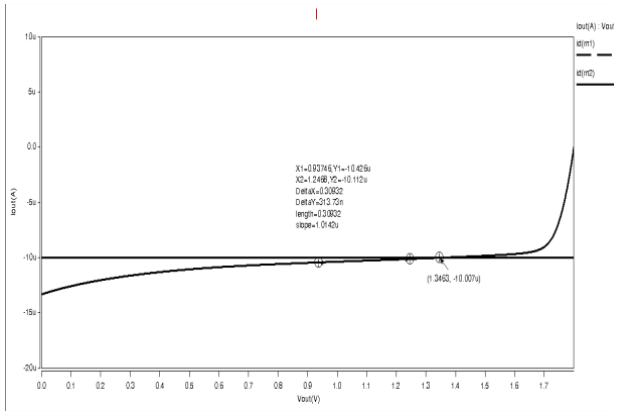


Figure 7 Basic PMOS current mirror

Figure 7 shows schematic diagram for basic PMOS current mirror.DC analysis without VSS and with VSSshows output characteristics as shown in figure 8 and 9.



. Figure 8 Output characteristics of basic PMOS CM

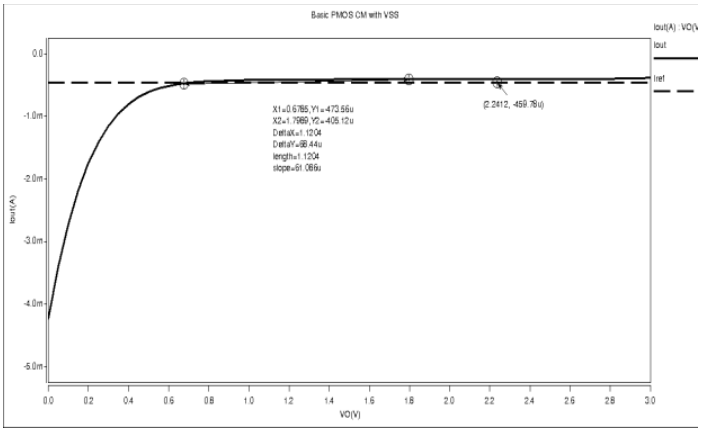


Figure 9 Output characteristics of basic PMOS CM with VSS

Table 1 shows comparison for various NMOS current mirrors analyzed.

Table 1 Comparison of various basic NMOS CM

NMOS Current Mirror	Iref(A)	Gain	Power dissipation (W)
without VSS with R	460µ	1	1.24m
with VSS,R	460µ	1	4.57m
With current source and 2 NMOS	460u	0.99	679 µ
Modified with current source and 3 NMOS(cascode)	460u	0.95	512 µ
With current source and 2 NMOS	10µ	1	3.9µ
Modified with current source and 3 NMOS to reduce power dissipation	10µ	0.89	1.186µ

Table 2 shows comparison between various PMOS current mirror analyzed in our work.

Table 2 Comparison of various basic PMOS CM

PMOSCurrent Mirror	Iref (A)	Gain	Power dissipation (W)
without VSS with R	460µ	1	1.47m
with VSS,R	460µ	1	3.9m
With current source and 2 PMOS	460u	1	1.42m
With VSS,current source and 2 PMOS	460u	1	169m
Modified with current source and 3 PMOS	460u	1	1.485m
With current source and 2 PMOS	10µ	1	25µ
Modified with current source and3 PMOS to reducepower dissipation	10µ	1	28.5µ

V. CURRENT STEERING CIRCUIT

Current steering plays an important role in design of determining highest or lowest signal strength input signal [6]. This concept is used in winner take all circuit used as MAX or MIN circuit in pattern recognition applications.Drain current of M3 comes from drain of M4[7]. Hence I4=I3 can steer a current from NMOS current mirror to PMOS current mirror or vice versa as shown in figure 10. NMOS transistor should match mutually also PMOS transistor should match such that Vth4=Vth5[11,12].

$$\frac{I5}{I4} = \frac{\left(\frac{W}{L}\right)5}{\left(\frac{W}{L}\right)4} = 1$$

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(3)

Thus source current I5 can be related to reference current Iref as

$$\frac{I5}{Iref} = \frac{\left(\frac{W}{L}\right)3}{\left(\frac{W}{L}\right)1} \cdot \frac{\left(\frac{W}{L}\right)5}{\left(\frac{W}{L}\right)4} \quad (4)$$

. The change is due to channel length modulation factor[8]. Table 3 shows DC characteristics for the same. Figure 11 showsoutput characteristics.

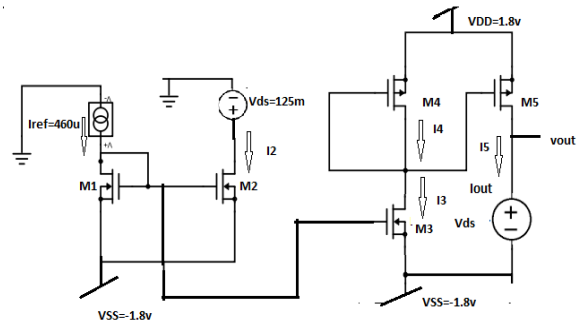

Figure 10 Current steering circuit

TABLE 3 DC CHARACTERISTICS OF CURRENT STEERING CIRCUIT

Iref(A)	Rin(Ω)	R0(Ω)	Gain	Power dissipation(W)
460µ	530	178K	0.98	2.4750m

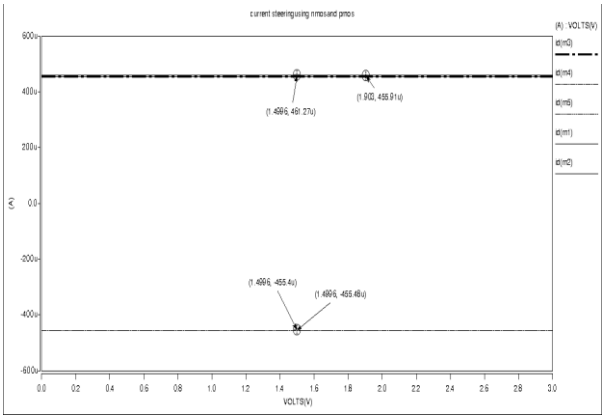

Figure 11 Output characteristics of current steering circuit

VI. CURRENT MIRROR FOR SCALING PURPOSE

Depending on aspect ratio output current can be made integral multiple of reference current[9]. Figure 12 shows its use in scaling. Transistor M2 has twice width of transistor M1 hence Id(M2) is doubled while for M5 width is halved hence Id(M5)also halved. Figure 13shows output response. Voltage source power dissipation was 104.8854µwatts.

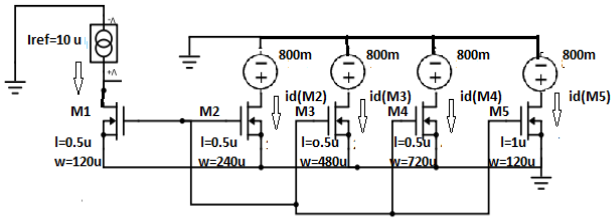

Figure 12 Schematicof Currentmirror for scaling purpose

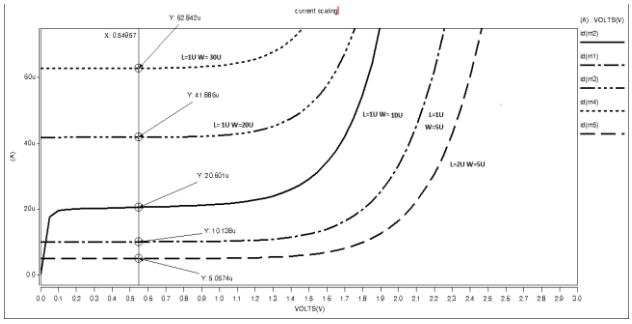

Figure 13Output characteristics of Current mirror for scaling purpose

VII SOURCE DEGENERATION CURRENT MIRROR

Schematic diagram for source degeneration current mirror is as shown in figure 14.It is used to improve output impedance[10,13]. Table 4 compares output impedance without R and with R

(source degeneration circuit).It is found that rout is improved by a factor 500**.** Figure 15 shows output characteristics of source degenerative resistance circuit.

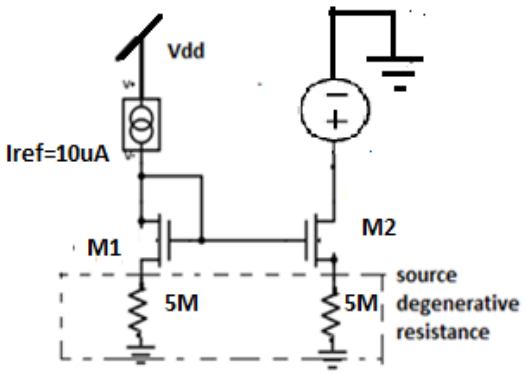

Figure 14 Source degeneration circuit

Without source degeneration output impedance was 2MΩ while with source degeneration circuit it is improved and is equal to 1203MΩ .

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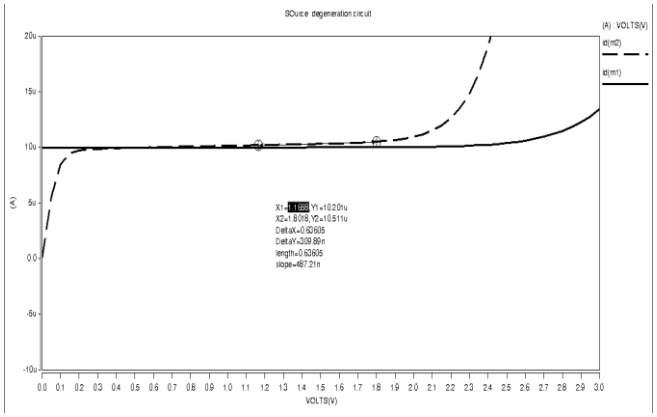

Figure 9 Output characteristics of source degeneration circuitt

CONCLUSION

Simulation on various designs of basic NMOS current mirror using HSPICE 180n technology at VDD of 1.8V shows input impedance is least in simple NMOS current mirror. Power dissipation of PMOS current mirror is more than NMOS current mirror. Power dissipation is least in modified cascode arrangement.For low power design it is useful. Apart from this various concepts useful in analog VLSI signal processing like use of current steering circuit, current scaler circuit, source degeneration circuit are analyzed.

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