International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169
Volume: 5 Issue: 6 1187 – 1190

VLSI Realization of Switched Hamming Neural Network for 3-Bit Digit Recognition

S. Archana,
ECE dept. BRECW
Hyderabad, India
archanasubhash2006@yahoo.co.in

Dr. B. K. Madhavi,
ECE dept, SWEC, Gandipet
Hyderabad, India
bkmadhavi2009@gmail.com

Dr. I V Murlikrishna
JNT University,
Hyderabad , India
iyyanki@gmail.com

***Abstract*—**Thispaper aims at analyzing neural network method in pattern recognition. HSPICE level 49 simulation of switched current mode hamming neural network is able to recognize any threebit digit provided its template is stored using current mirror. It determines highest input current signal and output it based on time division basisusing Winner Take All circuit (WTA) based on time division basis. The DC simulation shows power dissipation of 1.8517mW and rise time delay of 3.2318E-09 s

Keywords- VLSI, HSPICE, CM, WTA, SCHNN, AR, RR

*****

I. INTRODUCTION

A neural network is a processing device, whose design was inspired by the design and functioning of human brain and their components. The proposed solutions focus on applying Hamming Network and MAXNET model for pattern recognition [1].The efficient hardware integration of neural network based paradigms is a key element in speeding up the implementation of real-time applications while taking full benefit of their inherent parallel operation mode. The focus of the work described in the following is the development and integration into an integrated circuit of a specific NN model which is shown to allow several pattern recognition applications [2]. The proposed Hamming artificial neural network (ANN) performs Hamming distance calculation between a previously stored set of patterns, and the current input, based on two layer architecture [3]. The thrust of recent research has changed. CMOS is widely used for hardware implementation using various signaling scheme such as voltage , current, frequency, semi digital ,pulse modulated or fully digital[9,10] It is a two layer network. First layer consists of matching rate computation circuit for modules while second layer consists of matching rate comparison circuit[7]. Second layer also have other subcircuits such as switched current type order ranking circuit, pulse generating circuit,identification rejection judgement[4,5].

- Matching rate computation circuit: This layers compares between to be identified pattern and template pattern. This is called matching rate computation.
- Matching rate comparison circuit Once the computation is done ,second layer is used to provide ranking the order of matching rate.
- Switched current typr order ranking circuit: It accepts switched current input signals. It determines highest input current signal and output it based on time division basis.
- Identification rejection judgement circuit: It performs both absolute and relative judgement.Absolute judgement is
- Pulse generating circuit: It generates various clock pulses for sequential operation of network.

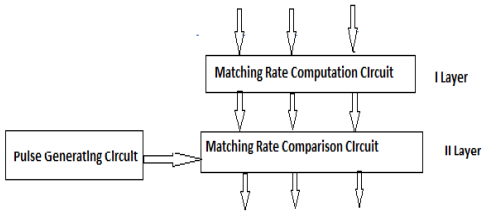

Figure 1 Block diagram for switched current mode hamming neural network

This second layer determines the most close pattern with respect to to be identified input pattern.It has winner take all circuit internally for determining the best match between input pattern and stored templates.The previous version of VLSI implemtation of pattern recogniiton circuits using hamming neural network could output only the most close match.Such circuits had less reliability. Present systems are much complex in terms of number of standard patterns stored as well as being multistage system requires more reliability[10]. This made it necessary to determine more than one output as

standard pattern which are most close to the to –be- identified input pattern.This concept is implemented in switched current mode hamming neural network which improves the reliabilty of system. Outputing the most close standard pattern first and

then outputing less close standard pattern is called ranking order on time division basis. If there are N standard pattern out of which m standard patterns match with input pattern then all m standard patterns are outputed in the order of matching score. Switched current mode hamming neural network also uses concept of thresold value to determine more than one output as standard pattern which are most close to to-be-identified input pattern[9]. Threshold value is calculated based on system decision such that it is divided into two absolute and relative threshold value. It uses two methods absolute identification rejection (AR) and relative identification rejection(RR) method[8].

- Absolute identification rejection (AR) Method: Absolute method determines single output. System produces identificaton rejection signal(IR) only when maximum matching rate is less than absolute threshold value. Basic hamming neural network uses this method.
- Relative identification rejection (RR) Method: Relative method determines multiple outputs, System produces identification rejection signal(IR) when a difference value between maximum matching rate and second maximum mathching rate is less than the relative threshold value.Thus overall system performance is improved compared to basic hamming neural network[8].

The main blocks used are :

- Current mirrors for template storage units
- Winner take all circuit
- Absolute identification rejection and Relative identification rejection

II. CURRENT MIRRORS AND TEMPLATE STORAGE UNITS

First m input patterns of size n bits are given to m template storing modules.Thus each neuron cell is storing one fixed pattern. In our design we took three templates each of size 3 bit to avoid complexity. Each input pattern has 3 bits: in1, in2 and in3 . The template storage designed is designed for 3bits.Only three units are designed. For 000,101 and 111 input Set any one value, equivalent currents are generated from each cell and are outputed as Iin1, Iin2 Iin3 respectively.These currents are given to current mirror. Based on clk status the current is given to winner take all circuit.

III. III WINNER TAKE ALL CIRCUIT

The winner Take all circuit is used to determine largest current among the three input currents I0,I1 and I2. The purpose to determine maximum of input current is to identify which neuron cell gives maximum degree of matching score. The circuit uses inhibitory feedback to determine largest input signal current. Presently The output of WTA is given using following equation:

$$Iwout = MAX(I0,I1,I2) \quad (1)$$

If the input pattern is 000, I0 will be maximum among three cells.Hence WTA makes node 1 as high and node 2 and 3 as Low.

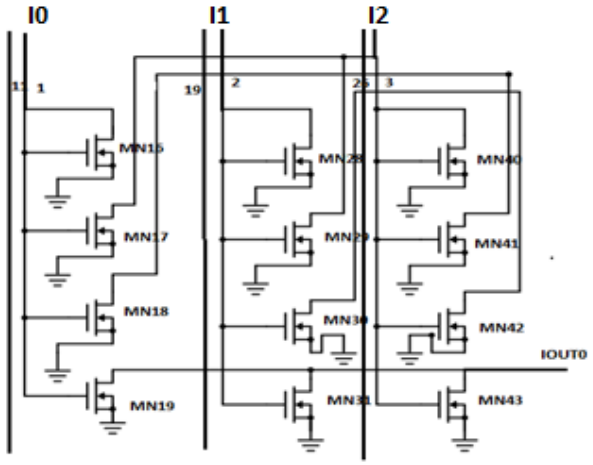

Figure 2 Winner Take all circuit of SCHNN

IV. ABSOLUTE IDENTIFICATION REJECTION AND RELATIVE IDENTIFICATION

The circuit consists of two input WTA. First WTA compares two inputs and set output for absolute identification circuit high to determine one and one output pattern, if switched hamming neural network uses this method else it sets output for relative rejection circuit if switched hamming neural network uses hod to determine one and one output pattern, If switched hamming neural network uses relative identification method,the network determines more than one output pattern.

V. V ANALYSIS AND RESULTS

The circuit was simulated on HSPICE. The response is as shown in figure 4.12The template circuit was simulated for input in1 in2 in3 as 000. As this pattern is stored in first neuron cell,the current Iin0 representing output of first neuron cell is maximum and Iin2 representing output of third cell is least. Table 1 shows DC analysis for template storage ciruits.

Table 1 Output current associated with input pattern 000 across 3 neuron cells

In1	In2	In3	Iin0(V)	Iin1(V)	Iin2(V)
0	0	0	860m	759m	127m

Transient analysis shows output across repective terminals as shown in figure 3

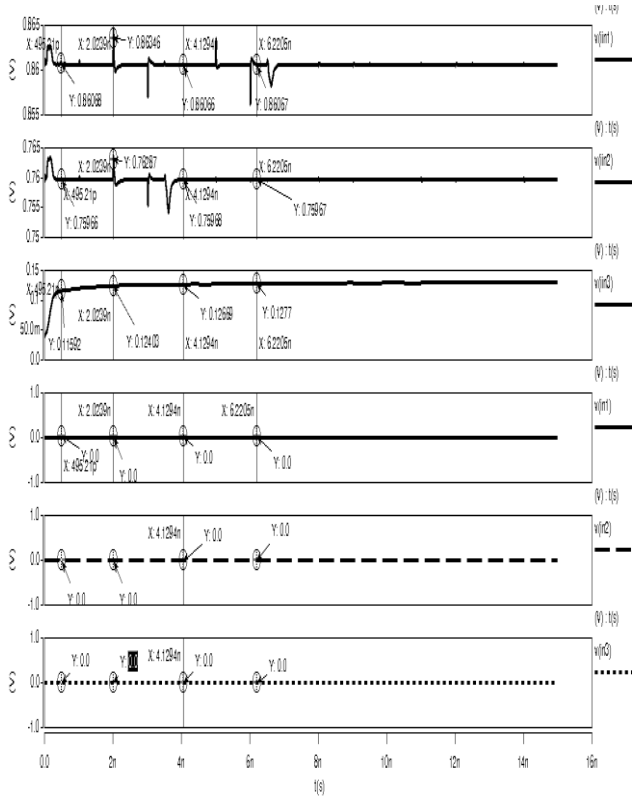

Figure 3Transient analysis of template storage circuit in SCHNN

Table 2 DC analysis of winner take all cirucit.

CKP	CK0	Iin0	Iin1	Iin2	I0	I1	I2	Iout0
H	L	860m	759m	127m	864m	760m	124m	860m

Table 2 shows DC analysis of winner take all circuit. As it selects largest of three input signals, Iout0 is equal to I0. Transient analysis shows Vout1 high compared to Vout2 and Vout3. Hence Vout4 is equal to Vout1as shown in figure 4.

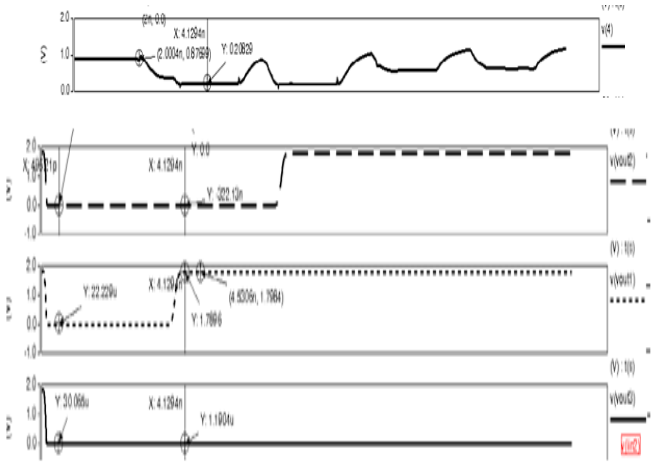

Figure 4Transient analysis of winner take all circuit in SCHNN

Partial simulation result of switched hamming neural network s as shown in figure 5. Based on closeness(hamming distance) of input pattern with template stored value, equivalent currents are generated for 000,101 and 111 inputs.The rise time measured for switched hamming neural network for 3 bit digit recognition circuit was 3.2318E-09 at power dissipation of 1.8517m W.

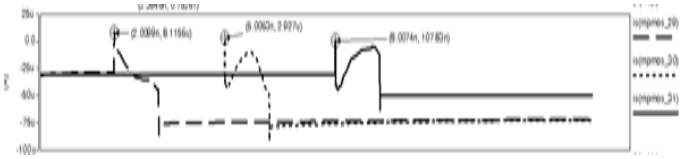

Figure 5 Partial Transient analysis of SCHNN

VI. CONCLUSION

Simulation of switched hamming neural network using HSPICE level 49 model parameters with version 3.1180n at VDD of 1.8V showscircuit is able to recognize any three bit digit inputs provided at least one is stored in template storage unit. Using absolute identification rejection and relative identification rejection it is possible to determine exact pattern or exact and most close pattern. The limitation thus for storing ten digit is ten neuron templates need to be designed with ten input WTA which makes the circuit more complex. More over maintaining clock for proper operation is not easy. Still it is one of the simple method used in pattern recognition for digit recognition.

ACKNOWLEDGMENT

I would like to thank my guide Dr. BK Madhavimadam,whose constant support inspired me to work on this topic. I also thank my guide Dr. I V Murali Krishna for his valuable suggestions and guidance.

REFERENCES

[1] S. Badel, A. Schmid, Y. Leblebici, "VLSI Realization of a Two-Dimensional Hamming Distance Comparator ANN for Image Processing Applications", ESANN, 2003 proceedings - European Symposium on Artificial Neural Networks Bruges (Belgium), 23-25 April 2003, d-side publi., ISBN 2-930307-03-X, pp. 445-450

[2] R. P. Lippmann, "An Introduction to Computing with Neural Nets, IEEE ASSP"

[3] A. Schmid, Y. Leblebici and D. Mlynek, "Hardware Realization of a Hamming Neural Network with On- Chip Learning", Proceedings of the 1998 IEEE International Symposium on Circuits and Systems ISCAS'98, Monterey, CA, 1998. Magazing, April 1987.

[4] Gioxing Li, Bingxue shi "Current-mode programmable and expandable Hamming neural network"IJCNN'99 **Date Added to IEEE Xplore:** 06 August 2002**Print ISBN:** 0-7803-5529-6

[5] Stéphane Badel, Alexandre Schmid, Yusuf Leblebici " Mixed analog-digital image processing circuit based on

Hamming artificial neural network architecture", ISCAS (5) 2004: 780-783

[6] Amit Kumar Gupta and Yash Pal Singh ,"Analysis of Hamming Network and MAXNET of Neural Network Method in the String Recognition" Proceeding in CSNT '11,International Conference on Communication Systems and Network Technologies.

[7] Mark Hudson, Beale, Demuth Hayden, De Jesús ,"Neural network Design" 2nd Edition 2002

[8] Zhi-Jian Li,Bing-Xue Shi,Bin-Qiao Li,"Hamming Neural Network circuit", US 5630021 -patent 30 Sept 1994

[9] A Schmid, Y Leblebici and D Mlynek,""A mixed analog-digital artificial neural network architecture with on-chip learning",Accepted for publication in the IEEE Transactions on VLSI System 1998

[10] A Schmid ," Neuromorphic microelectronics from devices to hardware systems and applications", Non linear Theory and its applications,IEICE Vol 7 no 4 pp 468-469 @IEICE 2016 DOI 10.1587/nolta 7.468