Design & Performance Analysis of 8-Bit Low Power Parity Preserving Carry-Look Ahead Adder

Palak Sharma[1], Amandeep Singh Bhandari[2], Dr. Charanjit Singh[3]
[1]M. Tech Student, Deptt. of Electronics and Communication Engg., Punjabi University, Patiala
[2]Assistant Professor, Deptt. of Electronics and Communication Engg., Punjabi University, Patiala
[3]Assistant Professor, Deptt. of Electronics and Communication Engg., Punjabi University, Patiala

Abstract: In the field of quantum computation, the reversible logic and nanotechnology has gathered a lot of attention of researcher's in the recent years due to its low power dissipation quality. Quantum computing has been a guiding light for nanotechnology, optical information computing, low power CMOS design, DNA computing and Low power VLSI design. Parity preserving is one of the oldest method for error correction and detection in digital system design. In this paper we proposed two parity preserving reversible 8-bit carry look ahead adder circuits. First circuit is designed usingFredkin Gates and Double Feynman (F2G) Gates, while second circuit is designed using Double Feynman (F2G) Gates and Modified Fredkin Gates. By comparing both circuits, we demonstrate that our second proposed design of reversible parity preserving circuit is optimized in terms of quantum cost and power consumption.

Keywords:*Reversible logic, Parity Preservation, Quantum Computing, Power Measurement*

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1. Introduction

Energy loss is an important consideration in digital circuit design, also known as circuit synthesis. The loss of information is associated with laws of physics describing that one bit of information lost dissipates kTln2 of energy, where k is Boltzmann' constant and T is the temperature of the system [2]. Reversibility in computing implies that information about the computational states should never be lost. The reversible logic is either physical reversible or logical reversible. Reversibility in computing implies that no information about the computational states can never be lost, so we can recover any earlier stage by computing backward or un-computing the results. This is known as logical reversibility. The benefits of logical reversibility can be gained only after employing physical reversibility. Physical reversibility is a process that dissipates no heat in terms of wastage of energy [1]. Various parameters of reversible logic gates are used to design the work.

Reversible logic gate is an n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs. A reversible gate is also defined as a bijective Boolean function from n to n values. Let the input vector be Iv, output vector Ov and they are defined as follows,

Iv = (Ii, Ii+1, Ii+2 …In-1, In) and Ov = (Oi, Oi+1, Oi+2 … On-1, On). For each particular i, there exits the relationship **Iv = Ov** [10]

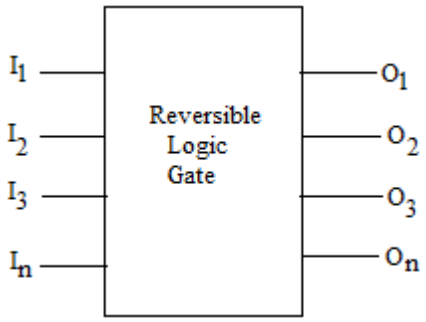

Fig. 1. Symbol of Reversible logic gate with n*n input and output

In the design of reversible logic circuits, the following points must be considered to achieve an optimized circuit.

1. Garbage outputs must be minimum.
2. Minimum delay.
3. Loops or feedbacks are not permitted.
4. Minimum quantum cost.
5. Fan-out is not permitted.

Reversible logic can be of two types they are Basic Reversible gate and Fault Tolerant Reversible Gates. Reversible gate are those gates having the same number of the input lines and the output line. While fault tolerant reversible gates are also known as the parity preserving reversible gates which perform reversible computation as well as the preserve the parity at the input side and at the output side.

2. Literature Survey

In 1961, R.Landauer described that the logical irreversibility is associated with physical irreversibility and requires a minimal heat generation per machine cycle. For irreversible logic computations, each bit of information lost generates kTlog2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. In conventional system the millions of gates used to perform logical operations. The author proved that heat dissipation avoidable if system made reversible [1].

In 1973, C.H.Bennett described that if a computation is carried out in Reversible logic zero energy dissipation is possible, as the amount of energy dissipated in a system is directly related to the number of bits erased during computation. The design that does not result in information loss is irreversible. A set of reversible gates are needed to design reversible circuit. Reversible gate can generate unique output vector from each input vector and vice-versa [2].

In 2011, Md. Mazder Rahman et al. presented a quantum gate library that consists of all possible two-qubit quantum gates which do not produce entangled states. These gates are used to reduce the quantum cost of reversible circuits. They proposed a two-qubit quantum gate library that plays a significant role in reducing the quantum cost of reversible gates [3].

In 2012, B.Raghu Kanth et al. described the comparison between the reversible and conventional logic gates. The authors compared the 4-bit reversible adder/subtractor circuit using DKG gate. The comparison is carried out in terms of low power consumption, lesser delay, number of gates, garbage outputs and constant inputs. The results of this adder/subtractor circuit using DKG gate was better as compared to existing one and this adder/subtracted circuit can be applied to the design of complex systems in nanotechnology. The authors demonstrated that a 4*4 reversible DKG gate can work singly as a reversible full adder and a reversible full subtraction [4].

In 2013, Partik Kumar Bhattdescribed the reversible comparator which is implemented with the Reversible BVN gate. The design is very useful for the future computing techniques like ultra-low power digital circuits and quantum computers. The implementation of this comparator has advantages of reducing the number of garbage outputs, gate count and number of constant input and quantum cost [5].

In 2014, A. Anjana designed the RS Flip-Flop using Reversible logic gate which is implemented by cascading the Toffoli gate and TNORG gate.By using reversible logic gates power consumption was estimated 52mW & path delay was about 6.991ns which was very less as compared to using conventional gate. The number of gates is reduced from 6 to 2 as compared to the existing module [6].

In 2014, Ashima Malhotra et al. proposed different types of reversible multiplexers using modified Fredkin gates. They proposed 2:1, 4:1, 8:1 and 16:1 reversible multiplexers. They also compared the quantum cost and power consumption of proposed reversible multiplexers with previous designs [7].

In 2014, Ashima Malhotra etal. described that reversible modified Fredkin gate used to design the multiplexers with low quantum cost and compare it with existing work. They compared the quantum cost of multiplexers design using Fredkin gate with Modified Fredkin gate used to design he multiplexers [8].

In 2015, Sukhjeet Kaur et al. proposed different types of reversible encoders using Feynman and Fredkin gates. They proposed 4:2, 8:3 and 16:4 reversible encoders. They also compared quantum cost of proposed reversible multiplexers with previous designs [10].

In 2015, Manjinder Pal Singhet al. proposed different types of reversible decoders using BVF, F2G and FRG gates. In this paper, 2:4, 3:8 and 4:16 reversible decoders were proposed. The quantum cost and hardware complexity of proposed reversible multiplexers has been reduced as compared to previous designs. The reversible logic circuits can also be designed with less area and delay [11].

In 2016, Ankush et al. described that the reversible modified Fredkin gates and modified HNG gates can be used to design the Carry Skip adder with low quantum cost. The quantum cost and the power dissipation of proposed carry skip adder design using modified Fredkin gates was reduced as compared to existing carry skip adder using Fredkin gate [12].

In 2016, Ankush et al. proposed different types of reversible residue adders using modified Fredkin gates and modified TSG gates. Variousparameters of reversible circuits such as, quantum cost and power dissipation of proposed reversible residue adderswere reduced as compared to previous designs. The reversible logic circuits can also be designed with less area and delay [14].

3. Deign of Reversible logic Gates

The various types of reversible logic gates used commonly are explained below:

3.1 Feynman Gate

Figure 2 shows the Feynman gate which is a 2*2 gate and is also called as Controlled NOT gate and it is widely used as a copying gate because fan-out is not allowed in reversible logic. The inputs (A, B) and outputs P=A, Q= A XORB. It has Quantum cost one.

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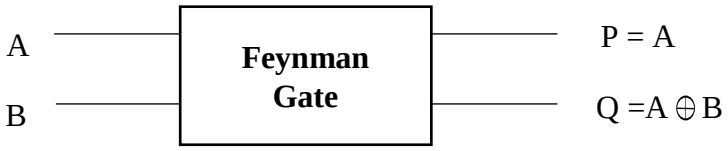

Fig.2 Feynman Gate – 2*2 gate

3.2 Feynman Double Gate (F2G)

Feynman double gate (F2G) is a 3*3 parity-preserving reversible gate. F2G gate acts as a bit copier. If B=0, it produces a copy of A in the second output. If C=0, it produces a copy of A in the third output. Quantum cost of F2G is equal to 2.

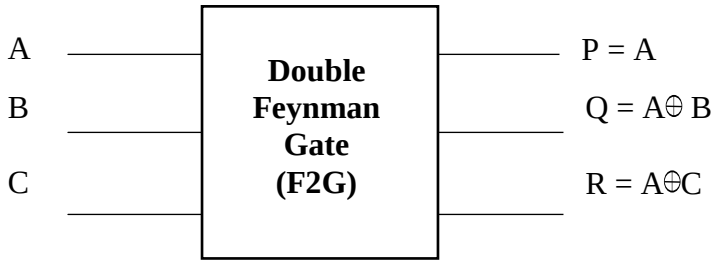

Fig. 4. Feynman Double Gate (F2G)

3.2 Fredkin Gate

Fredkin gate is 3*3 gate with input vector is I(A,B,C) and the output vector is O(P,Q,R).The output is P=A,Q=A'B+AC and R=A'C+AB. Quantum cost of Fredkin gate is 5.

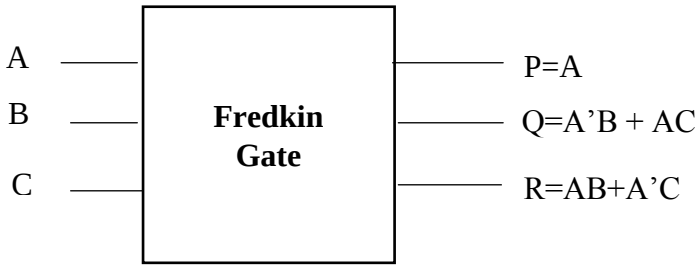

Fig. 5. Fredkin Gate – 3*3 Gate

3.3 MFRG gate

Modified Fredkin gate is 3*3 reversible gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R).The output is P=A, Q=AB'⊕ AC' and R=A'C⊕AB. Quantum cost of Modified Fredkin gate is 4.

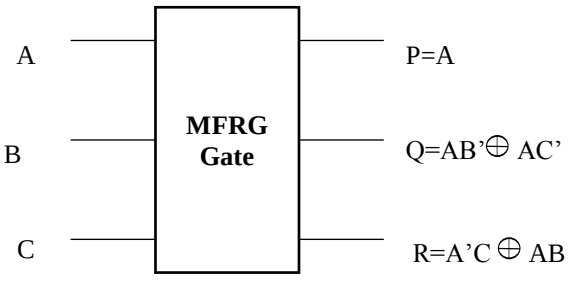

Fig. 6: MFRG Gate– 3*3 Gate

4. PROPOSED WORK

First Proposed Architecture: Parity Preserving CLA Adder Circuit using Feynman Double Gates(F2G) & Fredkin Gates (FRG)

Figure7 shows the proposed design of 8-bit parity preserving carry look ahead adder. The main idea behind the parity-preserving reversible CLA is an attempt to generate all incoming carries in parallel, without delay, avoid waiting for propagation carry and fault tolerance circuit in the stage of generating carry.

In the proposed implementation of reversible parity preservation carry look ahead adder circuit we used 20 Fredkin gates and 24 Double Feynman gates. Carry lookahead adder (CLA) circuit is one of the main processor circuits. In adder circuits, delay in propagation is a limiting factor of the circuit speed and this speed is increased along with an increase of the input bit number. If carry can be predicted, then there is no need to wait for previous full-adder carry to reach the next full adder. Thus, we use the CLA method to enable the adding operations to be done more quickly

QC (Architecture 1^{st}) = 24 QC (F2G) + 20 QC (FRG)
= 48+100
= 148

Algorithm 1^{st}: Algorithm for n-bit reversible CLA.

Input: Initial carry C0 = 0, two n-bit numbers (Xn-1,….., X2, X1, X0) and (Yn-1,….., Y2, Y1, Y0)
Output: An n-bit sum (Sn-1,….., S2, S1, and S0) and n-bit carry (Cn,…., C2, and C1)
1. Begin
2. For i ← 0 to n - 1 do
3. With the help of F2G, generate a necessary amount of Xi and C0 to calculate Si and Ci
4. Generate CI+1 with help of i + 1 FRG with Xi, Pi and Ci application
5. From generated Pi and Ci; calculate Si, for this purpose use reversible F2G and FRG
6. End.

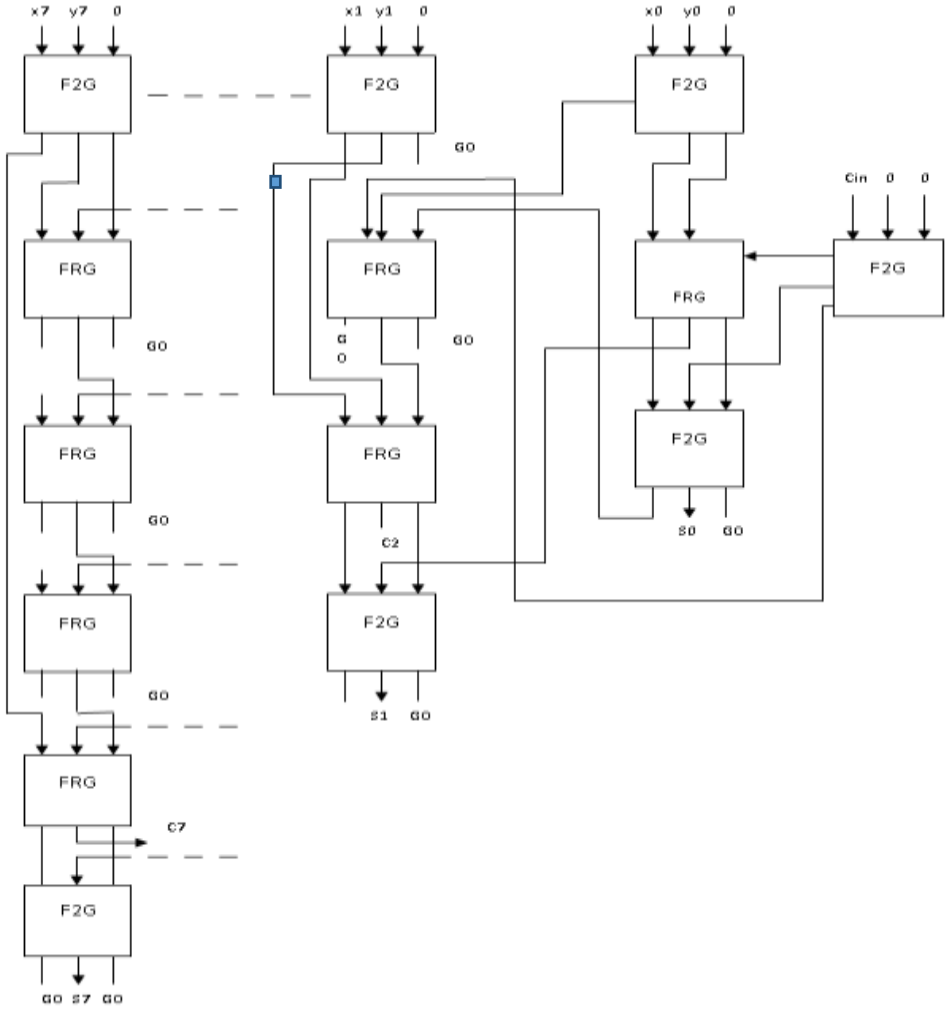

Fig. 7: First Proposed Architecture of Reversible 8-bit Parity Preserving CLA Adder Circuit

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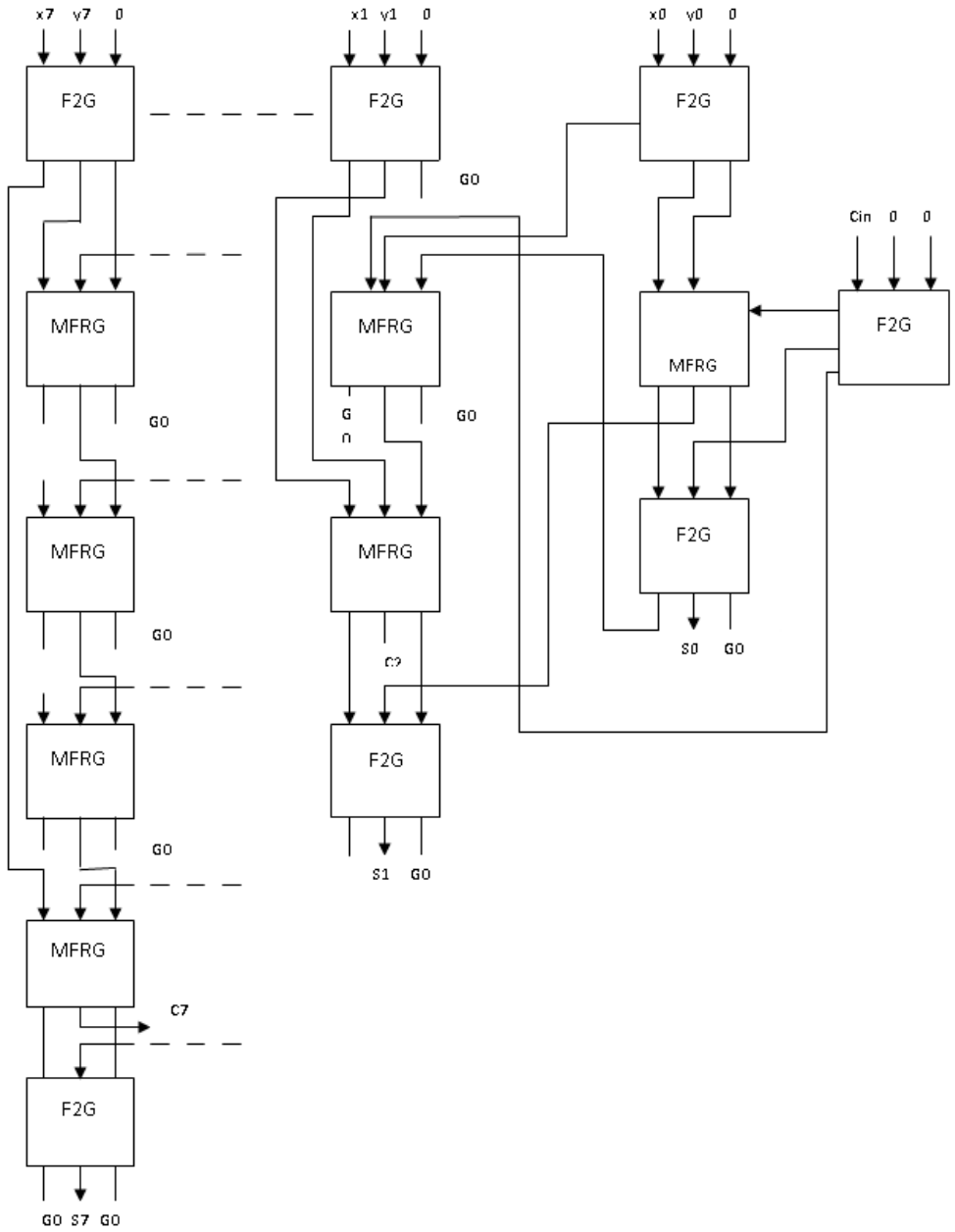

Fig. 8: Second Proposed Architecture of Reversible 8-bit Parity Preserving CLA Adder Circuit

Second Proposed Architecture: Parity Preserving CLA Adder Circuit using Feynman Double Gates (F2G) & Modified Fredkin Gates (MFRG)

Figure8 shows the proposed design of 8-bit parity preserving carry look ahead adder architecture using A sufficient condition for parity retaining in reversible circuits is that each one of the reversible gates should be capable of parity retaining. In reversible gates, if input parity is in compliance with output parity, the reversible gates will be capable of parity retaining.

The second proposed architecture CLA with 44reversible gates consists of 24 parity-preserving reversible Feynman Double(F2G) gates and 20 parity preserving Modified Fredkin (MFRG) gates. The CLA produces 32 garbage and requires 26 constant inputs. The quantum cost of this circuit is equal to 128 too, because

QC (Architecture 2^{nd}) = 24 QC (F2G) + 20 QC (MFRG)
= 48+80
= 128

Algorithm 2nd: Algorithm for n-bit reversible CLA.

Input: Initial carry C0 = 0, two n-bit numbers (Xn-1,….., X2, X1, X0) and (Yn-1,….., Y2, Y1, Y0)
Output: An n-bit sum (Sn-1,….., S2, S1, and S0) and n-bit carry (Cn,…., C2, and C1)

1. Begin
2. For i ← 0 to n - 1 do
3. With the help of F2G, generate a necessary amount of Xi and C0 to calculate Si and Ci
4. Generate CI+1 with help of i + 1 MFRG with Xi, Pi and Ci application
5. From generated Pi and Ci; calculate Si, for this purpose use reversible F2G and MFRG
6. End.

5. IMPLEMENTATION & RESULTS

Table1: Comparison of Proposed work with Existing work

Parity Preserving CLA Adder Circuit	Quantum Cost	Power Dissipation (W)
FirstProposed Architecture	148	5.88 W
SecondProposed Architecture	128	3.85 W

6. SIMULATION RESULTS

Figure9and 11 shows the RTL schematic of top module for reversible parity preserving CLA adder, it contains inputs x and y each of which contains 8 bits and Cin is the input carry. The S is the output which contains 8 bits and carry outputs Cout (1 - 7) is the output carry.Figure10and 12 shows the RTL Schematic of parity preserving circuit.

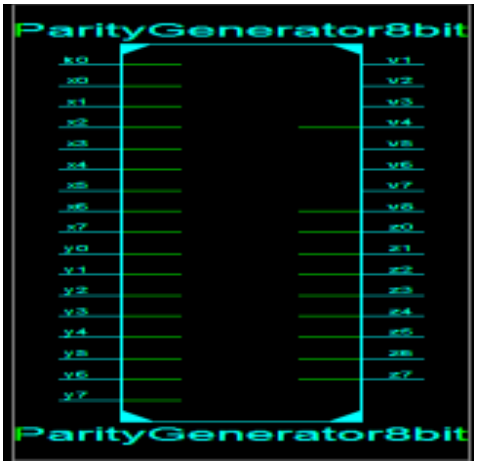

Fig. 9: RTL Schematic of 8 bit Reversible CLA Adder Circuit (FirstArchitecture)

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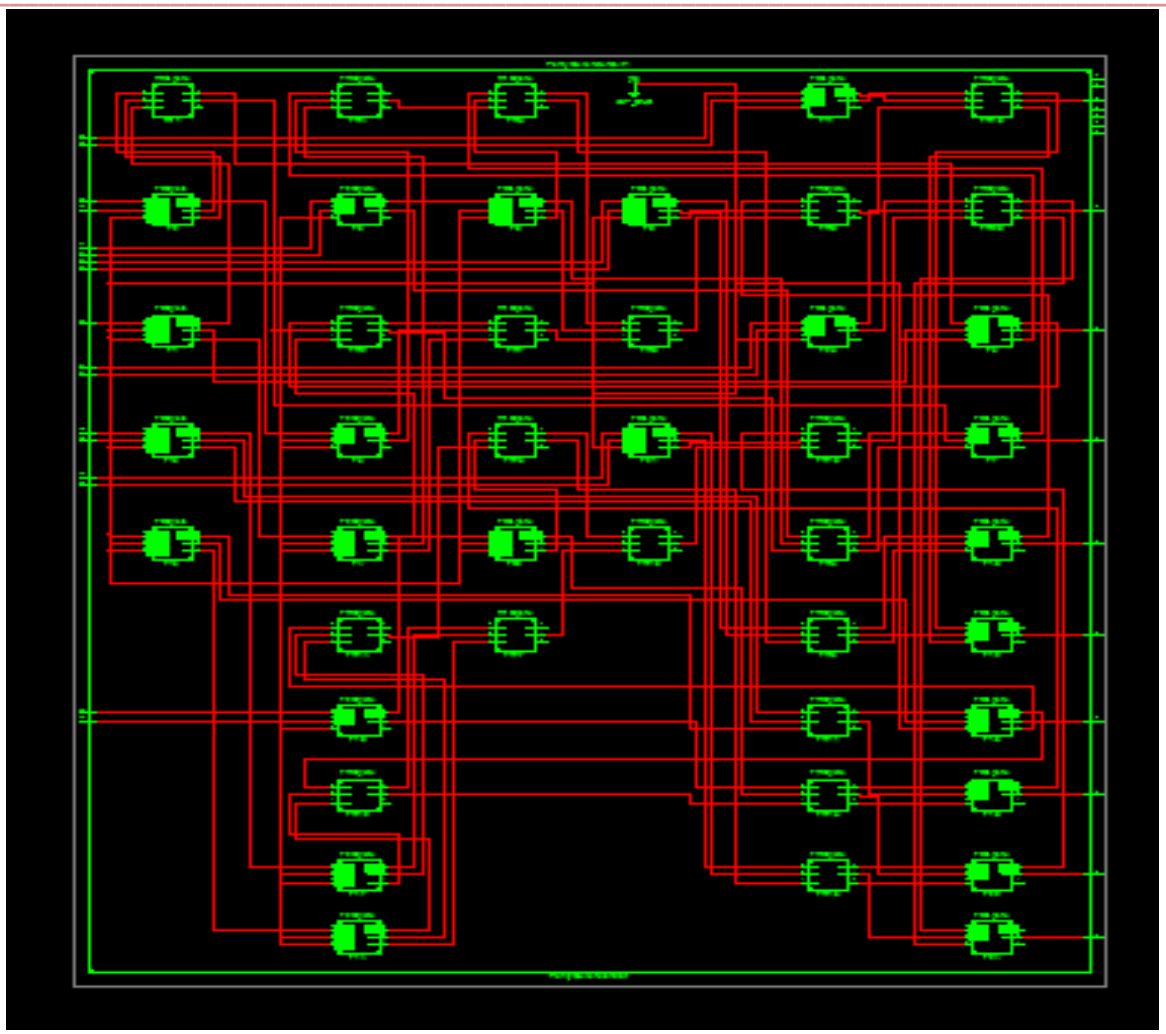

Fig. 10: RTL View of Reversible 8-bit Parity Preserving CLA adder Circuit (FirstArchitecture)

Fig. 11: RTL Schematic of 8 bit Reversible CLA Adder Circuit (SecondArchitecture)

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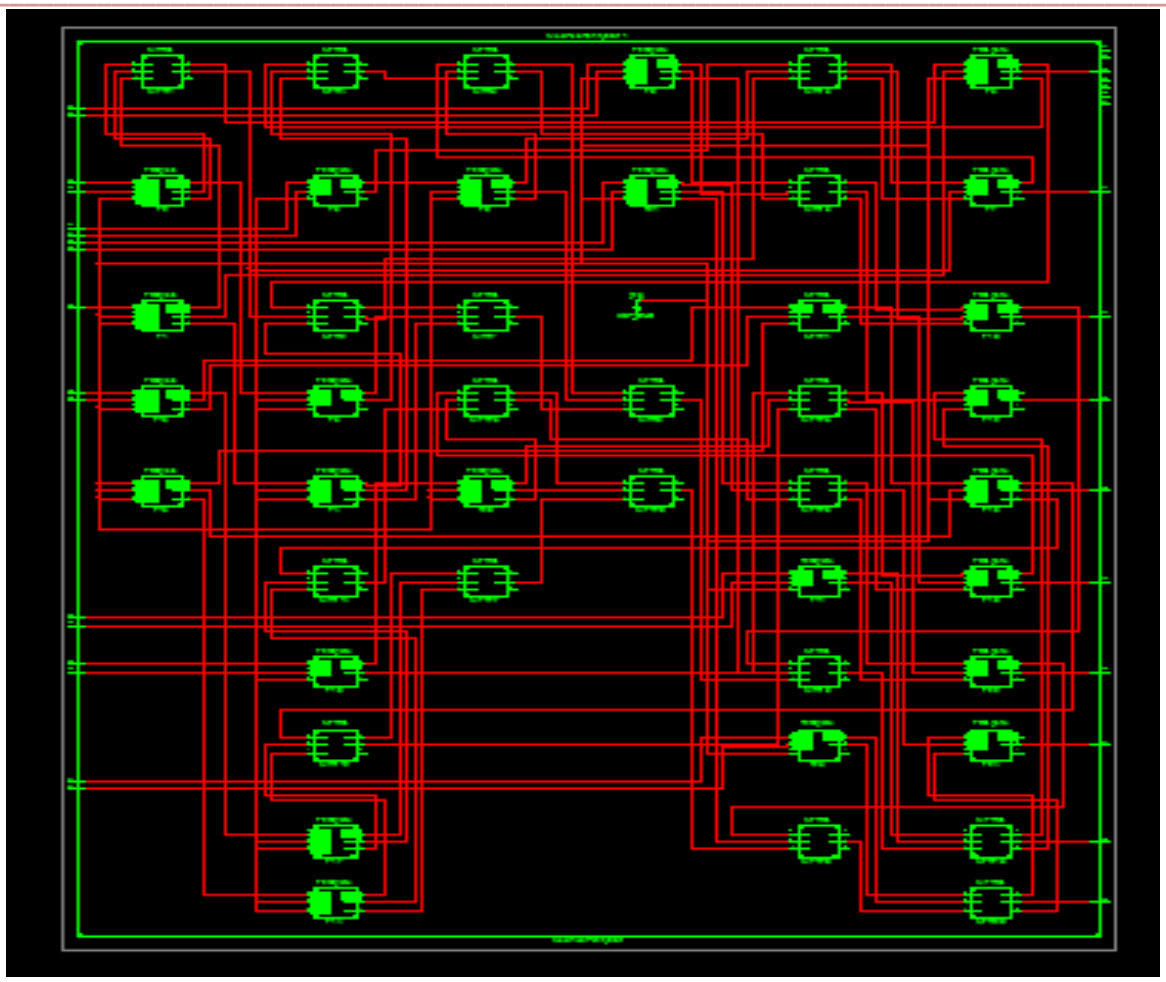

Fig. 12: RTL View of Reversible 8-bit Parity Preserving CLA adder Circuit (SecondArchitecture)

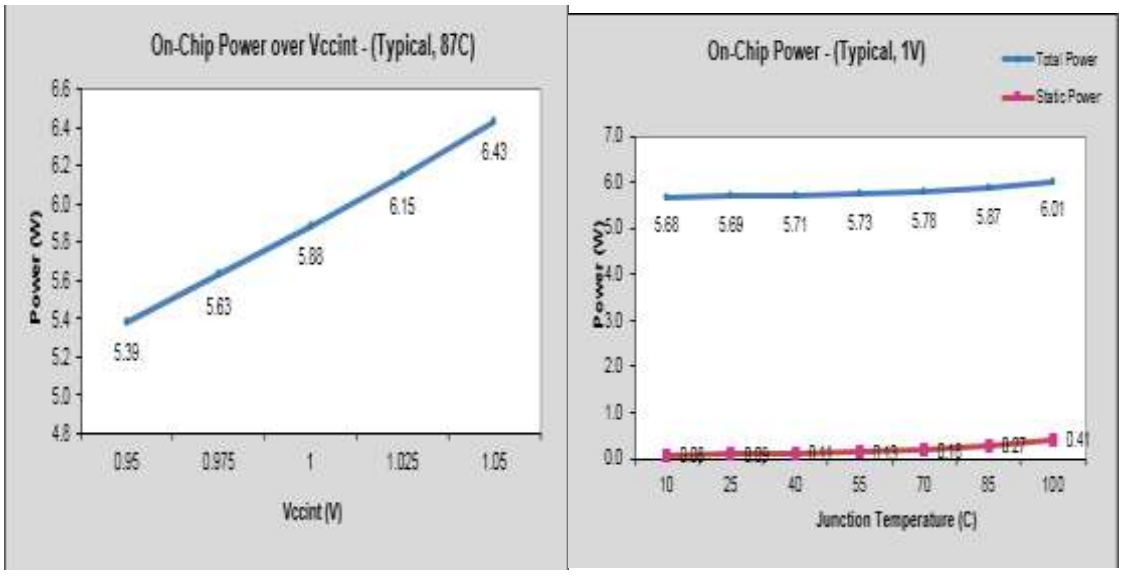

Fig. 13:Power Dissipation Graph for Proposed Reversible Parity Preserving CLA Circuit (Architecture 1st)

Figure 13shows that the maximum consumed power observed from Parity Preserving CLA Adder Circuit using Fredkin gate and Double Feynman gate is 5.88W.

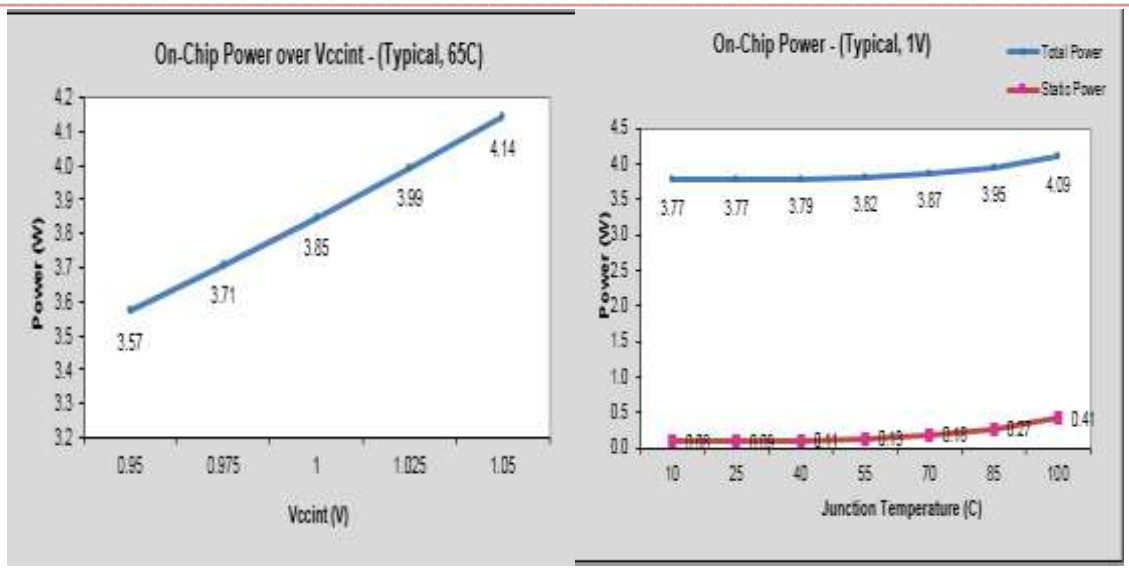

Fig.14:Power Dissipation Graph for Proposed Reversible Parity Preserving CLA Circuit (Architecture 2nd)

Figure 14shows that the maximum consumed power observed from Parity Preserving CLA Adder Circuit using Modified Fredkin gate and Double Feynman gate is 3.85W.

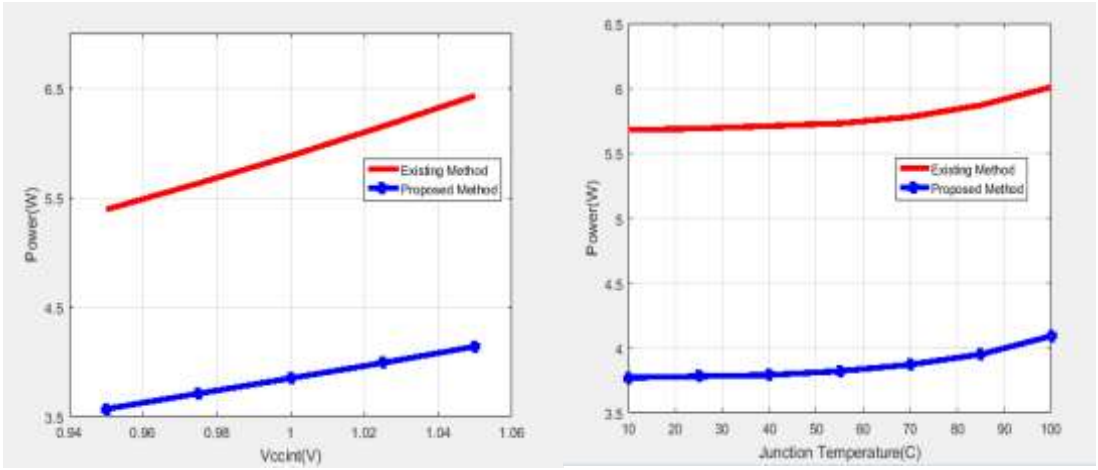

Fig. 15: Comparative Results of Power Dissipation Graph for First Proposed Architecture&Second Proposed Architecture of Reversible Parity Preserving CLA Adder Circuit

The comparative results of power dissipation graph for the first and second proposed architecture reversible parity preserving CLA adder circuit shows that the second proposed architecture consume very less power as compared to first proposed architecture. The graph between the Vcc & Power (fig. 15) shows that the second proposed architecture consumes 3.85 Watt power while the first proposed architecture consumes 5.88 Watt power.

7. CONCLUSION

In this paper, we have presented efficient designs of reversible parity preserving CLA adder primarily optimizing the parameters of Quantum Cost and Power Consumption. In the first proposed architecture,the quantum cost is 148 and power consumption is 5.88 W but in our second proposed architecture,the quantum cost is 128 and the power consumption is 3.85 W.Hence both theparameters are reduced. We conclude that the use of the specific reversible gates for a particular combinational function can be very much beneficial in minimizing the power consumption and quantum cost of the circuit. Further investigation into determining the delay & lesser area implementations can be done using logic synthesis methods.

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