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Design and Analysis of Multilevel Inverter with Reduced Number of Switches using Multicarrier SPWM Techniques

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***Abstract*—** Multi-level inverter has been widely accepted for high voltage applications. Their performance is highly superior to that of conventional two level inverter due to reduced harmonic distortion, lower electromagnetic interference and higher dc link voltages. Multi-level inverter (MLI) has some disadvantages such as increased number of components, complex pulse width modulation control method, and voltage-balancing problem. In order to increase the level of the output, the numbers of switches are increased and losses and complexity also increased. Hence to reduce these losses and complexity, a new topology is designed in this project i.e. Multi-level inverter (MLI) with reduced number of switches.

A new inverter topology has been proposed which has superior features over conventional topologies in terms of the required power switches and isolated dc supplies, control requirements and reliability. In the mentioned topology, the switching operation is separated into high- and low-frequency parts. Design and simulation analysis of new 7 level inverter topology with multicarrier spwm techniques is presented in this project thesis using MATLAB/SIMULINK

Keywords*—*MLI,SPWM.

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I. INTRODUCTION

A circuit that converts dc power into ac power at desired output voltage and frequency is called an inverter. Some industrial applications of inverters are for adjustable speed ac drives, induction heating, stand by air-craft power supplies, UPS (uninterruptible power supplies) for computers, HVDC transmission lines etc. The dc power input to the inverter is obtained from an existing power supply network or from a rotating alternator through a rectifier or a battery, fuel cell, photovoltaic array or magneto hydrodynamic (MHD) generator. The configuration of ac to dc converter and dc to ac inverter is called a dc-link converter. The rectification is carried out by standard diodes or thyristor converter circuits. Inverters can be broadly classified into two types: voltage source inverters and current source inverters[1].

II. CASCADED H-BRIDGE MULTI-LEVEL INVERTER

The smallest number of voltage levels for a multilevel inverter using cascaded inverter with SDCSs is three. To achieve a three-level waveform, a single full-bridge inverter is employed. Basically, a full-bridge inverter is known as an H-bridge cell, which is illustrated in Figure 1.5. The inverter circuit consists of four main switches and four freewheeling diodes.

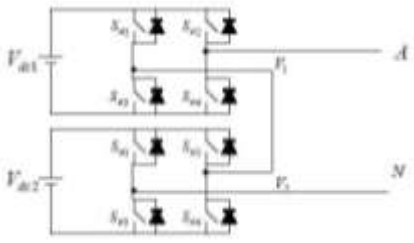

Figure 1 An H-bridge cell.

The inverter circuit consists of four main switches and four freewheeling diodes.

The cascaded H-bridge multi level inverter is to use capacitors and switches and requires less number of components in each level. This topology consists of series of power conversion cells and power can be easily scaled. The combination of capacitors and switches pair is called an H-bridge and gives the separate input DC voltage for each H-bridge. It consists of H-bridge cells and each cell can provide the three different voltages like zero, positive DC and negative DC voltages. One of the advantages of this type of multi level inverter is that it needs less number of components compared with diode clamped and flying capacitor inverters. The price and weight of the inverter are less than those of the two inverters. Soft-switching is possible by the some of the new switching methods.

Multilevel cascade inverters are used to eliminate the bulky transformer required in case of conventional multi phase inverters, clamping diodes required in case of diode clamped inverters and flying capacitors required in case of flying capacitor inverters. But these require large number of isolated voltages to supply the each cell. [1]

To synthesize a multilevel waveform, the ac output of each of the different level H-bridge cells is connected in series. The synthesized voltage waveform is, therefore, the sum of the inverter outputs. The number of output phase voltage levels in a cascaded inverter is defined by

m=2s+1……1.1

Where's' is the number of dc sources.

For example, a nine-level output phase voltage waveform can be obtained with four-separated dc sources and four H-bridge cells.

Fig 1 shows a general single-phase m-level cascaded inverter. From Fig. 2, the phase voltage is the sum of each H-bridge outputs and is given as

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$V_{AN} = V_{dc1} + V_{dc2} + + V_{dc}(s-1) + V_{dc}s$... (1.2)

Because zero voltage is common for all inverter outputs, the total level of output voltage waveform becomes 2s+1. An example phase voltage waveform for a nine-level cascaded inverter and all H-bridge cell output waveforms are shown in Fig.3. In this thesis, all dc voltages are assumed to be equal, i.e.

$V_{dc}1 = V_{dc}2 = = V_{dc}(S-1) = V_{dc}S = V_{dc}$…(1.3)

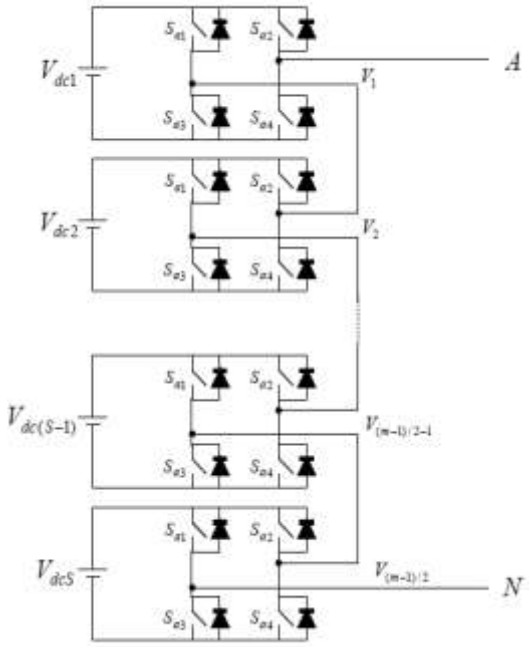

Figure 2 Single-phase configuration of an m-level cascaded inverter.

According to sinusoidal-liked waveform, each H-bridge output waveform must be quarter-symmetric as illustrated by V1 waveform in Figure2 Obviously, no even harmonic components are available in such a waveform[2,3].

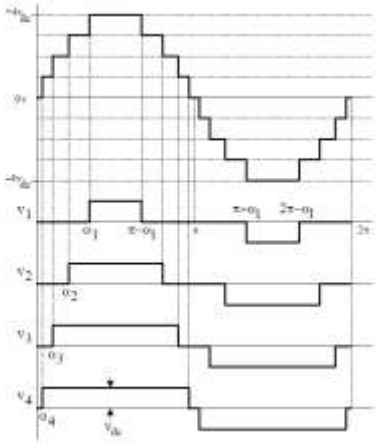

Figure 3: Waveform showing a nine-level output phase voltage and each H-bridge output voltage.

III. PROPOSED MULTILEVEL INVERTER

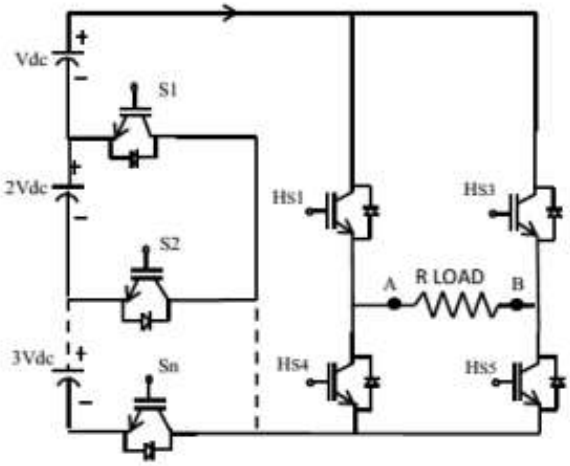

Figure 4 MLI with reduced no. of switches

3.1 Introduction

The above circuit diagram Fig 4 is a 7 level inverter with reduced number of switches. Here 12 switches which are used in cascading of 3 single level inverters is replaced with 3 high frequency switches (S1, S2, S3).The other full switches (Hs1, Hs3, Hs4, and Hs5) are polarity switches[4,5].

3.2 Switching Sequence

S1	S2	S3	HS1	HS3	HS4	HS5	Voltage Level
1	0	0	1	0	0	1	$+V_{dc}$
0	1	0	1	0	0	1	$+2V_{dc} + V_{dc}$
0	0	1	0	1	0	1	$+3V_{dc}+2V_{dc} + V_{dc}$
0	0	0	0	0	0	0	**0**
1	0	0	0	1	1	0	$-V_{dc}$
0	1	0	0	1	1	0	$-2V_{dc}- V_{dc}$
0	0	1	0	1	1	0	$-3V_{dc}-2 V_{dc}- V_{dc}$

Table1 Switching sequence of proposed multilevel inverter.

IV. Modulation Techniques

The following are the multilevel Modulation techniques.

Figure 5 Multilevel modulation techniques

Multiple Pulse Width Modulation Technique is used in three level or more than three levels. These are classified into two types: - Level Shift, Phase Shift. In this paper we used the level shifted modulation technique[6,7].

There are threedifferent types of level shifted SPWM strategies with differing phase relationships:

Phase disposition(PD)- All carrier waveforms are in phase.

Phase opposition disposition

(POD) – All carrier waveforms above zero reference are in phase and are 180^0 out of phase with those below zero.

Alternate phase disposition

(APOD) – Every carrier waveform is in out of phase with its neighbor carrier by 180^0.

4.1 PHASE DISPOSITION (PD)

In phase disposition (PD) modulation all carrier waveforms above zero reference and below zero reference are in phase.

The converter switches to - 2Vdc when the reference is lesser than 2nd negative carrier waveform. The converter switches to - 3Vdc when the reference is lesser than 3rd lowermost negative carrier waveform.

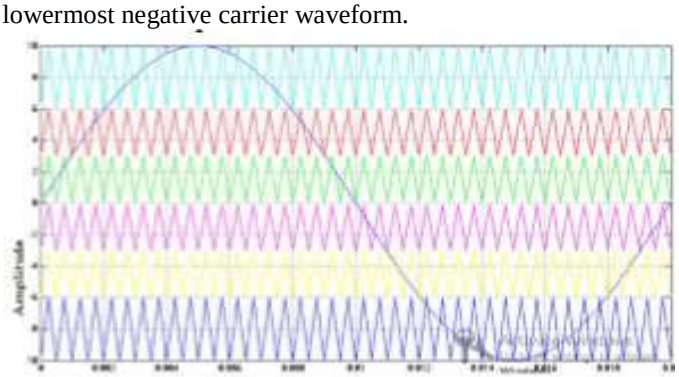

Figure 6 PD technique

For phase disposition (PD) modulation all carrier waveforms above zero reference and below zero reference are in phase.

The converter switches to +2Vdc when the reference is greater than the 2nd positive carrier waveform. The converter switches to +3Vdc when the reference is greater than the uppermost 3rd positive carrier waveform. The converter switches to 0 when the reference is lesser than all positive carrier waveforms as well as lesser than negative carrier waveforms. The converter switches to - Vdc when the reference is lesser than 1st negative carrier waveform[6,7].

4.2 PHASE OPPOSITION DISPOSITION (POD)

In phase opposition disposition (POD) modulation all carrier waveforms above zero reference are in phase and are 180 degrees out of phase with those below zero.

Carrier arrangements for PODPWM strategy The rules for the phase opposition disposition method, when the number of level N = 7 are The N –1 = 6 carrier waveforms are arranged so that all carrier waveforms above zero are in phase and are 180 degrees out of phase with those below zero. There are 3 carrier waveforms above the reference zero line and other 3 carrier waveforms with 180 degree shift are below the zero reference line. The converter switches to + Vdc when the reference is greater than 1st positive carrier waveform. The converter switches to +2Vdc when the reference is greater than the 2nd positive carrier waveform. The converter switches to +3Vdc when the reference is greater than the uppermost 3rd positive carrier waveform. The converter switches to 0 when the reference is lesser than all positive carrier waveforms as well as lesser than negative carrier waveforms.

The converter switches to - Vdc when the reference is lesser than 1st negative carrier waveform. The converter switches to - 2Vdc when the reference is lesser than 2nd negative carrier waveform. The converter switches to - 3Vdc when the reference is lesser than 3rd lowermost negative carrier waveform.

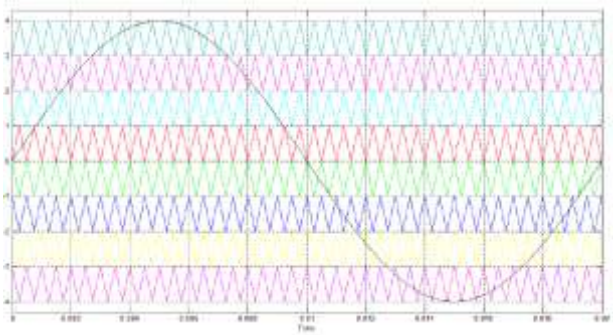

Figure 7 POD technique

For phase opposition disposition (POD) modulation all carrier waveforms above zero reference are in phase and are 180 degrees out of phase with those below zero[6,7].

4.3 ALTERNATE PHASE DISPOSITION (APOD)

In alternate phase opposition disposition (APOD) modulation, every carrier waveform is in out of phase with its neighbor carrier by 180 degrees. Carrier arrangements for APOD PWM strategy.

The rules for APOD method, when the number of levels are N = 7, then N – 1 = 6 carrier waveforms are arranged so that every carrier waveform is in out of phase with its neighbor carrier by 180 degrees.

There are 3 positive carriers whose magnitude is positive and 3 negative carriers whose magnitude is negative. The converter switches to + V_{dc} when the reference is greater than 1st positive carrier waveform. The converter switches to +2Vdc when the reference is greater than the 2nd positive carrier waveform. The converter switches to +3V_{dc} when the reference is greater than the uppermost 3rd positive carrier waveform. The converter switches to 0 when the reference is lesser than all positive carrier waveforms as well as lesser than negative carrier waveforms

The converter switches to -V_{dc} when the reference is lesser than 1st negative carrier waveform. The converter switches to - 2Vdc when the reference is lesser than 2nd negative carrier waveform. The converter switches to - 3Vdc when the reference is lesser than 3rd lowermost negative carrier waveform.

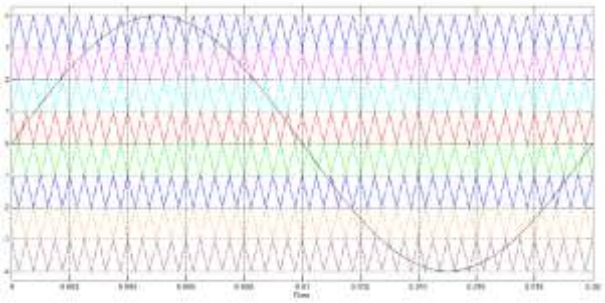

Figure 8 APOD technique

In case of alternate phase disposition (APOD) modulation, every carrier waveform is in out of phase with its neighbor carrier by 180 degrees[6,7].

V. SIMULATION DESIGN

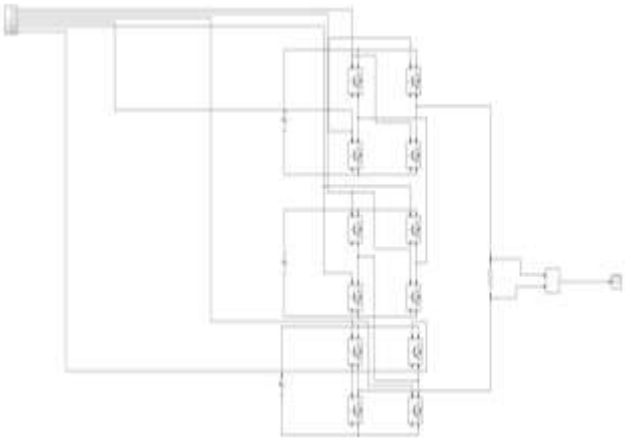

Figure 9 Level Cascaded multilevel inverter using PD, POD and APOD technique.

Components used:

1) Number of dc sources = 3
2) Number of IGBT high frequency switches = 12
3) Resistive load = 50 ohms

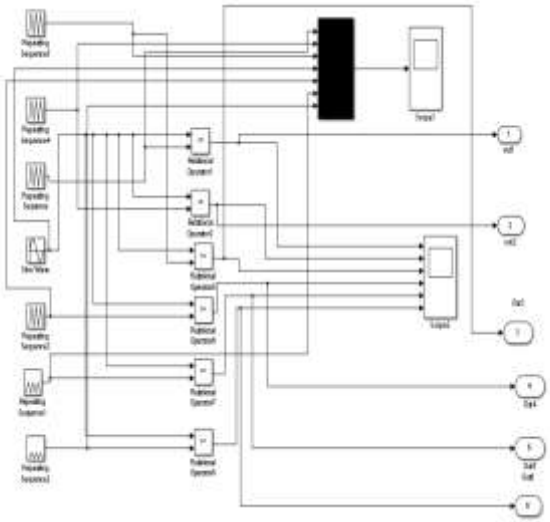

Figure 10 Subsystem of 7 Level Cascaded Multilevel inverter.

Number of repeating sequences= m-1 where 'm' is the number of levels. Here the value m is equal to 7. So, m-1=6 repeating sequences. The reference wave is a sine wave. PD,POD and APOD techniques are applied by changing the magnitude of the repeating sequences.

VI. PROPOSED DESIGN

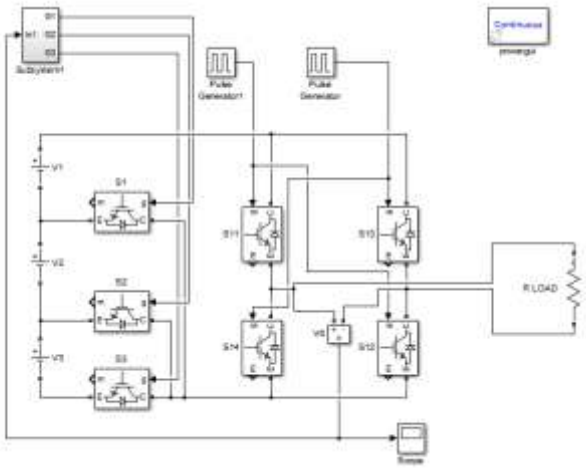

Figure 11 Proposed MLI using SPWM inverter topology.

Components used:

1) Number of dc sources = 3
2) Number of IGBT high frequency switches = 3
3) Resistive load = 50 ohms.

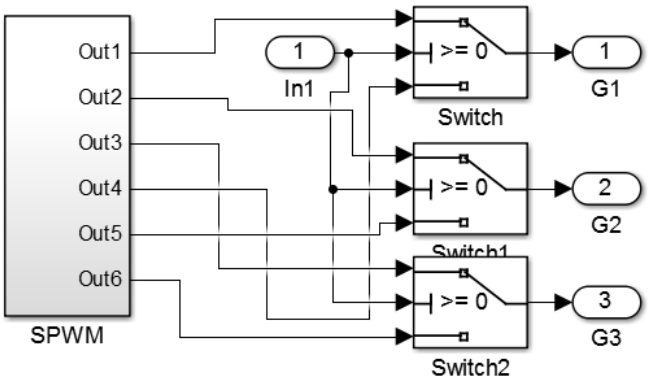

Figure 12 Sub-system of Proposed MLI using SPWM inverter topology. Depending on the polarity (+ or -) obtained from vo to the Subsystem1 the respective switches get on.

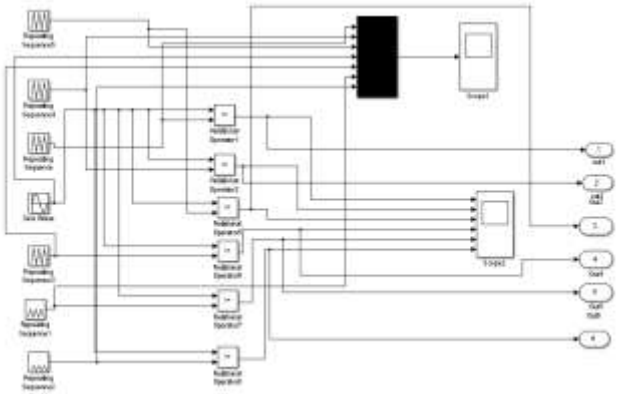

Figure13 Subsystem of SPWM block.

Number of repeating sequences= m-1 where 'm' is the number of levels. Here the value m is equal to 7. So, m-1=6. The reference wave is a sine wave. PD,POD and APOD techniques

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are applied by changing the magnitude of the repeating sequences.

4.2 Output And Thd Of 7 Level Cascaded Multilevel Inverter Using Multicarrier Spwm Techniques

4.2.1 USING PD TECHNIQUE

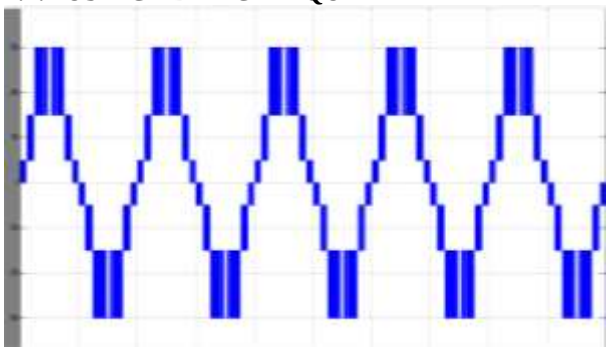


Figure14 Output waveform of 7 level cascaded multi level inverter using PD technique.

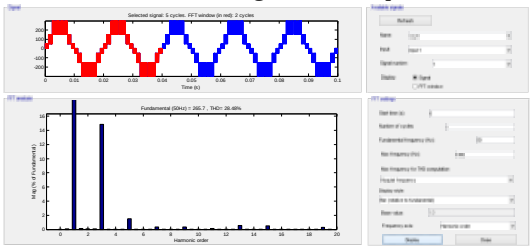


Figure15 Observed percentage of THD for 7 level cascaded multi level inverter using PD technique is 28.48%

4.2.2 USING POD TECHNIQUE

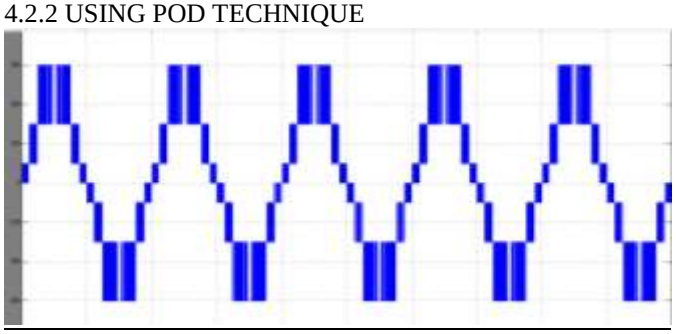


Figure16 Output waveform of 7 level cascaded multilevel inverter using POD technique.

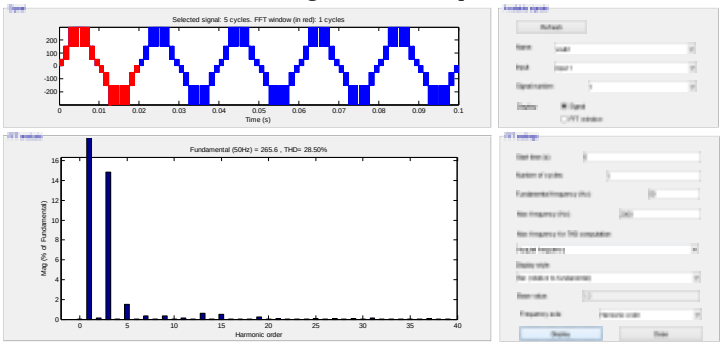


Figure17 Observed percentage of THD for of 7 level cascaded multi level inverter using POD technique is 28.50%.

4.2.3 USING APOD TECHNIQUE

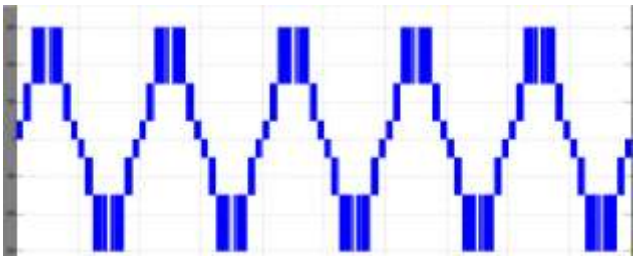
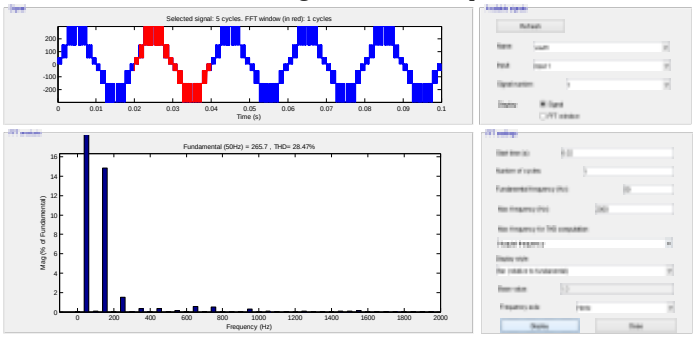


Figure18 Output waveform of 7 level cascaded multi level inverter using APOD technique.



Figur19 Observed percentage of THD for of 7 level cascaded multi level inverter using APOD technique is 28.47%.

4.3 Ouput and THD of proposed multilevel inverter with reduced number of switches using multicarrier spwm techniques:

4.3.1 USING PD TECHNIQUE

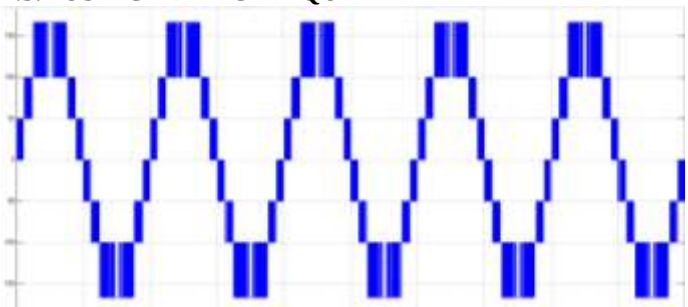


Figure20 Output waveform of 7 level new multi level inverter using PD technique.

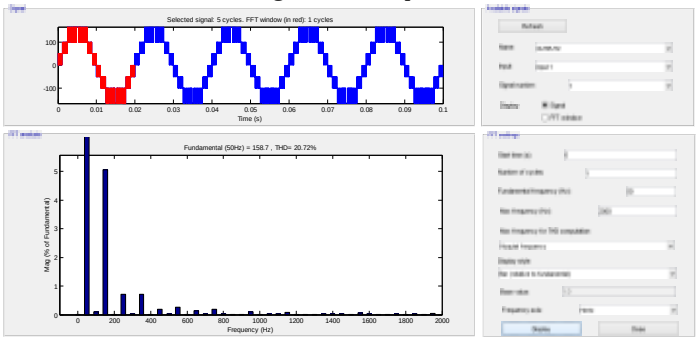


Figure21 Observed percentage of THD for of 7 level new multi level inverter using PD technique is 20.72%.

4.3.2 USING POD TECHNIQUE

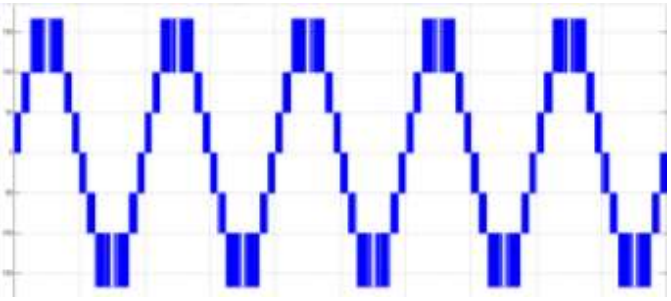


Figure22 Output waveform of 7 level new multi level inverter using POD technique.

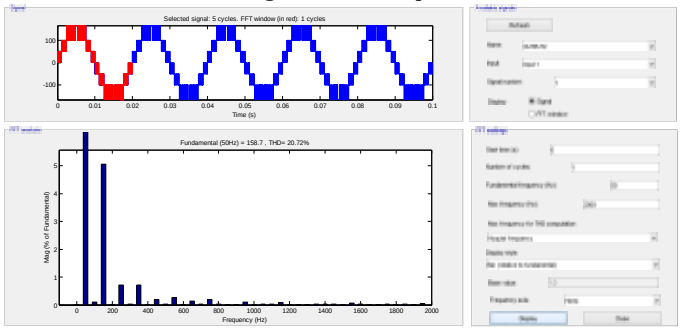


Figure23 Observed percentage of THD for of 7 level new multi level inverter using POD technique is 20.72%.

4.3.3 USING APOD TECHNIQUE

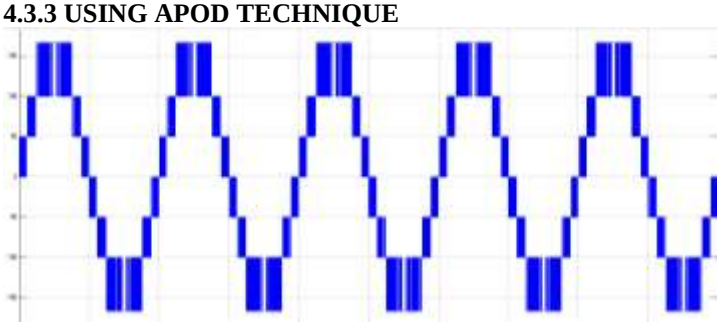


Figure24 Output waveform of 7 level new multi level inverter using APOD technique.

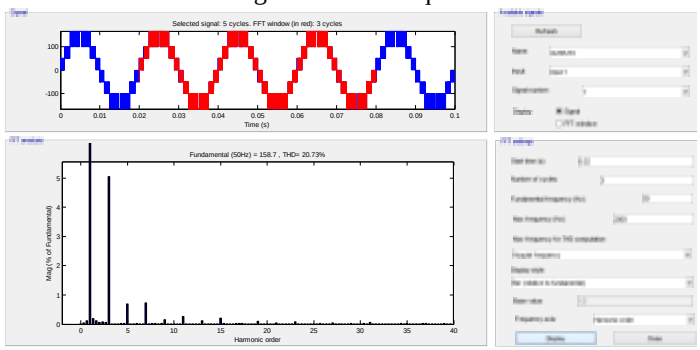


Figure 25 Observed percentage of THD for 7 Level new Multilevel inverter using APOD Technique is 20.73%

Comparison Of Conventional Multilevel Inverter With The Proposed Multilevel Inverter

S.No	Method	CONVENTIONAL MLI		PROPOSED MLI	
		% THD	No. of switches	% THD	No. of switches
1.	PD	28.48	12	20.72	3
2.	POD	28.5	12	20.72	3
3.	APOD	28.47	12	20.73	3

VII. CONCLUSION

In this paper "design and analysis of multilevel inverter with reduced number of switches using multicarrier spwm techniques" is done by using matlab/simulink software.

The following are the conclusions which we can draw from this analysis:

i. Here the number of high frequency switches have been reduced from 12 to 3 (i.e. a reduction of about 75%)
ii. This reduction in switches has not only reduced the circuit complexity but also reduced the "total harmonic distortion" as shown in our analysis.
iii. Moreover the switching losses are less which would reduce the distortions in the output waveform thereby reducing the THD,
iv. If implemented in hardware, the overall cost would be reduced by reducing the number of main switches.
v. Conduction losses would be less.

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