FPGA based High Speed ECG Signal Diagnosis for Artifacts

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Abstract—The paper is dedicated to the design of multiband digital FIR filter for removal of various interference signals present in the ECG signal which does not allow the correct diagnosis of the patient. Filtering is finding its applications in wide domains and one of those domains is the biomedical science. ECG is the electrical response of the heart with respect to time. Heart diseases especially heart attacks are way common today and to detect this very precise detailing is required. There is no scope for allowed interference level or noise which corrupts the signal. Seven band filter is designed which will remove the frequencies that are prone to disturbances i.e. the various spectral components where particular type of noise from different sources dominates like noise from power line, respiration, muscle movement etc. The filter is developed and designed in Matlab along with Xilinx DSP tools synthesized with XST using Spartan 6 and Virtex 5 as target device. Filter is optimized using DA based architecture to increase the speed and maximum area utilization is obtained. The processing speed is efficiently optimized up to 28.36% with Virtex 5 as compared to Spartan 6 with the maximum area utilization in the presented paper.

Keywords-*ECG; Interference signals; Digital filter; FIR filter; MATLAB;, FPGA*

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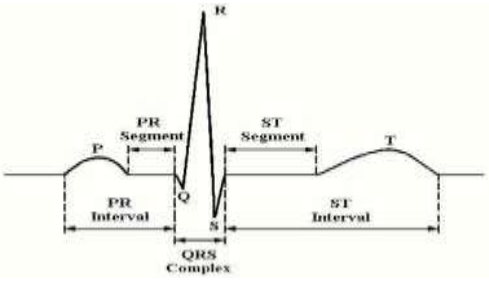
I. *INTRODUCTION*

Signal processing plays a vital role and its significance is well known in biomedical engineering. An electrocardiogram demonstrates the activity of the heart electrically and a multiband digital filter is used to analyse it [1]. Some of the features of ECG signal which are observed by physicians to monitor the condition of heart are:



Actual ECG signal [2]

Multiband digital filter is used to filter the ECG signal to get the correct clinical diagnosis of the patient's heart. When the patient is analyzed and diagnosed for heart disease it is done on the basis of ECG signal recorded. ECG is widely used to detect various abnormalities in heart rhythm, size of the heart chamber or possible damage to the heart muscle or its nervous system [3]. ECG signal of a normal heart beat consist of three parts-P wave, QRS complex and T-wave [4].But while recording the signal there are various other interference signals which corrupts the main signal. ECG which is a biomedical signal is naturally corrupt by various interferences such as 50/60Hz power line interferences (PLI) and some other biomedical signals like baseline wander, electromyogram (EMG) and electroencephalogram (EEG) [5] [6]. Patient movement, bad electrodes and improper electrode site preparation etc. are the main causes of baseline wandering. Baseline wander's range is usually below 0.5Hz [7].This may lead to serious problems such as unexpected interpretation of the signal due to different artifacts present in it. The cardiovascular disease have a major impact on human lives, so to retrieve the required information retention of ECG signal has got its own prime importance. So, we need to recover it faithfully without any distortion. An electrocardiogram is one of the painless testing applications which measure our heart beats in the electrical form. The experts then diagnose the recorded data that can be scripted on the paper or the screen [8].

The ECG signal band is from 0 to 150 Hz and the various interference signals [1] involved are: Power line interference signals with a frequency of 50 or 60 Hz which occur due to radiations from high voltage power line, improper grounding of the ECG equipment. It is a narrowband noise with bandwidth not more than 1 Hz. Noise arising from respiration having a frequency range 0.05 to 0.5 Hz which occurs due to the loose electrode connections with the chest. This is also called baseline wander noise. When the patient breathes his chest expands and contracts which also cause some disturbances. Muscle signals present with a frequency of 25 Hz occur because frequency of EMG that is below or overlap with ECG signal depends on the muscle movement rate and pressure which can be reduced by making the patient stay still and quiet so that the muscles are in relaxed state. White noise present within the ECG band.

Filters basically modifyor alter the attributes of a signal in time or frequency domain [9]. Finite Impulse Response filters are basically convolution filters i.e. the impulse response of the filter is convolved with the input bit sequence.A FIR filter's impulse response is of finite duration means it approaches to zero in finite time [10].The output of the filter depends on the present and the past input samples and not on the past output samples, that's why they does not have a

feedback structure. One of the most important properties of FIR filters is their linear phase response which allows for linear phase characteristics within the passband of the filter and not distorting the output. A basic FIR filter is characterized by the equation:

$$y(n) = \sum_{i=0}^{N-1} h(k)x(n-k) \quad (1)$$

Where

$$H(z) = \sum_{i=0}^{N-1} h(k)z^{-k} \quad (2)$$

FIR filters have various advantages. They have linear phase response and are stable filters [11, 12]. They are non-recursive filters. The design methods are generally linear. They can be implemented efficiently in hardware. They require more number of coefficients as compared to IIR filter to implement the same design but this can be overcome by using the phase symmetry property of the FIR filter. They are used when we want to exploit its linear phase property i.e. when linear response is the main requirement rather than the area constraint.

II. MATLAB BASED DESIGN SIMULATIONS

The designed filter is a seven band Least Square FIR filter [1] to remove the various interference signals mentioned. The ECG is a low frequency signal ranging from 0 to 150 Hz. The various bands in the multiband filter correspond to four stop bands. First stop band is from 0 – 0.5 Hz for removing interference signals arising from respiration. Second stop band is from 22 - 28 Hz for filtering undesired muscle signals. Third stop band is from 47 - 53 Hz for removing power line interference signals. Fourth stop bandis from 150 - 500 Hz for other interference signals out of band. Two pass bands are there - First pass band is from 0.5 – 22 Hz and Second pass band is from 28 – 47 Hz. The filter order, N is 1500. Sampling frequency is 1000 Hz. Attenuation is –40 dB. Maximum transition width is 0.9 Hz. Input word length is 16 bits and fractional length is 15 bits. Output word length is 35 bits and fractional length is 31 bits. Product wordlength and fraction length is 31 bits. Accumulator wordlength is 35 bits.

The filter was designed and simulated in Matlab. The specifications are as specified above.The filter is quantizedand the quantized response is shown in Figure 2 which shows the magnitude and the phase response. Impulse response shown in Figure 3 tells about the characteristics of the filter i.e. how the output is going to appear for a particular input. In Figure 4, the noise power spectrum graph shows the peaks of the interference signal at the different frequency points i.e. where the interference signal is present in the ECG band.

III. HARDWARE SYNTHESIS

To emphasize the extent of low hardware complexity, it is implemented on FPGA.AFPGAis anintegrated circuit which is configured or programmed by a customer in the field of experiment – hence called "field-programmable".FPGAs consist of an array of configurable logic blocks (CLB), Look Up Tables and a hierarchy of reconfigurable interconnects that enables the connection between different blocks. CLB's can be programmed to implement various logic functions. The FPGA's provide the benefit of reprogramming it again whenever we want some changes without having to replace the whole hardware and thus reducing the up gradation cost. Thus, FPGA's are very flexible to work with. The simulateddesign has been implemented in ISE environmenton various families of FPGA using VHDL language [13] and compared for the results. The design has been implemented using Distributed Arithmetic architectures with pipelining.

DA is an efficient technique for calculation of inner product or MAC operations but is serial in nature and therefore, is slow. MAC operations are implemented by multipliers very fast but they consume considerable amount of hardware. Look Up Tables constitute a very important part in DA based computations and hence DA architecture is best for FPGA implementation. Pipelined architectures leads to high speed implementation of FIR filter [14]. Our aim is to reduce the area consumption which can be achieved by Distributed arithmetic [15]. It can provide up to 80% area efficiency in the DSP designs by replacing the explicit multiplications by ROM look–ups, an efficient technique to implement on FPGA's. We are exploiting the memory in FPGA's to implement the MAC operation. In DA multiplications are reordered and rearranged so that they become distributed through the structure rather than being lumped.

Pipelining comes from the idea of a water pipe - we just continue sending the water without having to wait for it to come out. It is somewhat same as parallel processing.Pipelining is a technique you can use to increase the throughput of the FPGA. In a pipelined design, you take advantage of the parallel processing capabilities of the FPGA. Pipelining allows different functional units of a system to run concurrently.It reduces the effective critical path i.e. the minimum time required to process the new sample by introducing pipelining latches along the critical path. Pipelining cannot decrease the processing time required for a single task. The advantage of pipelining is that it increases the throughput of the system when processing a stream of tasks. It leads to a penalty in terms of an increased latency and delay latches. We introduce pipeline latches at the cutsets. It either increases the clock speed or reduces the power consumption at the same speed.Parallel processing also enhances the speed by using concurrency. The key difference is that a parallel technique distributes the tasks among the various replicated functional units. Therefore, it performs more tasks in less time but leads to more expensive resource costs.

After implementing the design in the ISE environment, we can perform timing simulation on the design. Timing simulation gives information about the time taken by a signal to travel through the gates i.e. the gate delay and the maximum frequency at which the circuit can be operated. In order to do a timing simulation, the design is implemented in a specific target device. Timing simulation allows to check that the implemented design meets all timing requirements and behaves asis expected with the device. Total number of gates in the path taken by the signal and the placement of gates in the FPGA with respect to inputs and outputs govern the total delay of the circuit. In short, delay of the circuit depends on the placement, floor planning and routing. Performing a

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thorough timing simulation ensures that the finished design is free from defects.

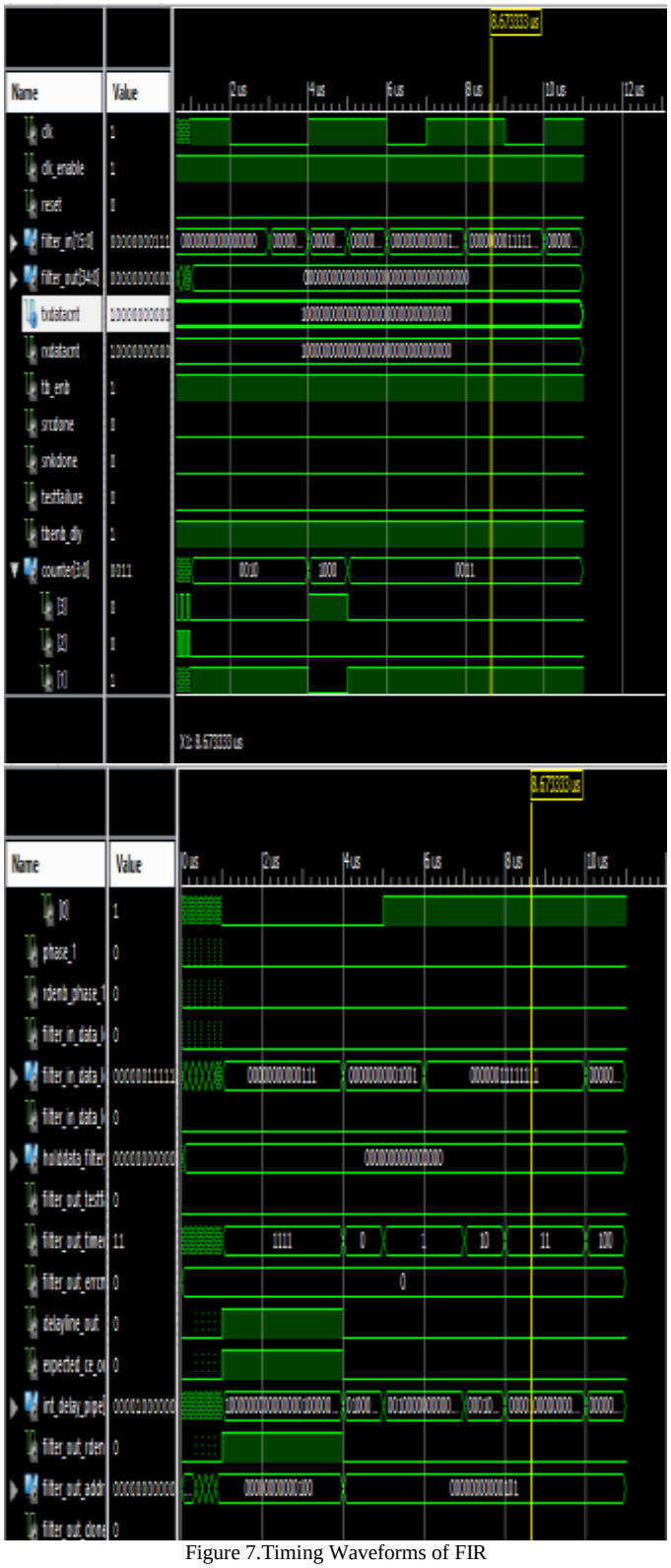

Figure 7.Timing Waveforms of FIR

IV. RESULT ANALYSIS

The various results of the proposed design implemented on Spartan 6 based xc6slx75t target device are shown in Table I and Virtex 5 based xc5vlx20t target device in Table II using Distributed Arithmetictechnique with pipeline register. Table III shows the comparison between the two implementations.

TABLE I. RESOURCE UTILIZATION USING SPARTAN 6

Device Utilization Summary			
Logic Utilization	***Used***	***Available***	***Utilization***
Number of Slice LUTs	10159	46648	21%
Number of occupied slices	3167	11662	27%
Number of fully used LUT-FF pairs	4718	10279	45%
Number of bonded IOBs	54	292	18%
Speed		201.320 MHz	

TABLE II.RESOURCE UTILIZATION USING VIRTEX 5

Device Utilization Summary			
Logic Utilization	***Used***	***Available***	***Utilization***
Number of Slice LUTs	10960	12480	88%
Number of occupied slices	2971	3120	95%
Number of fully used LUT-FF pairs	5536	11018	50%
Number of bonded IOBs	54	172	31%
Speed		281.038 MHz	

TABLE III. COMPARATIVE ANALYSIS

Logic Utilization	**Spartan 6**	**Virtex 5**
	Used	***Used***
Number of Slice LUTs	10159/46648	10960/12480
Number of occupied slices	3167/11662	2971/3120
Number of fully used LUT-FF pairs	4718/10279	5536/11018
Number of bonded IOBs	54/292	54/172
Speed	201.320 MHz	281.038 MHz

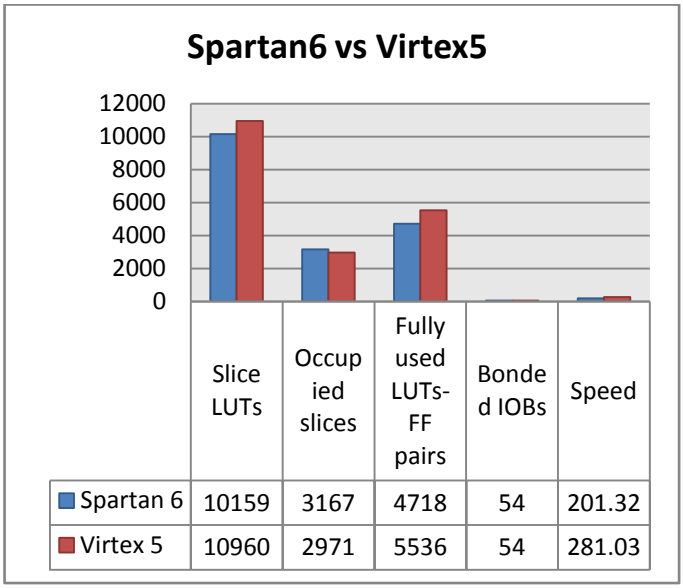

Figure 9.Comparison Bar Graph

V. CONCLUSION

In this paper, FPGA implementation of the proposed design leads to maximum area utilization and increased speed efficiency. The proposed design is implemented using DA based architecture which is being used for high speed implementations. The processing time for 10 bits word length in milliseconds is optimized to 16 bits word length in nanoseconds. The speed of the design is 281.038 MHz using Virtex 5 and 201.320 MHz using Spartan 6 as target devices. So, it can be concluded from the above results that maximum operating frequency of the proposed filter is 281.038 MHz using Virtex 5 and it also leads to maximum area utilization using DA based architecture with pipelining. Hence, a speed efficient multiband filter has been implemented on FPGA.

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