Approximate Compressors for Multiplication

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Abstract: At nanometric scales, approximate computing is an attractive prototype used for digital processing. Despite providing less accurate results, approximate computing is preferred over exact computing as it provides a fast & significant output along with low power consumption. Designing of an efficient multiplier has always been a challenge for VLSI designers as multipliers have a large area, long latency consumes considerable power. For this inconvenience compressor with low latency, low power consumption and reduced stages of the product are designed. This paper proposes two methods to design high order compressors (8:4 & 9:4) (i) Using adders (half & full) (ii) Using multiplexers in Cadence VIRTUOSO tool using 45nm technology. Extensive simulation results show that the proposed designs achieve significant accuracy improvement along with power, area, and delay reductions compared to previous compressor designs.

Keywords: *approximate computing; multipliers; high order compressors; latency; power consumption.*

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I. INTRODUCTION

Multiplication operation serves as the backbone of all signal processing applications like in DSP & Embedded systems. The speed of multiplier decides the speed of the processor. Speed attribute of any processor which involves multipliers depends on efficiency obtained in the multiplication process.

Multiplication process can be stated as repeated sum of partial products. The final product is obtained by repeatedly adding the multiplicand to itself number of times specified by another multiplier. The hardware requirements of multipliers are very high which results in low precision, increase in chip area & hardware complexity along with increased latency. To carry out time efficient multiplication, high-speed multipliers are being used that electronically computes the result by following certain logics. Due to the vast application area of multipliers, it is imperious to design a multiplier that offers low latency, consumes low power along with physically compact design.

Multiplication is intrinsically a three step process

- partial product generation
- partial product reduction
- final result computation.

As the number of bits (to be multiplied) increases the number of partial products generated also increases. However, the problem comes while multiplying high order bits as the partial products reduction have long vertical paths which leads to high latency. The most common technique used by the designers to reduce these vertical paths was by using adders. More number of stages were introduced to reduce the partial products which eventually create problems such as signal discontinuities. So the designers come up with the idea of using compressors in multipliers. Compressors serve as a critical component of a multiplier & are used in large numbers to perform the reduction process. These are combinatorial devices that provide effective partial product reduction by reducing the latency of this step by following certain logics. The performance of the multiplier can be enhanced by improving the compressor designs by lowering the transistors count that ultimately reduces the delay.

A compressor takes equally weighted inputs & produces binary outputs. More specifically an ***m:n*** compressor counts the number of ones at the inputs & provides with the binary count at the output (here ***m*** represents input bits & ***n*** represents output bits). The weight of the LSB of the compressor output is the same as the weight of each of the inputs, and the remaining bits have increasingly higher weights.

Depending on the bits converted, compressors are classified into two classes low order compressors (such as 3-2, 4-2, 5-2) [3] & high order compressors (such as 5-3, 6-3, 7-3, 8-4, 9-4). In this paper, two designs of high order compressor (8-4 & 9-4) one using half & full adders & other using multiplexers are being designed & analyzed & their performance matrices such as power, delay & area are compared with the present technical designs.

II. PROPOSED DESIGN OF COMPRESSOR

In this section, two designs are presented to design 8-4 & 9-4 compressors in 45nm technology using Cadence tool. The first design is by using adders & another design is by using multiplexers. Both the high order compressor's designs show

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much better results regarding delay, area & power as compared to the traditional designs[1].

A. Design 1 : 8-4 & 9-4 compressors using adders

Figure 1 shows the schematic of 8-4 compressor designed using half adders & full adders. An 8-4 compressor has eight inputs (i0-i7) & produces four outputs (X1-X4) i.e. it compresses eight partial products into four. If all the input bits are one (i.e. 11111111), then the output will be 1000. It demonstrates that output is the binary equivalent of the inputs. It uses three stages of half & full adders to compress the inputs by applying all sum **o**utputs of the first stage to one adder of the second stage & all carry outputs to another adder. The set of equations (1-4) shown below governs the process.

$$X1 = a \oplus c \oplus e \quad (1)$$

$$X2 = \big((ac)|(ae)|(ce)\big) \oplus (b \oplus d \oplus f) \quad (2)$$

$$X3 = \Big(\big((ac)|(ae)|(ce)\big) \cdot (b \oplus d \oplus f)\Big) \oplus \big((bd)|(bf)|(df)\big) \quad (3)$$

$$X4 = \Big(\big((ac)|(ae)|(ce)\big) \cdot (b \oplus d \oplus f)\Big) \cdot \big((bd)|(bf)|(df)\big) \quad (4)$$

where :

$$a = I0 \oplus I1;\ B = I0 \cdot I1;$$
$$c = I2 \oplus I3 \oplus I4$$
$$d = \big((I2 \cdot I3)|I2 \cdot I4|(I3 \cdot I4)\big);$$
$$e = I5 \oplus I6 \oplus I7$$
$$f = ((I5 \cdot I6)|(I5 \cdot I7)|(I6 \cdot I7))$$

Figure 2 shows the schematic of the 9-4 compressor using three stages of adders. It takes nine inputs (I0-I8) & compresses to 4 outputs (X1-X4) following a set of equations (5-8). In 9-4 compressors, if all the inputs are high i.e. I0-I8 are high (11111111) then maximum output (X1-X4) will be 1001. The proposed 9-4 compressor uses a combination of 5 full adders &half adders. The total number of adders used in the proposed design are much less as compared to the number of adders used in low order compressors as in low order, the number of components increases progressively with the input bits to be compressed. So the number of stages decides the performance characteristics such as delay, area, power consumption.

$$X1 = a \oplus c \oplus e \quad (5)$$

$$X2 = \big((ac)|(ae)|(ce)\big) \oplus (b \oplus d \oplus f) \quad (6)$$

$$X3 = \Big(\big((ac)|(ae)|(ce)\big) \cdot (b \oplus d \oplus f)\Big) \oplus \big((bd)|(bf)|(df)\big) \quad (7)$$

$$X4 = \Big(\big((ac)|(ae)|(ce)\big) \cdot (b \oplus d \oplus f)\Big) \cdot \big((bd)|(bf)|(df)\big) \quad (8)$$

where :

$$a = I0 \oplus I1 \oplus I2;$$
$$b = ((I0 \cdot I1)|((I0 \cdot I2)|((I1 \cdot I2);$$
$$c = I3 \oplus I4 \oplus I5;$$
$$d = \big((I3 \cdot I4)|I3 \cdot I5|(I4 \cdot I5)\big);$$
$$e = I6 \oplus I7 \oplus I8;$$
$$f = ((I6 \cdot I7)|(I6 \cdot I8)|(I7 \cdot I8))$$

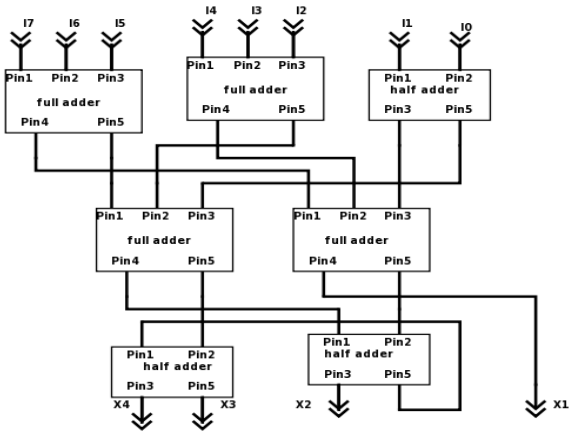

Figure 1. Schematic of 8-4 compressor using adders

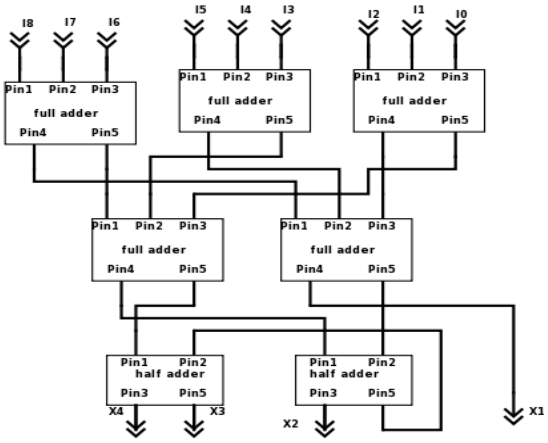

Figure 2. Schematic of 9-4 compressor using adders

B. Design II: 8-4 & 9-4 Compressors using multiplexers

Although compressors built using adders shows much improvement over conventional ones, the performance can be further enhanced using multiplexers instead of adders. Figure 3 & 4 shows the schematic of 8-4 & 9-4 compressors designed using multiplexers respectively. As the select lines control multiplexer's operations, so the required part of the structure can be made active & rest can be set in ideal mode. This feature serves as a significant advantage in reducing the power consumption of the circuit along with critical path delay reduction.

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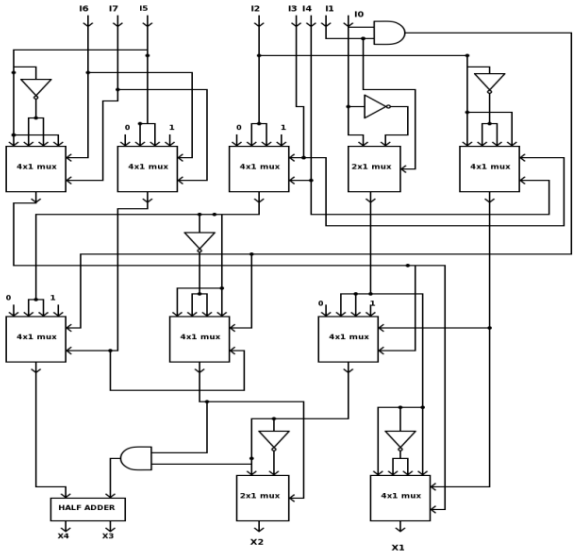

Figure 3. Schematic diagram of 8-4 compressor using multiplexers

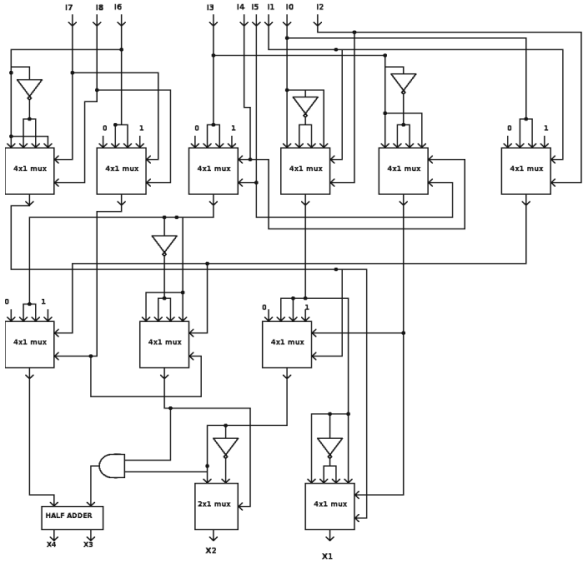

Figure 4 Schematic of 9-4 compressor using multiplexer

III. Simulation & Results

In this section, the proposed 8-4 & 9-4 compressors designs depicted in section II are analyzed & compared with the traditional designs. For analyzing power, delay & area, the designs are implemented in 45 nm CMOS technology using Cadence Virtuoso tool. The simulation results obtained are discussed using tabular comparison.

Figure 5 shows the simulation results of the 8-4 compressor with inputs from I0-I7 & output from X1-X4.

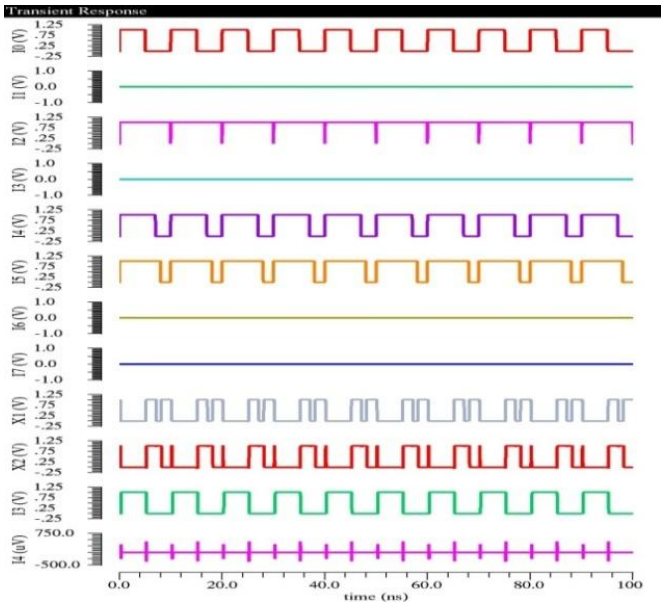

Figure 5. Output waveform of 8-4 compressor using adders

Figure 6 shows the simulated waveform of 9-4 compressor designed using adders with inputs from I0-I8 & output from X1-X4.

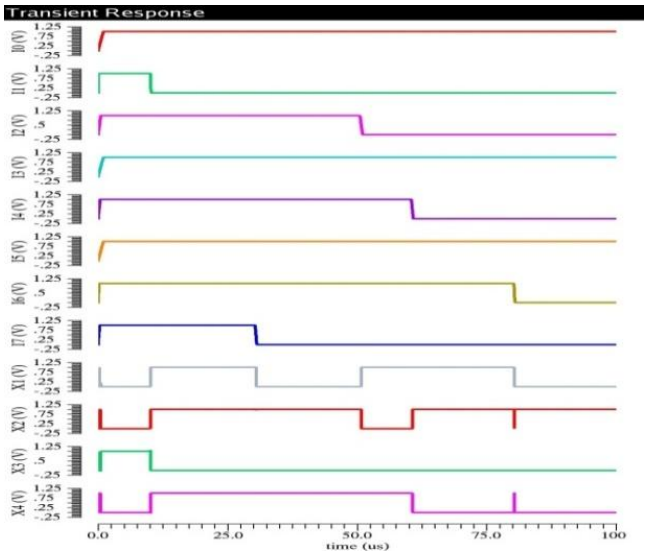

Figure 6. Output waveform of 9-4 compressor using adders

Figure 7 shows the output waveform of the 8-4 compressor using multiplexers with inputs from I0-I7 & output from X1-X4.

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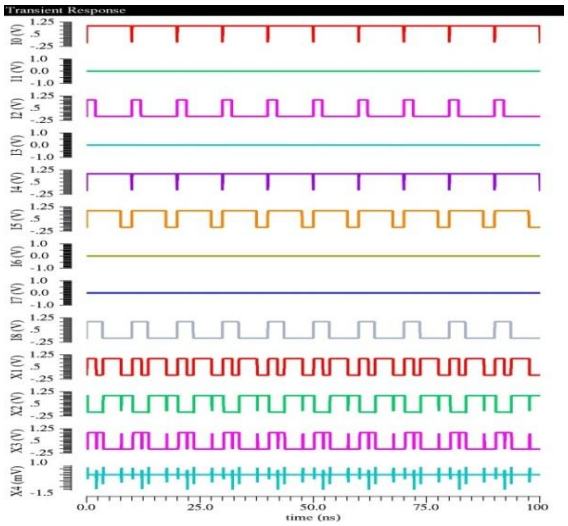

Figure 7. Output waveform of 8-4 compressor using multiplexers

Figure 8 shows the output waveform of the 9-4 compressor using multiplexers with inputs from I0-I8 & output from X1-X4.

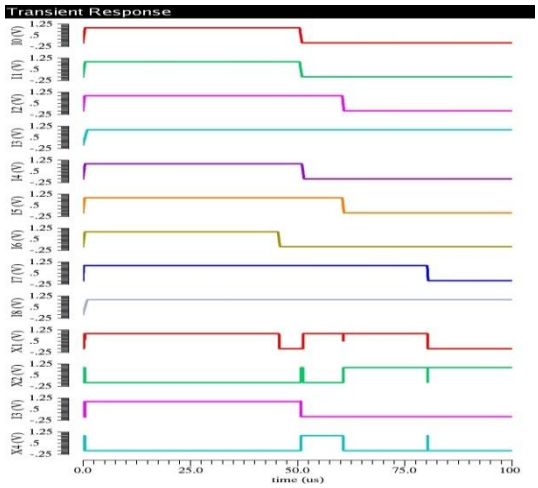

Figure 8. Output waveform of 9-4 compressor using multiplexers

Table 1 describes the performance comparison of the proposed 8-4 & 9-4 compressors with the previous results where it depicts the superiority of the proposed work over the traditional design in terms of power, delay & area.

TABLE I. Performance Comparision Of 8-4 & 9-4 Compressors

	8-4 compressor				**9-4 compressor**			
PARAMETERS	***Using half & full adders***		***Using multiplexers***		***Using half & full adders***		***Using multiplexers***	
	Previous results [1]	***Proposed design results***	***Previous results [1]***	***Proposed design results***	***Previous results [1]***	***Proposed design results***	***Previous results [1]***	***Proposed design results***
POWER(nW)	18276.250	1037	15263.603	2628	21848.218	837.4	15459.456	3018
AREA(um^2)	93.139	21.60	110.779	91.91	102.1900	36.00	112.190	107.72
DELAY(ps)	1028	5.167	1071	5.239	1082	5.180	1077	5.166

IV. CONCLUSION

To speed up multipliers such as Dadda[5], Wallace tree, Booth, compressors are the key in partial product reduction. The use of compressors in the multipliers not only reduces the vertical critical path but also reduce the stage operations simultaneously. To show better improvement, two different designing process has been explored (one using adders & other using multiplexers in the circuitry) in 45 nm technology using Cadence Virtuoso tool. The simulation results demonstrate considerable improvement regarding delay, area & power over conventional 8-4 & 9-4 compressor designs.

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