Design of High Speed Carry Select Adder using Spurious Power Suppression Technique

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***Abstract*:-** Design of a compact, power efficient and high speed digital adder is one of the most extensive research area in VLSI Design. One of the goals is to increase speed which can be achieved by reducing the propagation delay. Carry Select adder (CSLA) is the most demanding adder which is utilized in data processing systems to achieve fast arithmetic results. Still there is scope for reducing the power consumption, area and delay in the existing designs of CSLAs. In this paper, an easy and competent technique has been used to achieve the same which includes designing of SPST based carry select adder comprising of detection unit and signed extension circuit. Adders being the most important building block of multiplier, will also enhance its performance.

Keywords: *Carry Select Adder, SPST, Detection Unit, Verilog.*

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Introduction

Adders are an essential part of most digital designs. They are employed almost everywhere from basic to complex DSP applications[3]. These adders can be designed for any numerical radix e.g. binary, decimal, hexadecimal. Based on designs, adders can be of different types. The most widely used adders are carry look-ahead adder (CLA), carry select/skip adder and carry save adder (CSA) for their operating speed.

CSLA is utilized in various computations based systems to improve the speed of carry propagation by fast generation and selection of carry to attain the sum[3]. This carry select adder (CSLA) consists of a set of two ripple carry adders (RCA) to produce carry and partial sum by taking into consideration Cinas 0/1, then the resultant carry and sum are picked by the multiplexer.

SPST Technique

SPST is one of the proficient low power VLSI techniques to minimize the unwanted switching activities to reduce power dissipation in the circuits[2][6]. It consists of a Pre-computation logic unit which splits the data range of arithmetic units in two categories, depending on whether it affects the results or not. When a part of MSB data doesn't influence the final result, it is stored by latch cicuit of SPST adder to evade unwanted switching activities occuring inside the multipliers or adders which contributes in power reduction to a large extent[8].

Carry Select Adder

A particular way of adding more than two binary numbers is Carry Select Adder (CSLA). The CSLA is a simple and faster adder, consisting of ripple carry adders (RCA) and multiplexers resulting in larger area[1]. The structure of a 4-bit CSLA is shown in fig 1. Cin is "0" for upper adder and "1" for lower adder. Input carry from the previous segment selects one of these two RCAs. If the Cin is zero or one respectively, the sum and Cout of upper adder and lower adder are selected.

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In CSLA, addition of two n-bit numbers is done with two RCAs; one considering Cin as '0' and other as '1'. The results are given as input to 2:1 multiplexer with actual carry taken as select line[7].

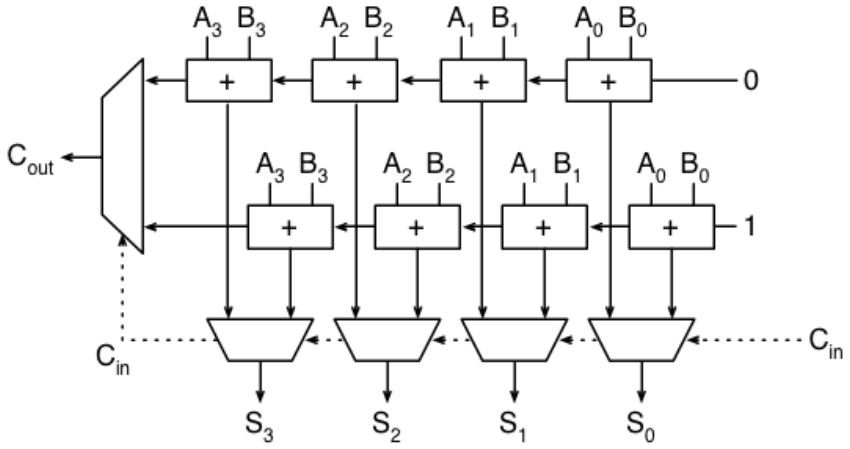

Fig 1:Carry Select Adder

Proposed Carry Select Adder

In modified carry select aadder, technique named as Spurious Power suppression technique has been used. In this SPST carry select adder, a detection unit is used to avoid unwanted MSB carry[5]. By using this technique, signed binary numbers can also be added by CSLA with the help of sign extension unit of this adder . The proposed adder shown in fig 2 is madeup of two blocks, one for MSB's known as Most Significant Part (MSP) and the another for LSB's known as the Least Significant Part (LSP).The LSP adder is implemented like a conventional adder.

MSP differs from the presented design of adder and is modified with the help of pre-computation logic circuits, latches to store unwanted carry and a sign extension circuit. Pre-computation or detection logic provides three outputs as close, carry_ ctrl and sign[7].

• **Close** - Used to turn on/off the MSP circuits.

• **Carry_Ctrl** - Represents the (n/2)+1th bit from the LSB of an 'n' bit adder.

• **Sign** - Represents the remaining (n/2-1) MSP bits of an 'n' bit adder[4].

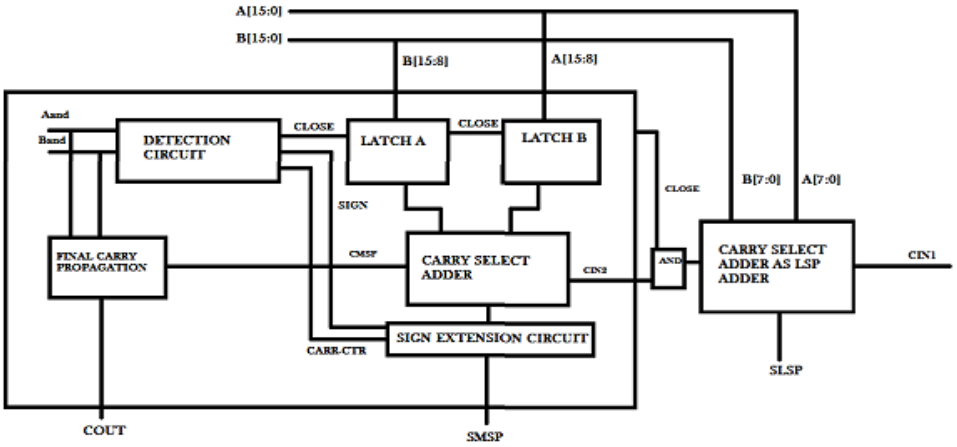

Fig 2: Carry Select Adder using SPST

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Implementation Design

The conventional CSLA and proposed SPST based CSLA have been implemented on Xilinx 14.7 using Verilog. The schematics of these two adders are summerised as follows:

Carry Select Adder:

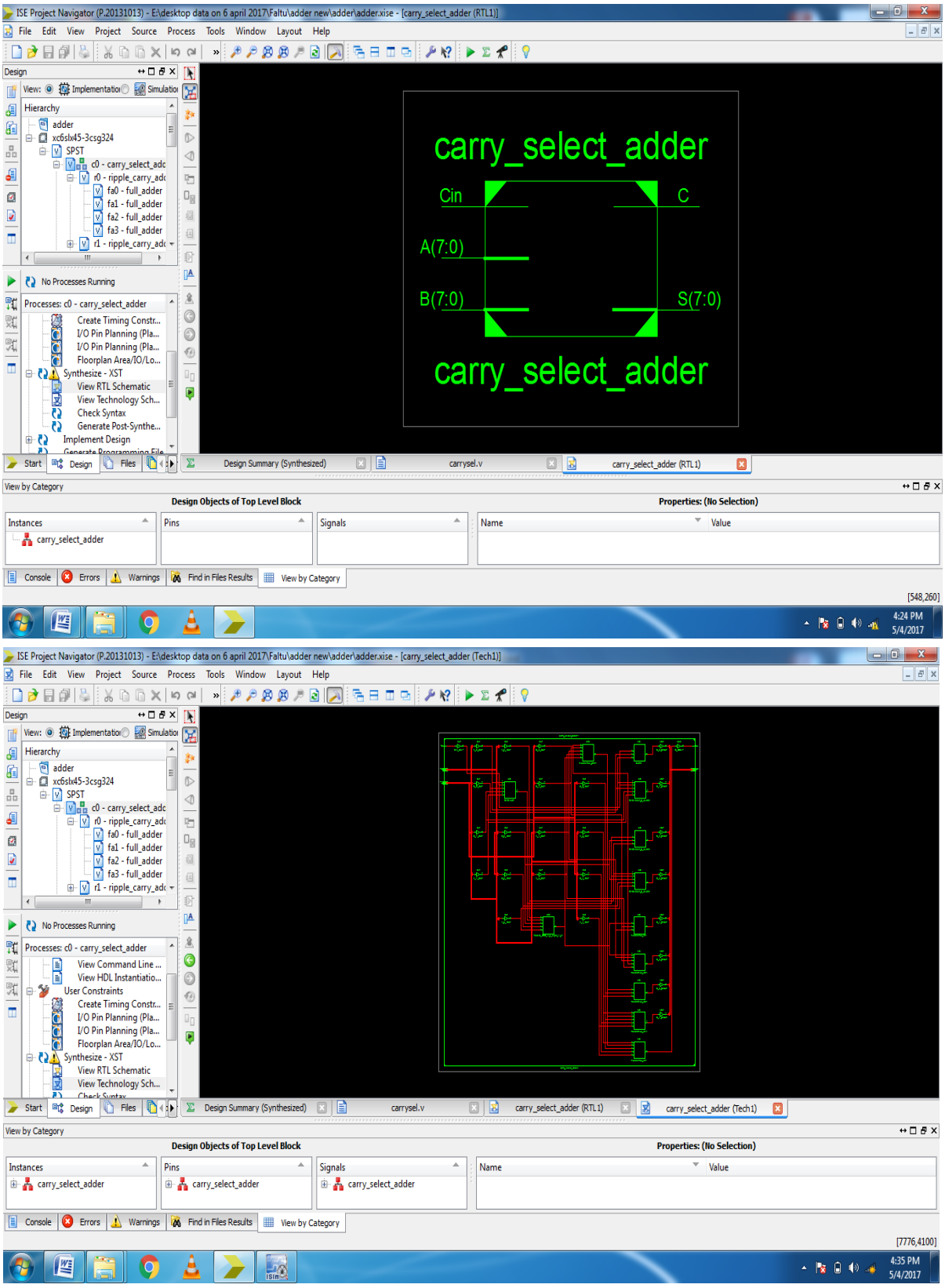

Fig 3: RTL and Technology Schematic diagram of CSLA

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SPST based Carry Select Adder :

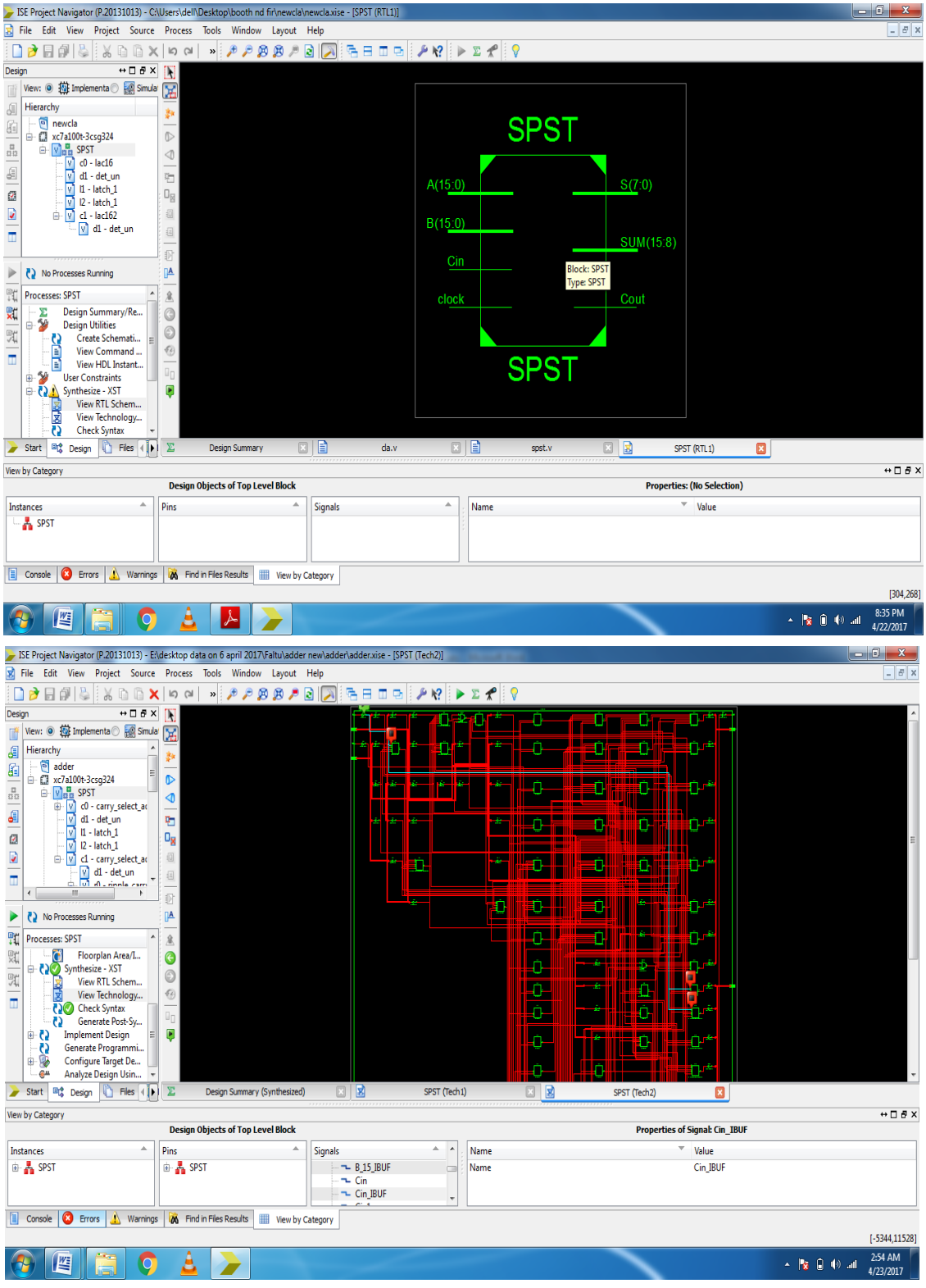

Fig 4: RTL and Technology Schematic Diagram of SPST based CSLA

Simulation Results

Output waveforms of conventional CSLA and SPST based CSLA for unsigned & signed numbers are shown in fig 5 and fig 6. Table 1 shows comparision between the parameters as area, power and delay; of these two adders.

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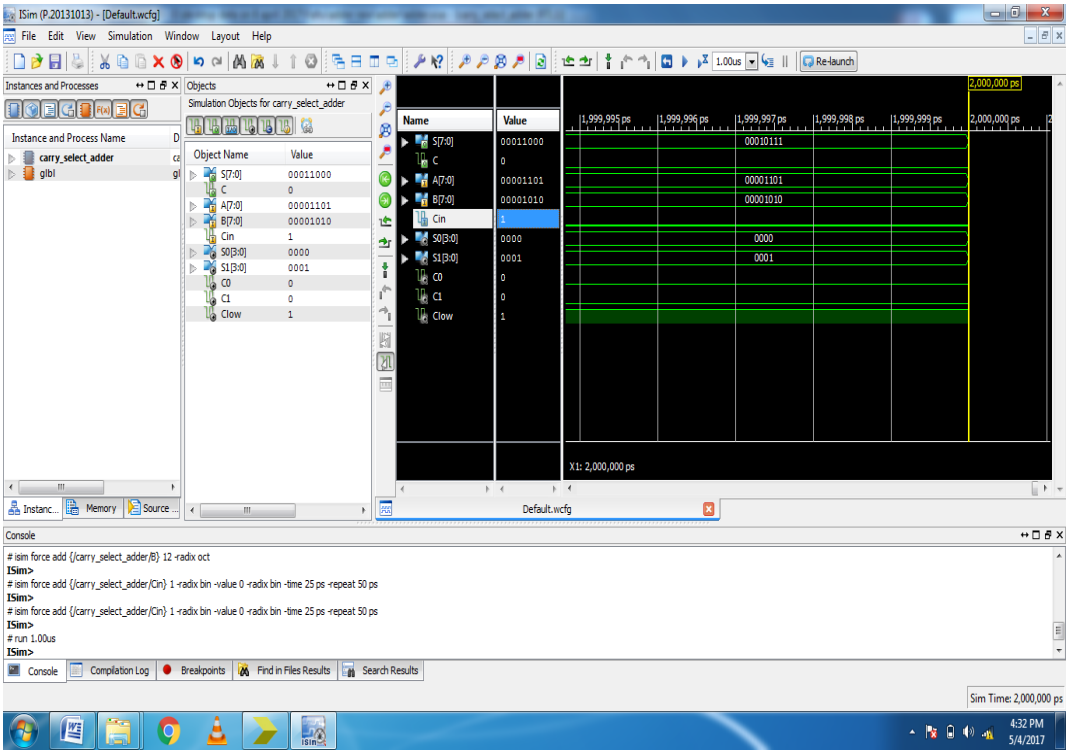
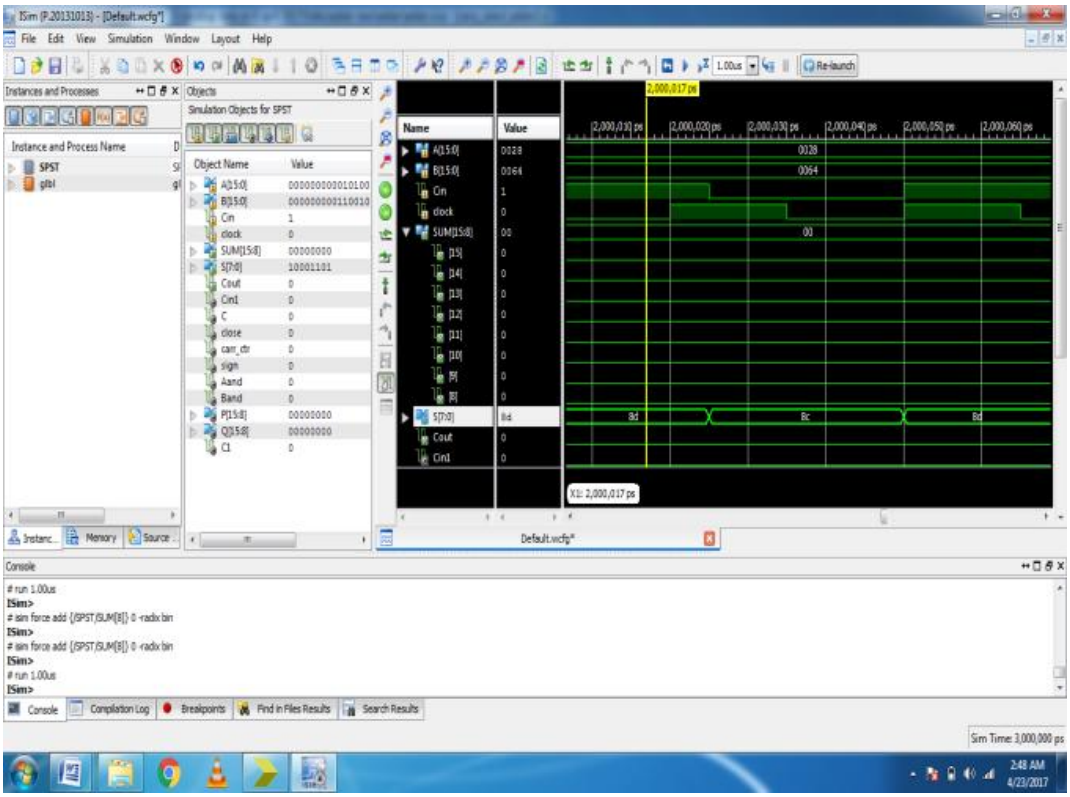


Fig 5: Output Waveform of conventional CSLA



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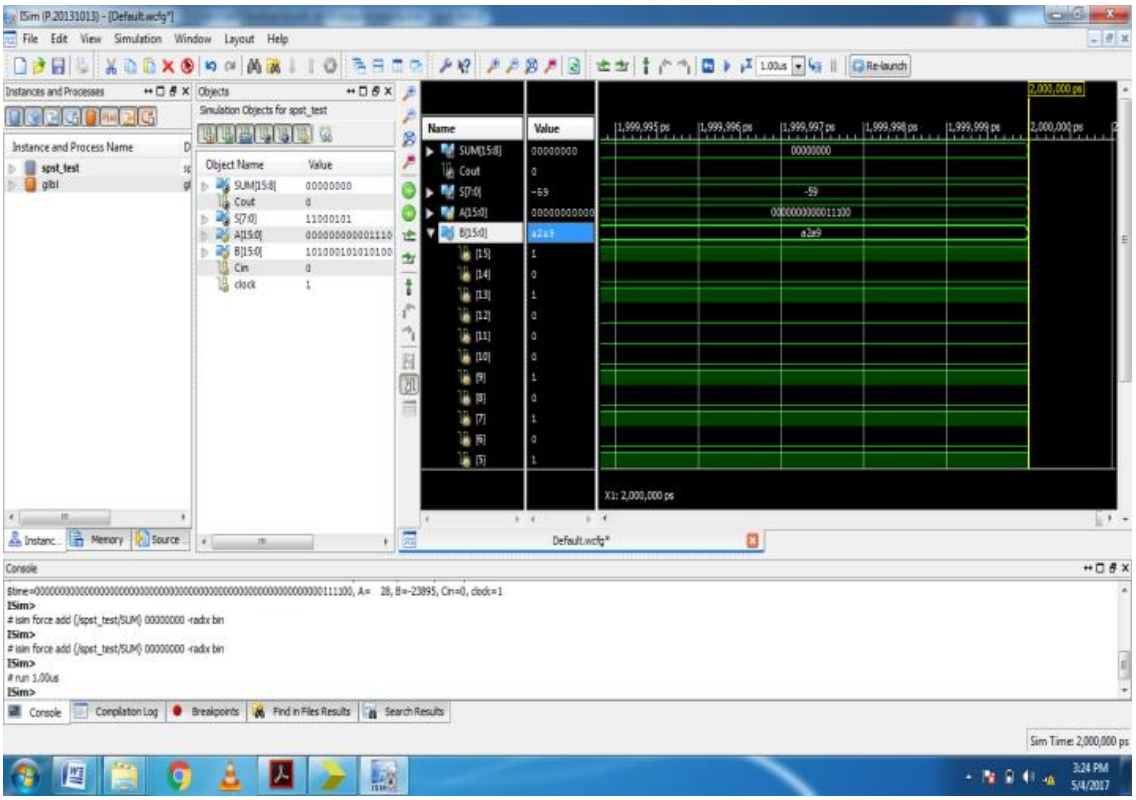

Fig 6: Output Waveforms of SPST based CSLA for unsigned and signed numbers.

Comparison Table

S.No.	Parameters	Carry Select Adder	SPST Carry Select Adder
1.	**No. Of LUT Used**	12	8
2.	**Delay(Ns)**	4.950	3.095
3.	**Power(Mw)**	116.39	82

Table: 1 Comparision between Convetional and SPST based CSLA

Conclusion

A high speed and low power SPST based CSLA has been designed . Table 1 shows that SPST based CSLA results in low power consumption and achievement in higher speed. Power consumption is reduced by 27% and achievement in speed is approximately 10% as compared to conventional CSLA. This design is synthesised using Xilinx 14.7 with Verilog HDL coding.

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