Optical Quadruple Feynman Gate using SLM and Savart Plate

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***Abstract*—**In recent years, Reversible logic is emerged as a promising computing paradigm with applications in low-power CMOS, quantum computing, optical computing and nanotechnology. The classical set of gates such as AND, OR, andEXOR are not reversible. However, optical computing technology the trinary and quadruple valued logic systems are the most important ones in the many valued logic system.In this paper, spatial light modulator (SLM) and Savart Plate based circuit has been proposed and described for realization of quadruple Fenyman Gate. It is optical in nature. SLM and Savart Plate can play a significant role in this field of ultra-fast all optical signalprocessing.

Keywords-*Di-bit; Feynman Gate;Quadruple;SavartPlate; SLM.*

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I. INTRODUCTION

Recently, there have been major advances in integrated circuit technology that have made feasible implementation of electronic circuits operating with more than two discrete levels of signal. Such circuits called multi-valued logic circuits, offer several potential opportunities for the improvement of present VLSI circuit designs. E.V. Dubrova [1] and others have proposed and developed multi -valued logic (MVL) circuit design, revealing both the opportunities they offer and the challenges they face [2-4]. Vasundara Patel and K. S. Gurumurthy demonstrated the arithmetic operations like addition, subtraction and multiplications in modulo-4 arithmetic, and also addition, multiplication in Galois field, using MVL [5]. Quaternary to binary and binary to quaternary converters are designed using down literal circuits. Negation in modular arithmetic is designed with only one gate. Logic design of each operation is achieved by reducing the terms using Karnaugh diagrams, keeping minimum number of gates and depth of net into consideration. Quaternary multiplier circuit is proposed to achieve required optimization. This architecture enables one to perform all-optical processing of signals, including two input logic operations, half-adder, full-adder, full sub-tractor, one-bit data comparator, etc.

During the last thirty years due to the needs of tremendous operational speed and processing a number of data, many new ideas are being floated in the field of computing. These include exploration of implementation of optical processor for switches in one hand and on the other hand the logical developments from binary to multivalued logic are also being included in their field of activities. Though the major attraction for optical processors lies in the parallel operation but it was also felt that it is possible to implement multivalued logic in optical system using the polarization states of light beam along with the presence or absence of light [6]. The parallelism of optical beam could not be properly utilized using cascaded single- bit operating units thereforea signeddigit number system was initiated with the pioneering works of Avizienis [7]. The carryfree operation was also suggested using a modified signed digit [8-11] or modified trinary [12] system. The demand for implementations of such gates has also extended the activities in the field. However, Lukasiewicz [13] who initiated the use of ternary logic based on three states and has modified it later with an idea that four states logic is a much better proposition.

Design of reversible logic is highly demanding in many applications for lossless data processing[14-17]. Conservative and reversible logic gates are widely known to be compatible with revolutionary computing paradigms such as optical and quantum computing. To this aim, we have presented optical quadruple Feynman Gate using SLM and Savart Plate in this paper. The superiority of the proposed scheme is verified by simulation results and compared with selected other models.

The proposed paper is arranged as follows: The quadruple valued logic systemsare reported in Section II. Section III describes briefly the truth tables based on di-bit representation. Section IV presents the working principle of basic building block using SLM and Savart Plate. The working principle and design of Quadruple Feynman gateare presented in Section V. Section VI shows logical simulation results and finally concluding remarks are made in Section VII.

II. QUADRUPLE VALUED LOGIC SYSTEM

The four-state representations of the quadruple valued logic system may be classified as the true, partly true, partly false and the false [18-20]. In this case we have considered these four states explicitly as {0, 1, 2, 3} and their di-bit representations as {00, 01, 10, 11}. It is to be noted here that the four valued system with states {0, 1, 2, 3} does not satisfy the basic field conditions whereas as a di-bit representation of the form 00 ➔0, 01 ➔1, 10 ➔ 2 and 11➔ 3 may be used to represent a four valued logic where the basic two valued logic are applicable. As four is not a prime number, it cannot be considered as a field nevertheless this can be included in Galois Field GF(k^r), where k is a prime number and r is a positive integer . The logical states, their representations and corresponding di-bit representations and the state of polarization is given in the Table I.

TABLE I. QUADRUPLE-VALUED LOGIC SYSTEM

Logical state	Represented by	Dibit representation	State of polarization
False/ Wrong information	0	00	No light
Partial Information	1	01	Vertical polarization
Partial Information (complement of 1)	2	10	Horizontal polarization
True/ Complete Information	3	11	Presence of both the horizontal & vertical polarization

III. TRUTH TABLES BASED ON DI-BIT REPRESENTATION

The basic logical operations with dibit representation as mentioned in the earlier section may be expressed in the following fashion. In the present system the normal logical gates e.g., OR, AND, NOT, XOR, NAND, NOR and XNOR may be represented bit-wise. The truth table for these conventional bit wise logic gates are represented in Table II.

TABLE II. TRUTH TABLES FOR (A) OR, (B) AND, (C) NOT (D) XOR, (E) NAND, (F) NOR AND (G) XNOR GATES

B \ A	00	01	10	11
00	00	01	10	11
01	01	01	11	11
10	10	11	10	11
11	11	11	11	11

(a)

B \ A	00	01	10	11
00	00	00	00	00
01	00	01	00	01
10	00	00	10	10
11	00	01	10	11

(b)

A	Ā
00	11
01	10
10	01
11	00

(c)

B \ A	00	01	10	11
00	00	01	10	11
01	01	00	11	10
10	10	11	00	01
11	11	10	01	00

(d)

B \ A	00	01	10	11
00	11	11	11	11
01	11	10	11	10
10	11	11	01	01
11	11	10	01	00

(e)

B \ A	00	01	10	11
00	11	10	01	00
01	10	10	00	00
10	01	00	01	00
11	00	00	00	00

(f)

B \ A	00	01	10	11
00	11	10	01	00
01	10	11	00	01
10	01	00	11	10
11	00	01	10	11

(g)

IV. THEBASIC BUILDING BLOCK

The basic building block to implement the logical operations in quadruple valued logic system is shown in Fig. 1. Light from a laser source L after passing through the polarizer P is polarized at an angle 45^o with respect to the two crystal axes and incident on the Savart Plate S_1 as shown in Fig. 1. The light incident on S_1 is splitted into two orthogonal components and comes out of S_1 with a spatial shift between them. The electrically addressable negative SLMs - P_1 and P_2 are then used for the controlling of two components of inputs beam. The nature of the negative SLM is such that it is transparent when there is no electric voltage applied on it and it becomes opaque when an electric voltage is applied on it. The property of positive SLM is just reverse. Hence the input may be considered as in the form of di-bit (two bits) representation. The outputs from SLM are finally combined by the Savart Plate S_2.

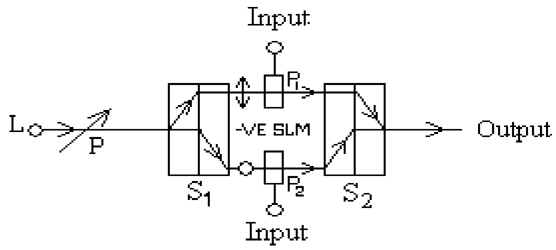

Figure 1. The Basic Building Block

V. QUADRUPLE FEYNMAN GATE : PRINCIPLE AND DESIGN

Feynman gate is a (2:2) one-through reversible logic gate. It has two inputs (A, B) and two outputs (X, Y) satisfy the relation as follows:

$$\left.\begin{array}{l} X = A \\ Y = (A \oplus B) \end{array}\right\}$$

The binary truth table is given in Table III.

TABLE III. BINARY TRUTH TABLE OF FEYNMAN GATE

Input		Output	
A	B	X	Y
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

The quadruple truth table with di-bit representation is given in Table IV.The SLM and Savart Plate based circuit for optical reversible Feynman gate is given in Fig. 2.

TABLE IV. QUADRUPLE TRUTH TABLE OF FEYNMAN GATE

A	*A1*	*A2*	***B***	*B1*	*B2*	***X***	*X1*	*X2*	***Y***	*Y1*	*Y2*
0	0	0	**0**	0	0	**0**	0	0	**0**	0	0
0	0	0	**1**	0	1	**0**	0	0	**1**	0	1
0	0	0	**2**	1	0	**0**	0	0	**2**	1	0
0	0	0	**3**	1	1	**0**	0	0	**3**	1	1
1	0	1	**0**	0	0	**1**	0	1	**1**	0	1
1	0	1	**1**	0	1	**1**	0	1	**0**	0	0
1	0	1	**2**	1	0	**1**	0	1	**3**	1	1
1	0	1	**3**	1	1	**1**	0	1	**2**	1	0
2	1	0	**0**	0	0	**2**	1	0	**2**	1	0
2	1	0	**1**	0	1	**2**	1	0	**3**	1	1
2	1	0	**2**	1	0	**2**	1	0	**0**	0	0
2	1	0	**3**	1	1	**2**	1	0	**1**	0	1
3	1	1	**0**	0	0	**3**	1	1	**3**	1	1
3	1	1	**1**	0	1	**3**	1	1	**2**	1	0
3	1	1	**2**	1	0	**3**	1	1	**1**	0	1
3	1	1	**3**	1	1	**3**	1	1	**0**	0	**0**

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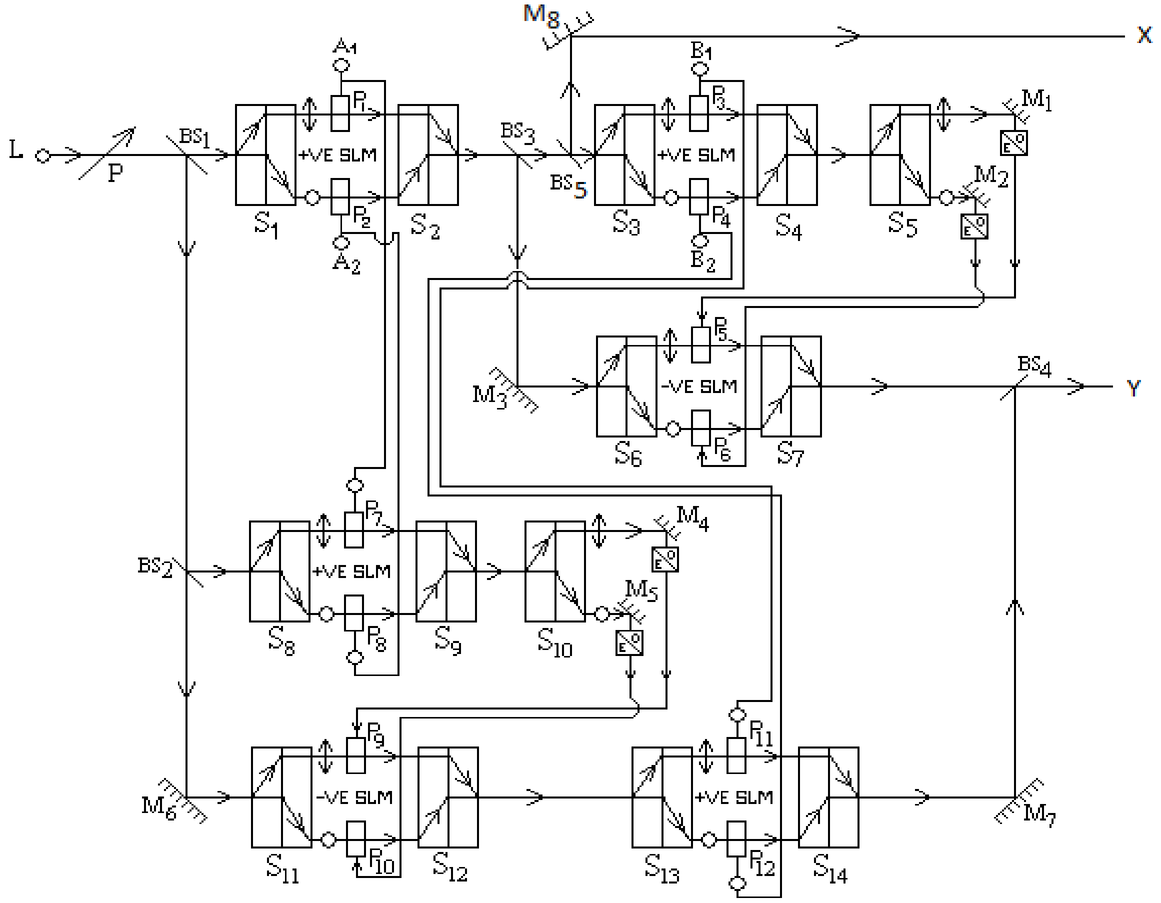

Figure 2. SLM and Savart Plate based Feynman gate

The polarized parallel beam coming from the Laser source L through polarizer P is incident on the beam splitter BS_1 - where it is splitted into two directions as shown Fig. 2. One part is incident on the Savart Plate S_1 and the other part on the beam splitter BS_2. The Savart Plate S_1 splits the beam into two orthogonal components - the p-polarization and the s-polarization. The input A (combination of A_1 and A_2) controls the positive SLMs P_1 and P_2 and accordingly the p-polarization and s-polarization come out of P_1 and P_2.The outputs of P_1 and $P_2$are recombined by the Savart Plate S_2 and incident on the beam splitter BS_3. The one part of the output of BS_2 is incident on S_8 and by similar process it is also spatially modulated by the positive SLMs P_7 and P_8 depending on the input $A(A_1,A_2)$ and finally they recombined by S_9. The other part of the output of BS_2 ray reflected by the mirror M_6 is incident on the Savart Plate S_{11} and by similar process it is also spatially modulated by the positive SLMs P_9 and P_{10} depending on the input which is the output of S_{10}. The output of S_{10} passes through the opto-electrical converters (O/E) which are used to convert the light signal into electric voltage. The one output of BS_3 is fed to BS_5 which splits the light again in two directions.One is reflected by mirror M_8 and produce the output X=A. Another one is incident on Savart Plate S_3 and it is also specially modulated by the positive SLMs P_3 and P_4 depending on the control input $B(B_1,B_2)$ and finally they recombined by S_4. By the same procedure finally the output of S_{14} and S_7 combined by $BS_4$and produce the other output Y=A XOR B. The different cases are explained as follows:

(1)When A=0 (A_1=0,A_2=0) and B=0 (B_1=0,B_2=0) then no light is present at the output of S_2, so X=0 (X_1=0,X_2=0). There will be no light at the output of S_7 and S_{14}, so the output, Y =0(Y_1=0,Y_2=0).

(2)When A=0 (A_1=0,A_2=0) and B=1 (B_1=0,B_2=1) then no light at the output of S_2, hence X=0 (X_1=0,X_2=0). There will be no light at the output of S_7. As the P_9 and P_{10} are the –VE SLM, so both polarized light will be present at the output of S_{12}.As P_{11}=0 and P_{12}=1, the output of S_{14}will give vertical polarization. There is no light at the output of S_7.The final output is Y=1 (Y_1=0,Y_2=1).

(3) When A=0 (A_1=0,A_2=0) and B=2 (B_1=1,B_2=0) then no light at the output of S_2, hence X=0 (X_1=0,X_2=0).As the bit representation of B is reverse with respect to the previous case so P_{11}=1 and P_{12}=0. The outputof S_{14}consists ofhorizontal polarization. There is no light at the output of S_7. The final output is Y=2 (Y_1=1,Y_2=0).

(4) As A=0 (A_1=0,A_2=0) and B=3 (B_1=1,B_2=1) so light at the output of S_2, hence X=0 (X_1=0,X_2=0). The output of S14 consists of vertical and horizontal polarized light.   There is

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no light at the output of S_7. The final output is Y=3 (Y_1=1,Y_2=1).

(5) When A=1 (A_1=0,A_2=1) and B=0 (B_1=0,B_2=0) so the output of S_2 is at logic 1 state , hence X=1 (X_1=0,X_2=1).The output of S_7consists of only vertically polarized light and no light at the output of S_{14}. The final output is Y=1 (Y_1=1,Y_2=0)

(6) When A=1 (A_1=0,A_2=1) and B=1 (B_1=0,B_2=1) so the output of S_2 is at logic 1 state, hence X=1 (X_1=0,X_2=1).There is no light at the output of S_7 and S_{14}. The final output is Y=0 (Y_1=0,Y_2=0).

(7) When A=1 (A_1=0,A_2=1) and B=2 (B_1=0,B_2=1) so the output of S_2 is at logic 1 state, hence X=1 (X_1=0,X_2=1). The output of S_7 consists of vertically polarized light and the output of S_{14} consists of horizontally polarized light. The final output consists of both polarized light i.e. Y=3 (Y_1=1,Y_2=1).

(8) When A=1 (A_1=0,A_2=1) and B=3 (B_1=1,B_2=1) so the output of S_2 is at logic 1 state, hence X=1 (X_1=0,X_2=1). There is no light at the output of S_7 and the output of S_{14} consists of horizontally polarized light. The final output consists of only horizontally polarized light i.e. Y=2 (Y_1=1,Y_2=0).

(9) When A=2 (A_1=1,A_2=0) and B=0 (B_1=0,B_2=0) so the output of S_2 is at logic 2 state, hence X=2 (X_1=1,X_2=0). There is no light at the output of S_{14} and the output of S_7 consists of horizontally polarized light. The final output consists of only horizontally polarized light i.e. Y=2 (Y_1=1,Y_2=0).

(10) When A=2 (A_1=1,A_2=0) and B=1 (B_1=0,B_2=1) so the output of S_2 is at logic 2 state, hence X=2 (X_1=1,X_2=0). The output of S_7 consists of horizontally polarized light and the output of S_{14} consists of vertically polarized light. The final output consists of both polarized light i.e. Y=3 (Y_1=1,Y_2=1).

(11) When A=2 (A_1=1,A_2=0) and B=2 (B_1=1,B_2=0) so the output of S_2 is at logic 2 state, hence X=2 (X_1=1,X_2=0). There is no light at the output of S_7 and S_{14}. The final output is Y=0 (Y_1=0,Y_2=0).

(12) When A=2 (A_1=1,A_2=0) and B=3 (B_1=0,B_2=1) so the output of S_2 is at logic 2 state, hence X=2 (X_1=1,X_2=0). There is no light at the output of S_7 and the output of S_{14} consists of vertically polarized light. The final output consists of only vertically polarized light i.e. Y=1 (Y_1=0,Y_2=1).
(13) When A=3 (A_1=1,A_2=1) and B=0 (B_1=0,B_2=0) so the output of S_2 is at logic 3 state, hence X=3 (X_1=1,X_2=1). There is no light at the output of S_{14} and the output of S_{14} consists of both horizontally as well as vertically polarized light. The final output consists of both polarized light i.e. Y=3 (Y_1=1,Y_2=1).

(14) When A=3 (A_1=1,A_2=1) and B=1 (B_1=0,B_2=1) so the output of S_2 is at logic 3 state, hence X=3 (X_1=1,X_2=1).There is no light at the output of S_{14} and the output of S_7 consists of horizontally polarized light. The final output consists of only horizontally polarized light i.e. Y=2 (Y_1=1,Y_2=0).

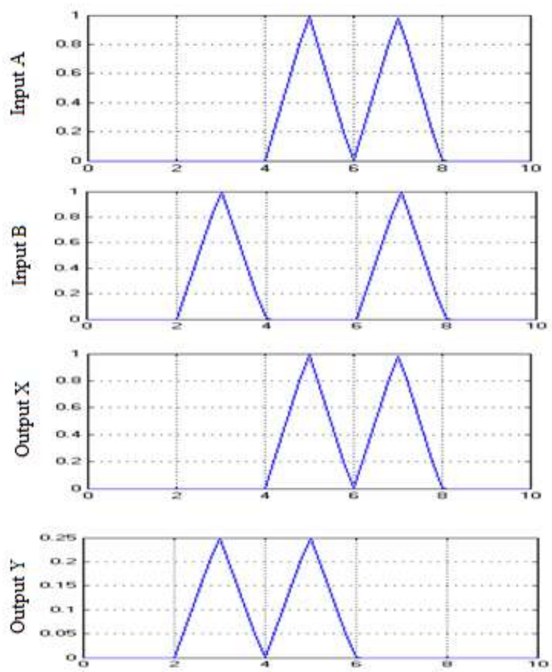
(15) When A=3 (A_1=1,A_2=1) and B=2 (B_1=0,B_2=1) so the output of S_2 is at logic 3 state, hence X=3 (X_1=1,X_2=1). There is no light at the output of S_{14} and the output of S_7 consists of vertically polarized light. The final output consists of only vertically polarized light i.e. Y=1 (Y_1=0,Y_2=1).

(16) When A=3 (A_1=1,A_2=1) and B=2 (B_1=0,B_2=1) so the output of S_2 is at logic 3 state, hence X=3 (X_1=1,X_2=1). There is no light at the output of S_7 and S_{14}. The final output is Y=0 (Y_1=0,Y_2=0).

VI. PERFORMANCE EVALUATION THROUTH SIMULATION AND DISCUSSION

Simulation is done in Mathcad-7. The power of the input pulse is taken A = B = 1.13 dBm. Here we use 50:50 beam splitters.The vertical axis in Fig.3 indicates power in dBm, while horizontal axis represents time scale in ps. The time instant for the occurrence of bit pattern are at 0, 5, 10, 15 ps.

Figure 3: Logical simulation result [x- axis: time (ps) and y-axis: power (dBm)].



Upper two set waveforms indicate the input bit sequences 0011, 0101 for the input variables A and Brespectively. Similarly, the lower two waveforms indicate bit sequence 0011, 0110 bit pattern change of output variables X and Yrespectively.

VII. CONCLUSION

In this paper, SLM and Savart Plate based quadruple Feynman Gate circuit has been proposed and described. The results obtained numerically and the theoretical models developedare very much useful to future optical reversible logic computing system.Different arithmetic and logic operations in reversible system can easily be performed with this gate.The purpose of this study is to explore the quadruple logic system in four-state implementation by whichit is possible to handle huge volume of data at a time. It is expected that the proposed work will provide to a new paradigm to the arena of reconfigurable computing.

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