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Variable Size 2D DCT with FPGA Implementation

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Abstract-A lot of research are going on in the field of image processing algorithm. Compression enables throughput processing through transmission medium.A lot of research is going on in this field to have a highly efficient output. In this paper a co-simulation environment is for discrete co-sine transform is proposed which enables compression for different size of images provides facts approximately FPGA implementation for compression of an image using the Xilinx system Generator[1] (XSG) for MATLAB. For using Xilinx system generator for an image processing minimizes the complexity in structural design also gives extra characteristic for hardware co-simulation[2].The most easiest and reliable constructing block for compression system is DCT. Which may be completed the usage of specialized algorithms. Fast prototyping based on FPGA platform of the virtex-5 family is used to validate the operation of the defined DCT device.

Keywords:-*FPGAImplementation, XilinxSystemGenerator, Matlab, Simulink, Co-simulation.*

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I. Introduction

A huge number of images records compression strategies are available, which are being tailored to a selected sort of applications, such as: compact disc, videoconference, videophones and multimedia ***systems***. In all of these programs the transmission line bandwidth will be determined by the compression general for use[2]. DCT includes particular traits which permit an effective image compression.Picture and video compression and decompression are applied in both software program and hardware. However, the hardware implementations are specifically crucial for the conclusion of hugely algorithms and may acquire an awful lot better throughput than software program solutions.

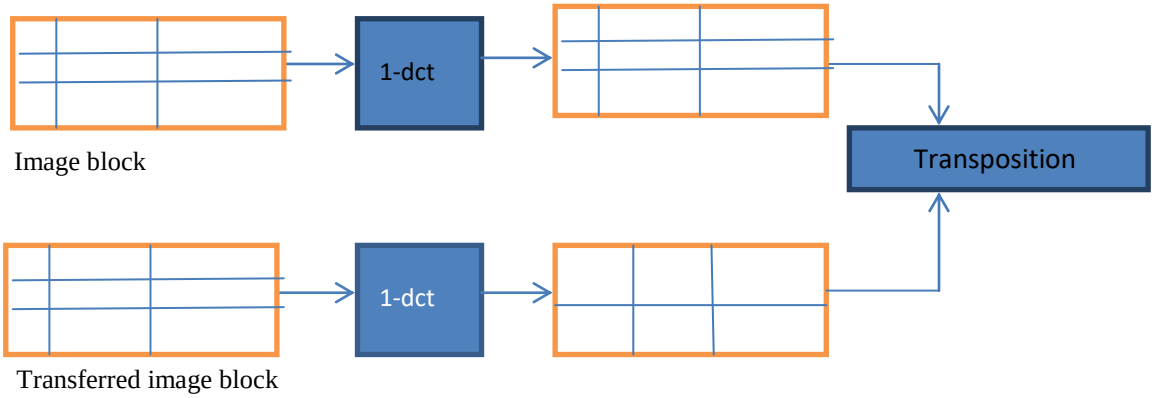

Fig-1 2D DCT

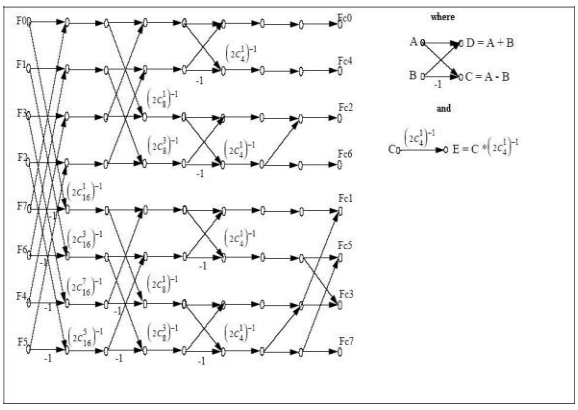

Fig2-Dct algorithm[2]

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$$A(u)=\sqrt{2}/nc(u)\sum_{x=0}^{n-1}A(x)\cos\frac{(2x+1)u\pi}{2n} \qquad u=0,\ldots\ldots,n$$

Where $c(u)=2^{-\frac{1}{2}}$ for u=0

=1 otherwise

Equation-1$(1D\ DCT)^2$

For calculating 2-DCT

$$A(u,v)=\frac{\sqrt{2}}{n}*\sqrt{2}/m\sum_{i=0}^{n-1}a(i)\sum_{i=0}^{m-1}a(j).cos\frac{(2x+1)u\pi}{2n}.cos\frac{(2x+1)v\pi}{2m}$$ for0<n<N-1

=0, otherwise

Equation-2$(2D\ DCT)^2$

II. Hardware design:-

1. Xilinx system generator-

System Generator is a product of the ISE® design Suite and due to this Xilinx DSP Blocksetwhich includeadders,multipliers, registers, filters and reminiscences for use of an unique layout. An optimized result can be got using these blocks.RTLsynthesis are not required for synthesizing a image processing algoon FPGA. Downstream codes and user constraints are automatically generated. It allows us to work under a co-simulation environment.

III. Design flow for image processing in system generator

In order to work with a co-simulation environment, we need to work with MATLAB andISE design suite at the same time. Both should beconfigured simultaneously in order to have system generator with it.The images are simulated in such manner that the pixels are achieved to simulate in Xilinx also for the real time operation.The results are available with video viewer. The outputs are simulated on FPGA board in order to have software and hardware co-simulation. The results are simulated in FPGA virtex-5 kit. System generator has ability to generate a code for a particular image processing.The code is generated according hardware descriptive language i.e., Verilog hdl and accessed using Xilinx ISE.The generated codes are then synthesized in order to have the netlist. And we have the automatically generated user constraint file (UCF) for hardware ***implementation***. By which the code is synthesized on FPGA.

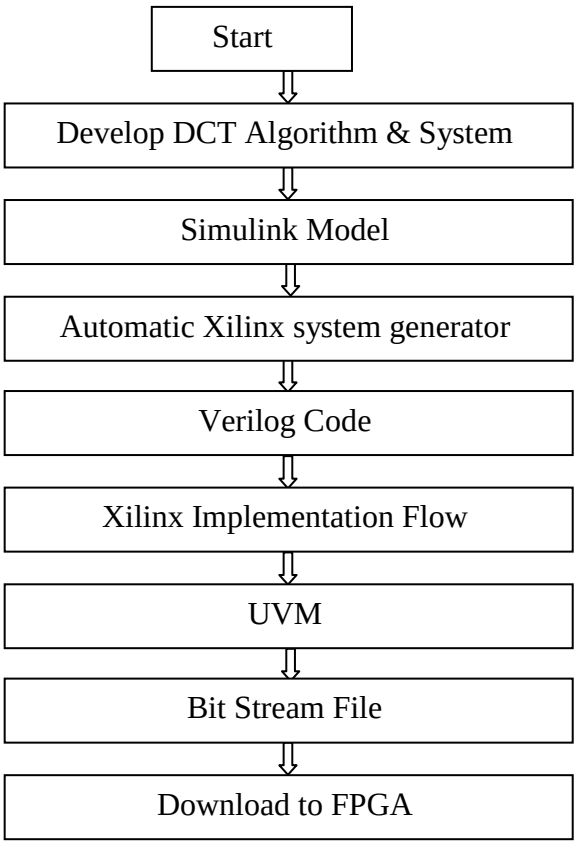

Fig3. –flow chart for co-simulation

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IV. Elements which are used for pre- processing and post-processing

Image pre-processingblocks are used in Simulink model for providing inputs to FPGA for hardware and ***software*** co- simulation.

- Resize- It allows the picture for setting in a suitable dimension..
- Convert 2-D to at 1-D-A multidimensional pixel array is transposed into a single pixel array.
- Frame conversion and buffer: The whole array is set into a single frame.

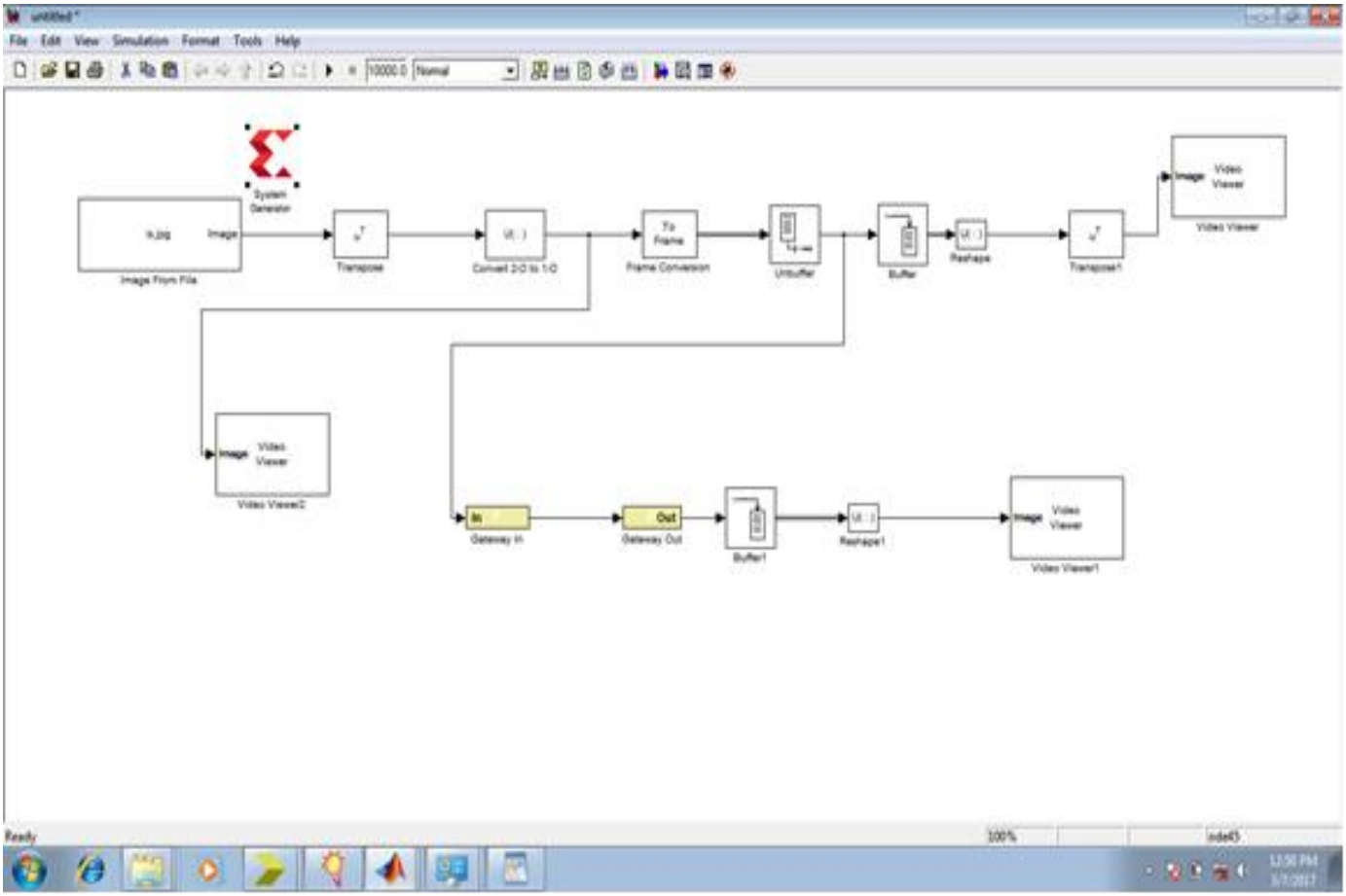

Fig-4.preprocessing and post processing blocks

Post-processing uses-

- Data type conversion-It transposes the pixels into unsigned character.
- Buffer-Italters scalar samples to the frame.
- Convert 1D to 2-This element is used for reshaping the image.
- Sink: The output is shown through this block.

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V. Image processing algorithm for compression

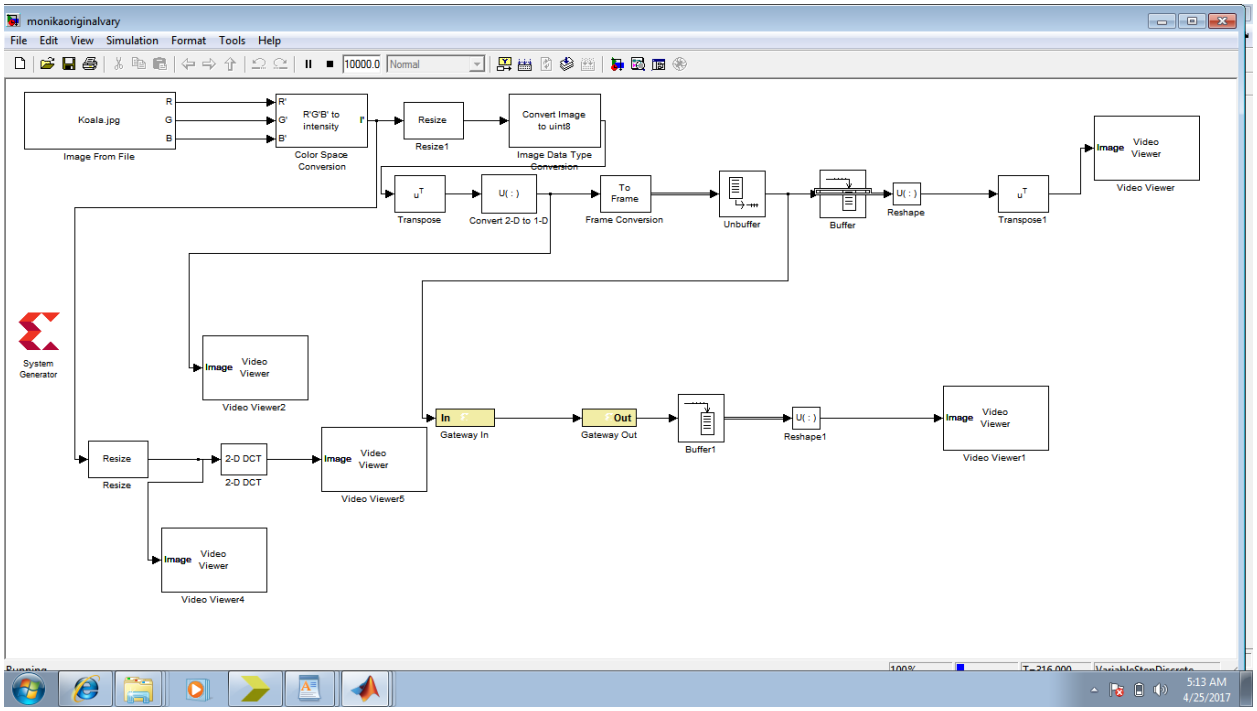

Fig-5 Simulink model for image compression

VI. RESULT

Original image-1

Image-2

Output of image-1

Output of image-2

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VII. Hardware co-simulation

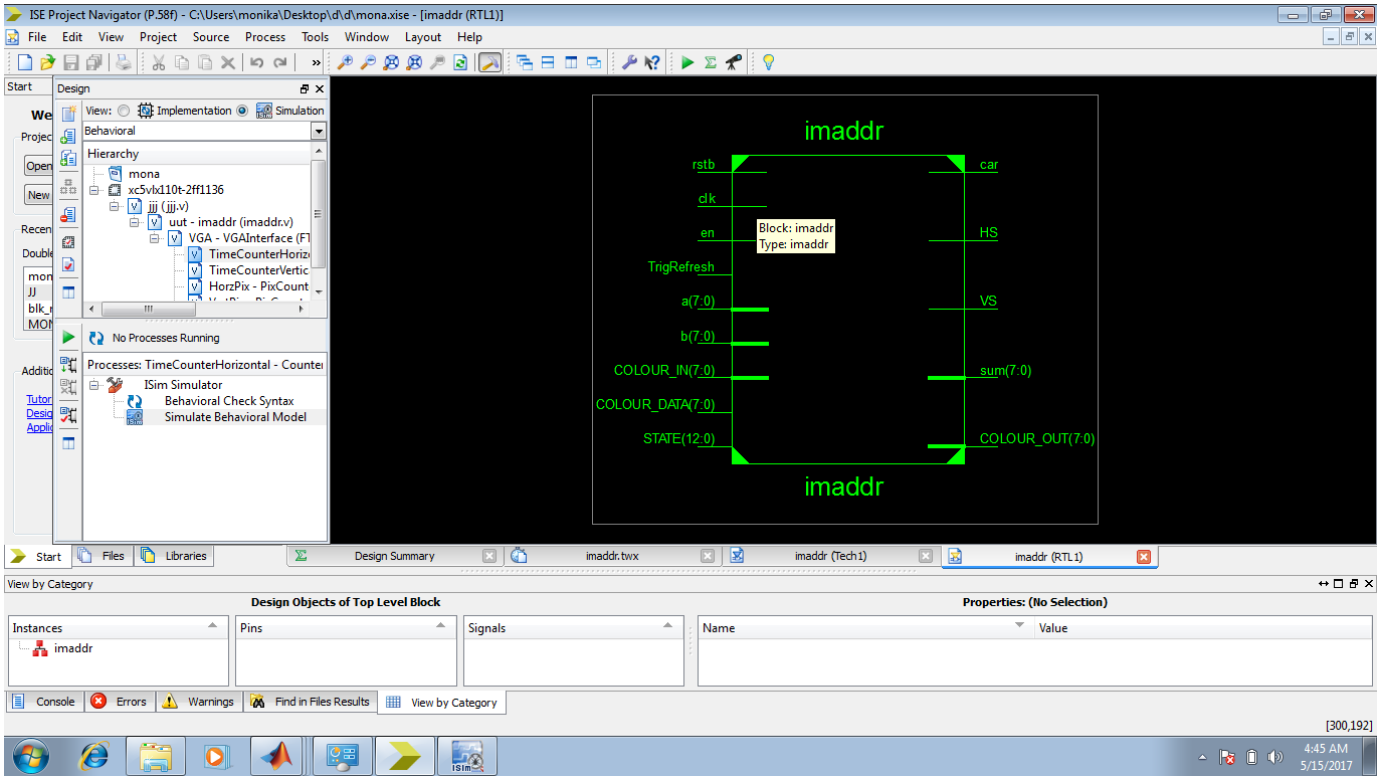

Fig-6 RTL schematic

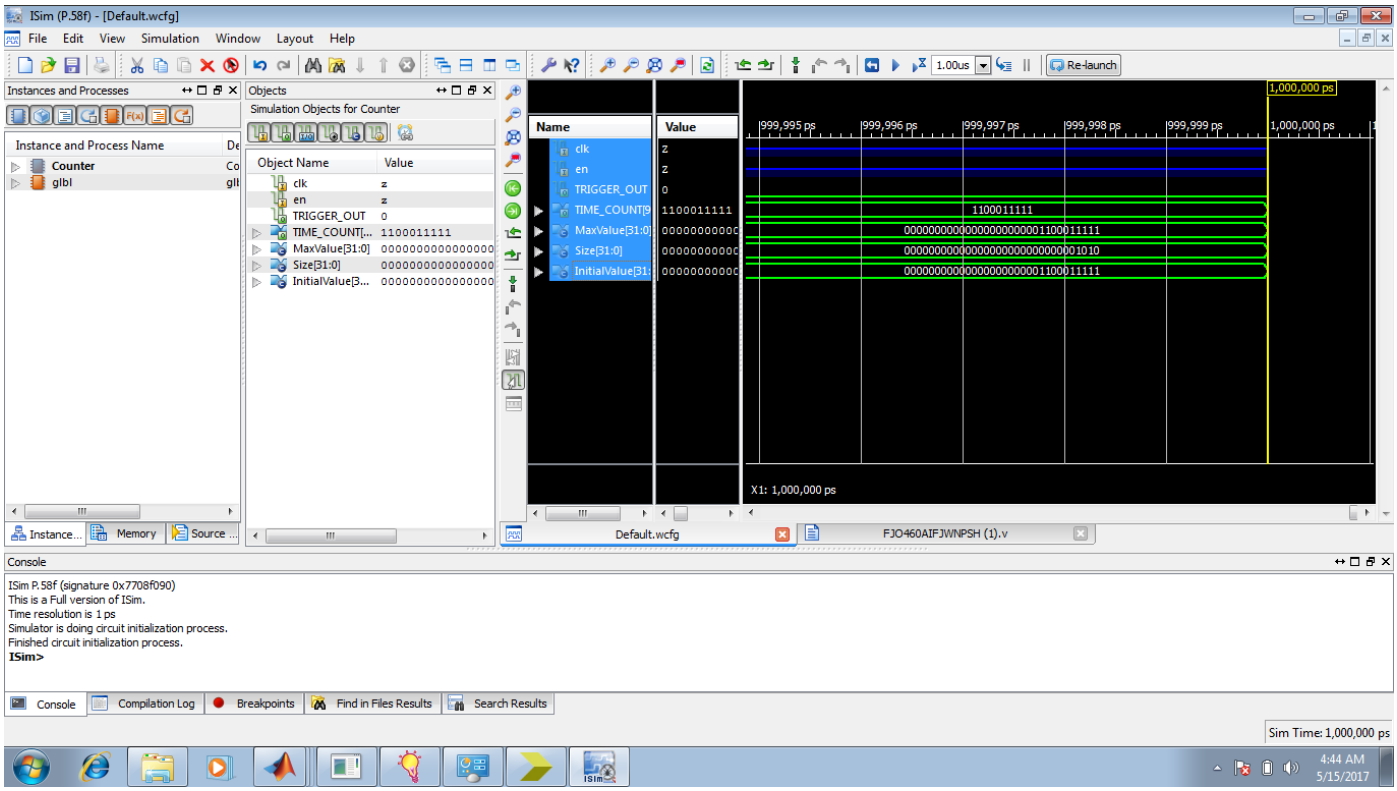

Fig-7 waveform of 2-D DCT compression algo

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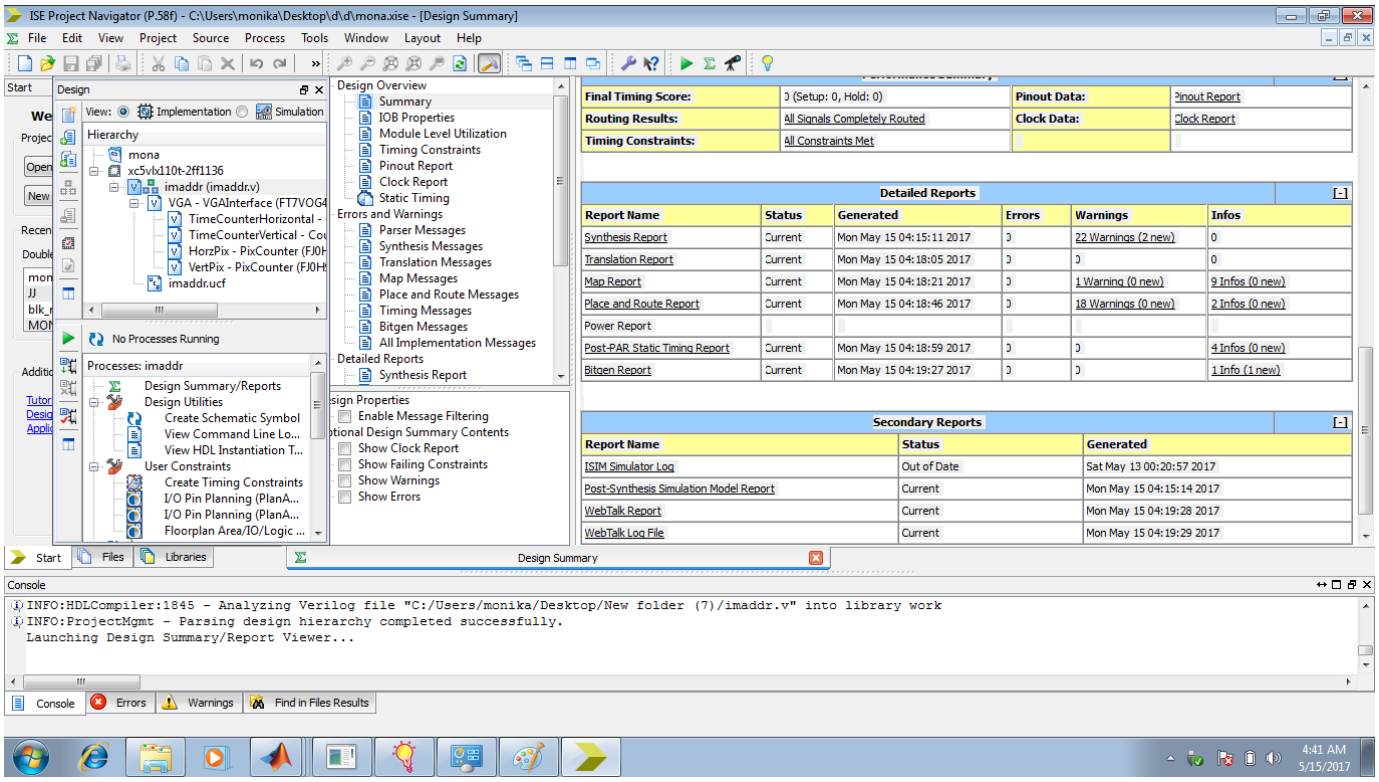

Fig-8 synthesis report

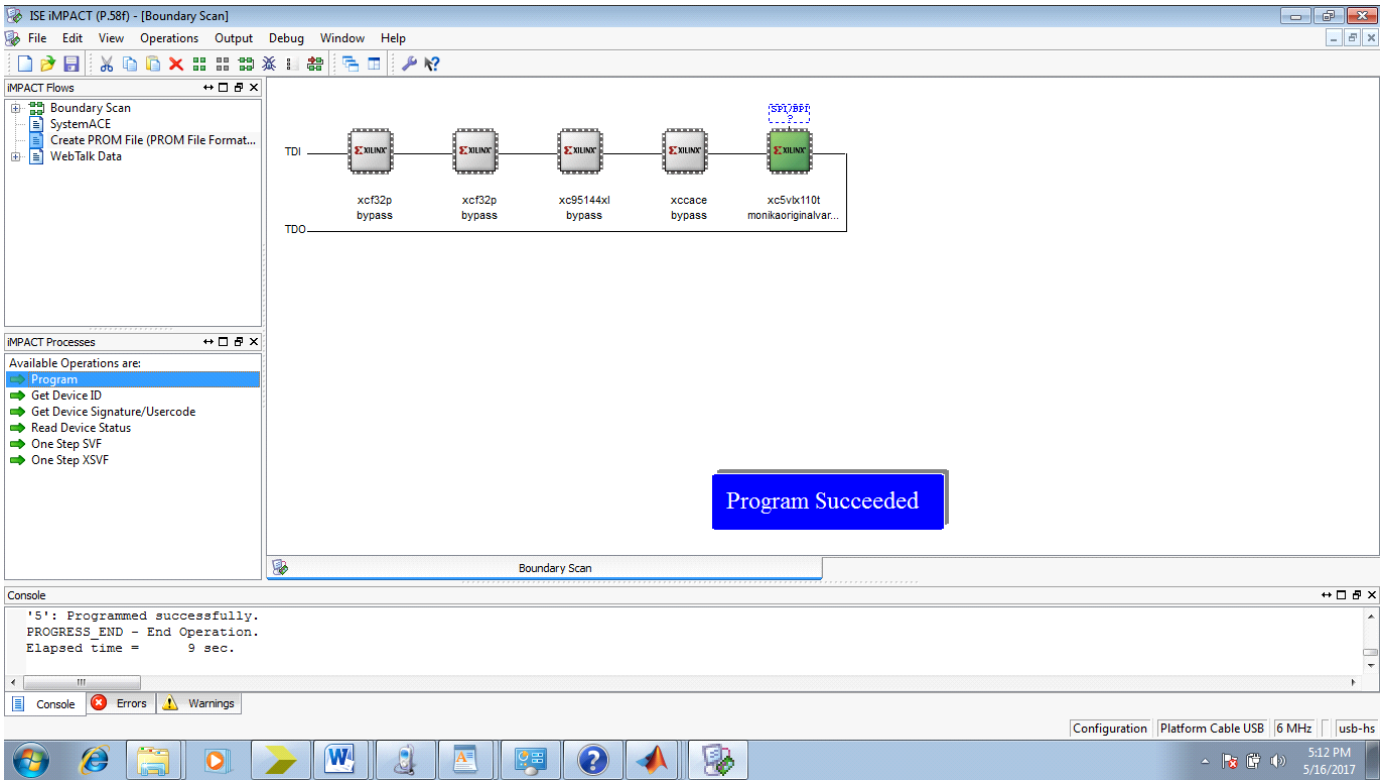

Fig-9 FPGA simulation

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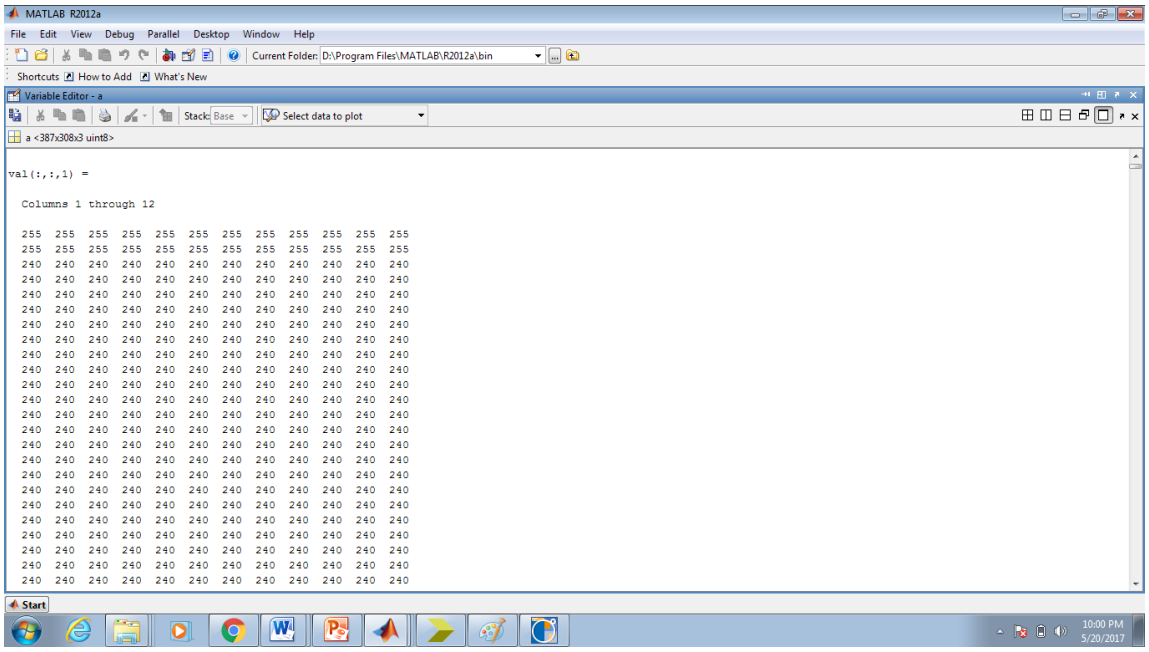

Fig-10 original image pixel

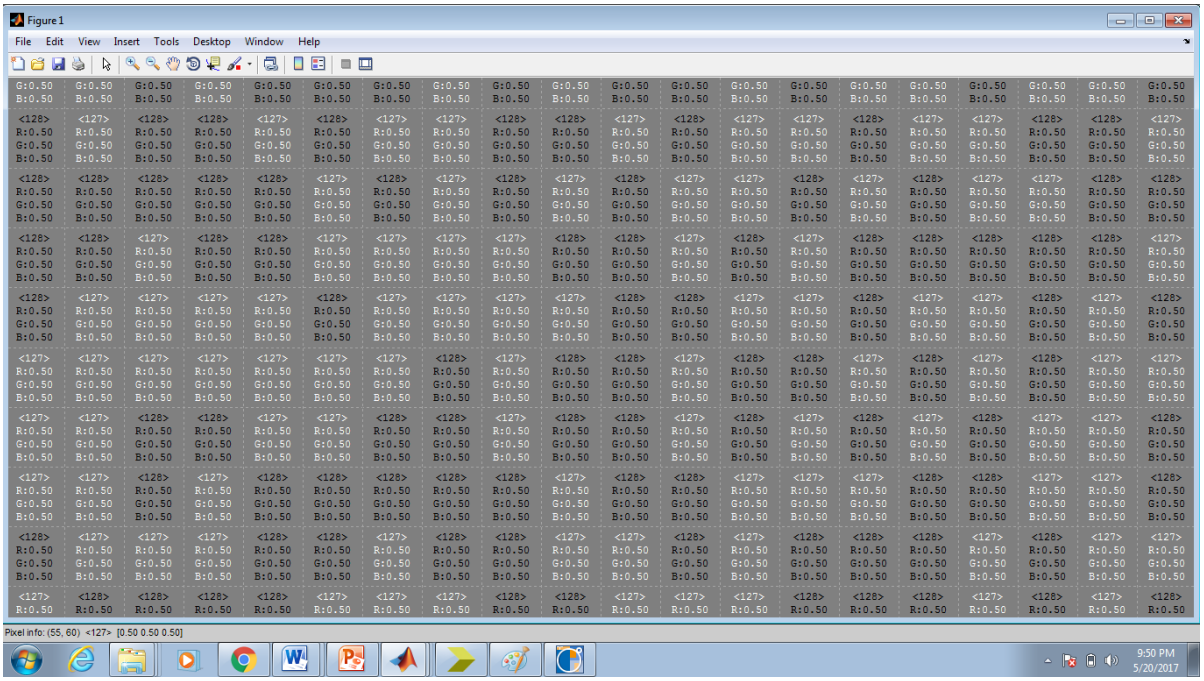

Fig-11 compressed image pixel

VIII. Conclusion-

We have implemented a 2d dct for image compression which supports variable size images and synthesized it on fpgavirtex 5 with clk9mhz and luts 9. Which will be a great achievement in image video and audio compression.

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