International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169
Volume: 5 Issue: 5 135 – 138

Designing Techniques for Low Power Multipliers: A Review

Swarnalika Nagi[1], Ms. Jagandeep Kaur[2], Ms. Nisha Charaya[2]
[1] Student M.Tech VLSI Design, Amity University Haryana
swarnalika10@gmail.com
[2]Asst. professor, Amity school of Engineering & Technology, Amity University Haryana
jkaur@ggn.amity.edu
charayanisha1010@gmail.com

Abstract:- Multipliers are fundamental building blocks of all DSP applications. Design of low power, high speed multipliers is carried out to reduce latency and power dissipation of a processing system because switching and critical computations of a multiplier are high, compared to other data path units of a processing architecture. In recent years, a few techniques have been developed that enhance power for accuracy by removing or rearranging multiplier's blocks. Choosing the proper technique and implementing it can make a big difference in the power dissipation. This is important for low-power battery-operated devices, where longer battery life could be preferred to higher output accuracy. To enhance speed many changes have been made over the existing booth algorithm. In this paper, a simplified comparative study has been presented among SPST based Wallace tree multipliers and other low power multiplier techniques.

Keywords: *Low power multiplier techniques, SPST, Wallace Tree Multiplier.*

*****

Introduction

Multiplier is an essential component in mostly each and every DSP system. Multiplier is one of the slowest and large area required elements in DSP applications which determine the overall performance of the system. In today's era faster devices with optimized power consumption are the requirement of every consumer [2]. Hence, enhancing the speed, power and area of the multiplier are main design goals to fabricate a DSP system. Enhancing speed results mainly in larger area due to tradeoff between area and speed. If speed and power consumption of components of the devices could be enhanced then overall performance of the devices will be increased ultimately. In many digital circuits, multiplier consumes most of the power and will produce lag [1].

There are various types of multipliers and each multiplier is described by different algorithm and structures. These multipliers also have different performance parameters and each one of them can be again optimized to get better performance parameters [1] e.g. serial multiplier, parallel multiplier, array multiplier, booth multiplier and Wallace tree multiplier. The objective of a good multiplier is to provide a physically packed together, low power consumption and high speed unit. In this paper, some techniques have been discussed which result in low power multipliers. In the last section SPST based Wallace tree multiplier has been described.

Parameters of a Multiplier

An efficient multiplier should have the following characteristics:

- **Area:** A multiplier should occupy less number of slices and LUTs.
- **Accuracy:** A good multiplier should give correct results.
- **Speed:** Multiplier should perform an operation at high speed.
- **Power:** Multiplier should consume less power.

Multiplication process has three main steps [2]:

1. Partial product generation.
2. Partial product reduction.
3. Final addition.

Background

Low Power Techniques for Multipliers [2]

1. Pipelining technique:

The pipelining technique has been used to increase throughput of a high speed circuit or system which splits whole system into various small cascade stages and put in some registers to synchronize each stage's output [5]. With the increase in the number of stages, the area and power consumption increases eventually. So, mostly pipelining technique can be utilized in Wallace tree multiplier to enhance the performance. Also, pipelined multipliers are useful when arithmetic throughput is of more interest than latency because the use of registers along the array reduces the unnecessary activity [3][5].

 ISSN: 2321-8169
135 – 138

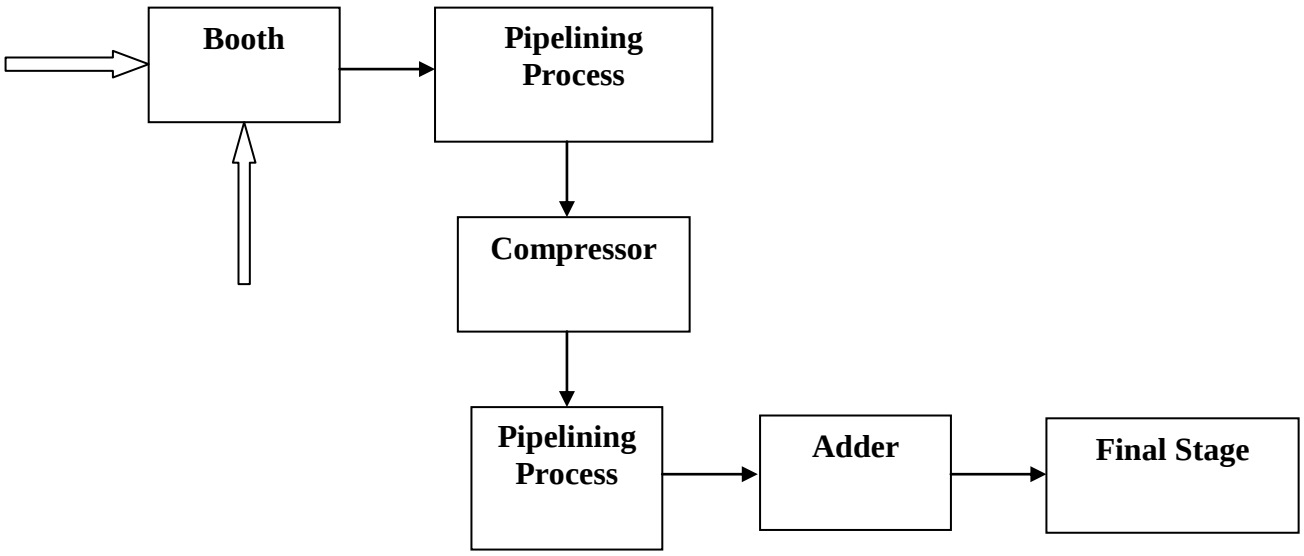

Fig 1: Block diagram of pipelining booth multiplier

2. Compressor based Multiplier:

The Wallace tree method for multiplication is generally used to sum up the partial products (PP) in a tree-like manner in order to get two rows of PP that can be summed up in the last stage [4]. The critical path delay is directly proportional to 'log (n)' where n is the number of bits in multiplier that's why Wallace tree multiplier is one of the fastest multipliers. This technique considers all the bits in each column at the same time and compresses them into sum and carry as two bits. Different types of compressors have been used to compress all the bits such as 4:2 compressor, 3:2 compressor, 5:3 compressor[2][3][4]. In this paper, the implementation and analysis of a novel Wallace tree architecture has been implemented. The latency of Wallace tree multiplier has been reduced from 27 to 23.

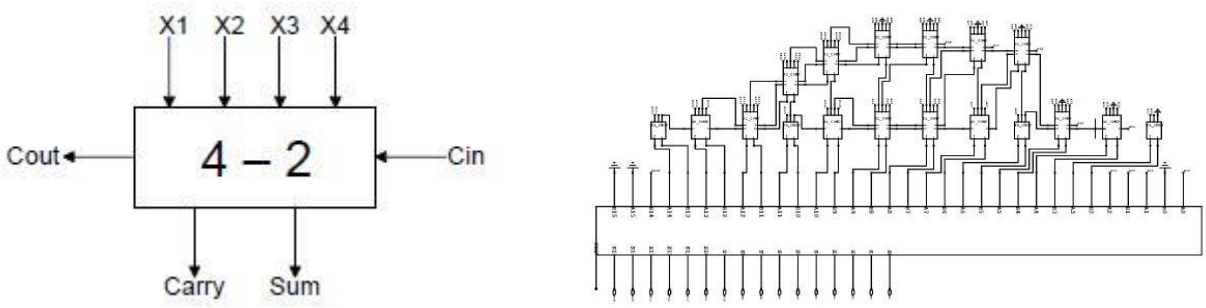

Fig 2: 4:2 Compressor and Compressors based Wallace Tree Multiplier

3. Booth Encoder and Decoder:

Radix-2 booth algorithm does not work properly when the multiplier bits are isolated ones. In such cases Radix-4 or modified booth algorithm is used that begins from grouping multiplicand binary number by three bits and encode them into one of (-2,-1,0,1,2), multiplier bits are multiplied with the generated encoding bits and partial products are generated which is known as booth decoder[6][7].

To recode the multiplicand bit, the modified booth encoder is used in order to lessen the number of partial products. This encoder groups the three bits into a single bit. To produce a single bit, booth encoder takes previous, present and next bit into account [7].

 ISSN: 2321-8169
135 – 138

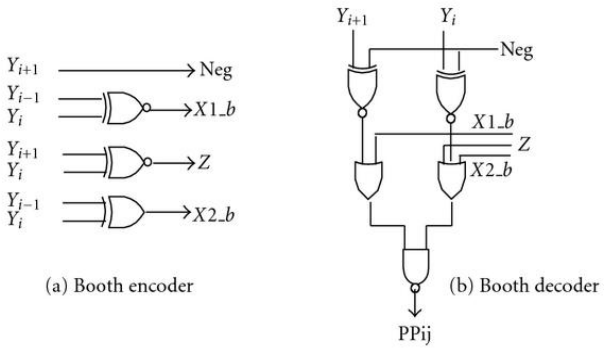

Fig 3: Modified Booth encoder and decoder [6]

4. Spurious Power Suppression Technique:

SPST is one of the proficient low power VLSI techniques to minimize the unwanted switching activities to reduce power dissipation in the circuits [2]. It consists of a Pre-computation logic unit which splits the data range of arithmetic units in two categories, depending on whether it affects the results or not. When a part of MSB data doesn't influence the final result, it is stored by latch circuit of SPST adder to evade unwanted switching activities occurring inside the multipliers or adders which contributes in power reduction to a large extent [8].

A low power SPST based adder has been designed which is then used in multiplier to get reduced power consumption and high speed. The adder is made up of two blocks, one for MSB's known as Most Significant Part (MSP) and another for LSB's known as the Least Significant Part (LSP).The LSP adder is implemented like a conventional adder [8]. MSP differs from the presented design of adder and is modified with the help of pre-computation logic circuits, latches to store unwanted carry and a sign extension circuit. The pre-computation component uses detection unit to find out the unwanted switching activity from the MSB's of the input and required the Cout from LSP part of the modified adder [2]. Pre-computation or detection logic provides three outputs as close, carry_ ctrl and sign [8].

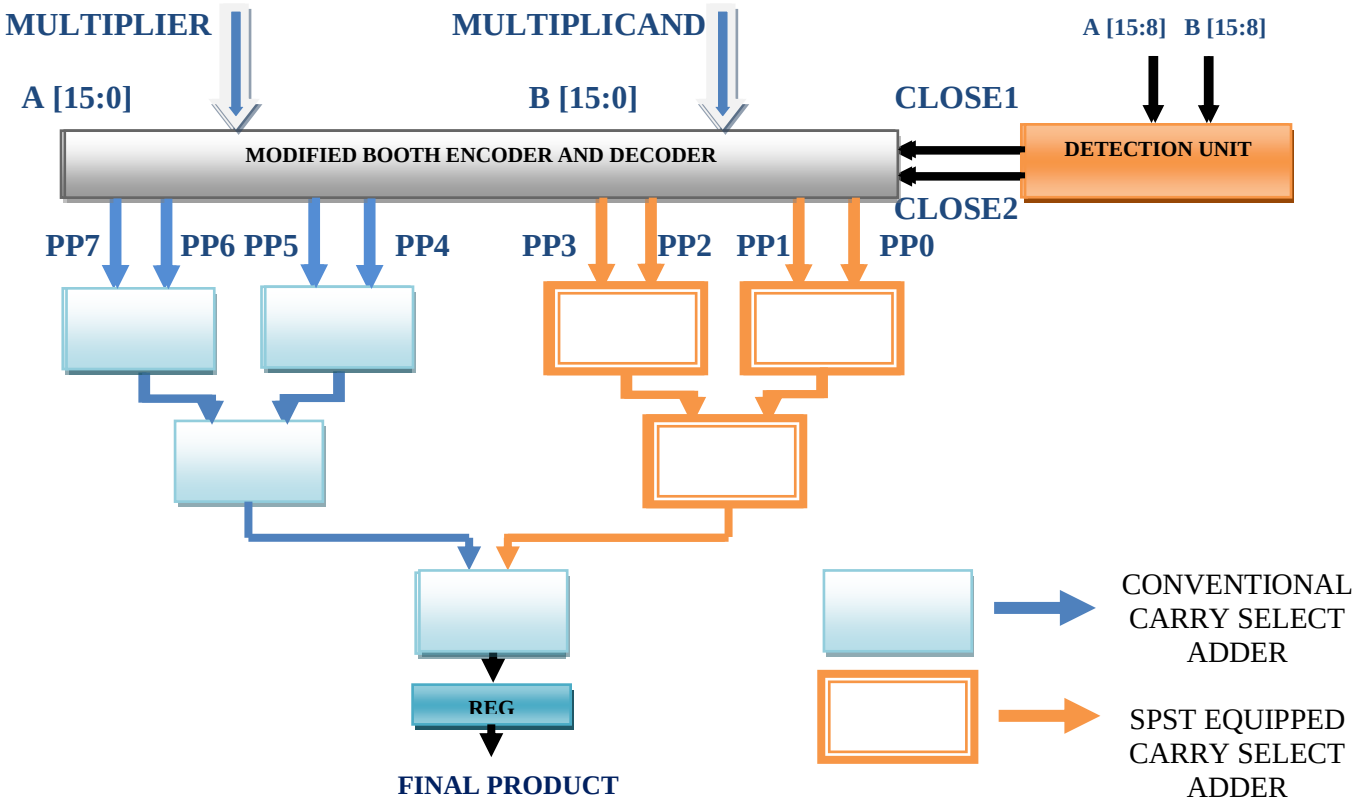

Fig 4: Low power multiplier using SPST adder

Conclusion

In this paper a review has been presented to show the comparison between different techniques that can be used to design low power multiplier. The study shows that the pipelining technique is useful to enhance arithmetic throughput of large area multipliers. On the other hand compressor and MBE based multipliers provide reduced latency of multipliers and speed up the multiplier operation with large area. A SPST based multiplier is used to get reduced latency and low power consumption. The Study shows that SPST based multiplier has achieved ~20-25% of reduced latency and ~45% reduction in power consumption. It can be concluded that SPST based multipliers are much more useful in all aspects.

References

[1] Abu-Khater, A. Bellaouar, and M. Elmasry, "Circuit techniques for CMOS low-power high-performance multipliers", *IEEE J. Solid-State Circuits*, vol.31, no.10, pp.1535-1546, Oct. 1996.

[2] E. de Angel and E.E. Swartzlander, Jr., "Survey of low power techniques for VLSI design," in *Proc. 8th Annual IEEE Int. Conf. Innovative Systems in Silicon*, pp.159-169, Oct. 1996.

[3] E. de Angel and E.E. Swartzlander, Jr., "Low power parallel multipliers," in *VLSI Signal Processing, IX*, pp.199-208, Oct. 1996.

[4] K.C. Bickerstaff, E.E. Swartzlander, Jr., and M.J. Schulte, "Analysis of column compression multipliers," in *Proc. 15th IEEE Symp. Computer Arithmetic*, pp.33-29, 2001.

[5] R. Canal, A. Gonzalez, and J.E. Smith, "Very low power pipelines using significance compression," in *Proc. 33rd Annual IEEE/ACM Int. Symp. Microarchitecture*, pp.181-190, 2000.[25] F. Catthoor, *Unified Low-power Design Flow*

[6] K. Choi and M. Song, "Design of a high performance 32*32-bit multiplier with a novel sign select Booth encoder," in *Proc. 2001 IEEE Int. Symp. Circuits and Systems*, vol.2, pp.701-704, May 2001.

[7] N.-Y. Shen and O.T.-C. Chen, "Low-power multipliers by minimizing switching activities of partial products," in *Proc. 2002 IEEE Int. Symp. Circuits and Systems*, vol.4, pp.93-96, May 2002.