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Design of Asynchronous Viterbi Decoder for Low Power Applications

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***Abstract*—** In todays digital communication systems, convolutional codes are broadly used in channel coding techniques.The viterbi decoder due to its high performance is commonly used for decoding the convolutional codes. Fast developments in the communication field have created a rising demand for high speed and low power viterbi decoders with long battery life and low weight. Despite the significant progress in the last decade, the problem of power dissapation in the viterbi decoders still remains challenging and requires further technical solutions.In this paper we proposed the methods for survivor path storage and decoding as Register Exchange Method (REM) and Hybrid Register Exchange method (HREM). REM cosumes large power and area, due to huge switching activity.The problem of switching activity of Viterbi decoder can be reduced by combining Traceback and REM and the method called Hybrid Register Exchange Method (HREM). The Viterbi decoder is designed using REM and HREM and simulated on Quartus tool and power is calculated on Power play power analyzer. As the switching activity is reduced in HREM as compared to REM the viterbi decoder achieves reduction in power in HREM as compared with REM .For further reduction in power of viterbi decoder we proposed asynchronous techniques like handshaking protocol. Here we designed the Asynchronous Viterbi decoder by using 2 phase dual rail encoding (LEDR)

Keywords- *Asynchronous Viterbi decoder, REM, HREM, Handshaking Protocol, LEDR*

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I. INTRODUCTION

The Viterbi decoder algorithm proposed in 1967 by Andrew J. Viterbi is a decoding process for convolution codes in memoryless noise. Viterbi decoder algorithm is an exact recursive algorithm for finding the shortest path through a trellis, and thus is actually an optimum trellis decoder. it is capable of handling extremely high speeds (tens of megabits). In Mobile station baseband modem [3], the Viterbi decoder consumes more than one-third of the chip area and the power dissipation of the baseband modem Therefore, a low-power implementation of the Viterbi decoder is a significant practical matter.

For viterbi decoder [10] there are two well known methods for survivor path storage and decoding, the Trace- back method (TBM) and Register Exchange method (REM). In trace-back method, memory requirement is high. TBM is the preferred method used in Viterbi decoders having large constraint length and high performance. However, the TBM has drawbacks, which requires last-in-first-out (LIFO) buffer and has to use multiple read operations for high speed operation. This multiple operation results in complex control logic. The REM is logically simple, but it will consume large power and area, due to huge switching activity. The problem of switching activity of viterbi decoder can be reduced by combining TB and REM that is Hybrid Register Exchange Method (HREM).

The following sections are arranged as follows .We first briefly review the Convolutional Encoder and Viterbi Decoder with all components in sections II & III and about decoding methods using REM, HREM and MTHREM in section IV. At last in section V we discuss about the handshaking protocols i,e 4 phase and 2 Phase dual rail encoding (LEDR) to make the system asynchronous for low power consumption

II. CONVOLUTION ENCODER

A Viterbi decoder and a convolutional encoder operate by finding the most likely decoding sequences for an input code symbol stream. A convolutional encoder is selected for error-correction with digital mobile communication. Binary convolution encoder can be implemented using shift registers and exclusive-OR gates (Modulo-2 adder) .A Convolution code is defmed by three integers: n, k and K, where n is termed as code rate=1/2, k is the number of input bits and K is called constraint length. The constraint length signifies the number of k-bit shifts over which a single information bit can influence the encoder output.

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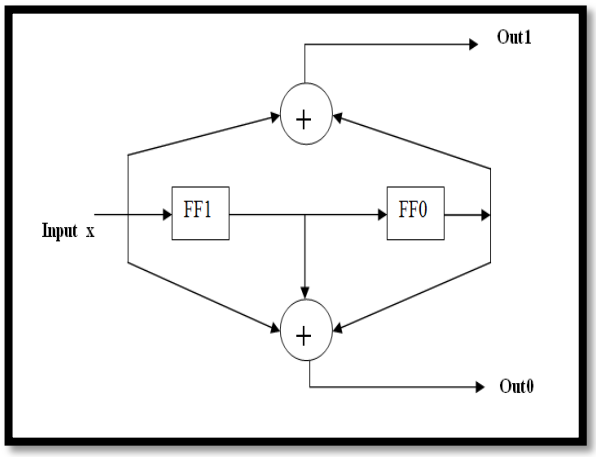

Figure 1. Block diagram of convolutional encoder

K=3, k=1, n=2

$$Out0 = Input \oplus FF1 \oplus FF0 \quad (1)$$

$$Out1 = Input \oplus FF0 \quad (2)$$

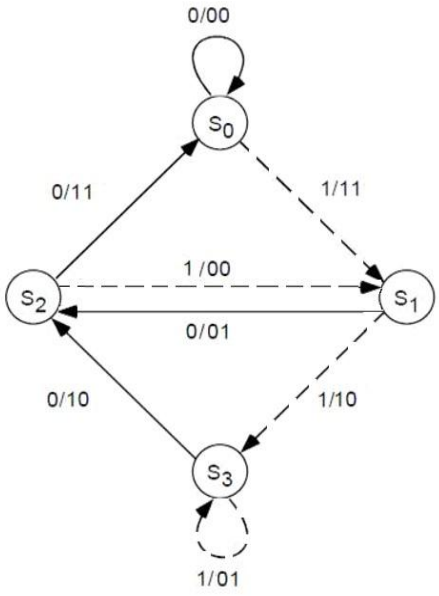

Figure 2: State Diagram of Encoder

III. VITERBI DECODER

At the destination, the decoder utilizes the trellis diagram to decode the received stream by finding the sequence with the maximum likelihood. Viterbi decoder consists [11] of three basic computation units. The branch metric Unit (BMU), the Add-Compare-Select Unit (ACSU) and the Trace Back Unit (TBU). The BMU calculates the branch metrics by Hamming distance or Euclidean distance, and the ACSU calculates a summation of the branch metric from the BMU and previous state metrics, which are called the path metrics. After this summation, the value of each state is updated and then the survivor path is chosen by comparing path metrics. The TBU processes the decisions made in BMU and ACSU, and outputs the decoded data.

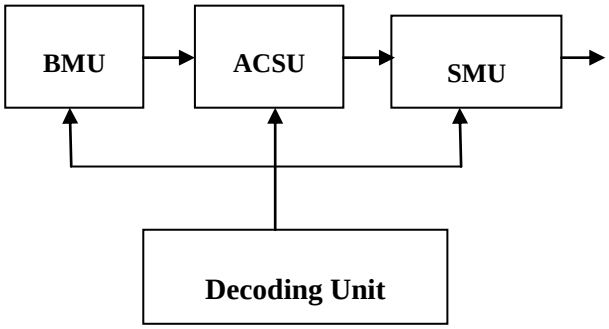

Figure 3. Viterbi Decoder

IV. DECODING METHODS

A REGISTER EXCHANGE METHOD

The approaches are often used to record survivor branches are Traceback & Register-exchange Method As shown in Figure4. a register is assigned to each state contains information bits for the survior path throught the trellis.Total number of states and the corresponding registers requires are 2^m .The register keeps partially decoded output sequence along the path.The register exchange method eliminates the need to traceback since the register of final state contains the decoded output, but it requires the complex hardware due to the need to copy the content of all the registers from state to state at every time.so power consumption of Viterbi decoder is very high.

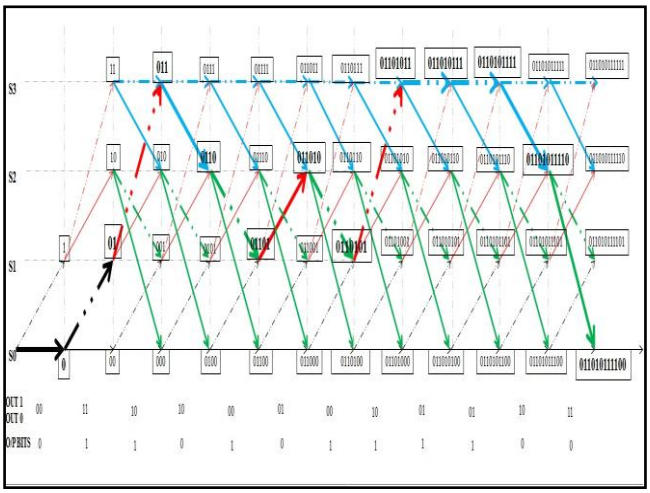

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Figure 4. Register Exchange Method

B HYBRID REGISTER EXCHANGE METHOD

Hybrid Register Exchange method is combination of register exchange method and Traceback method hence the name Hybrid register exchange method. This method reduces the

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switching activity and power.Here we are using the property of trellis is that ,for m cycles the data bits will be the corresponding present state bits irrespective of the initial state from where the data gets transferred.To find the initial state we have to traceback through an 'm' cycles by observing the survivor memory ,and then transfer the partial decoded data from an initial state to the next state which is m cycle later (not at subsequent cycle as in REM) and the present decoded data will be the present state itself. The memory operation is not in every cycle, and it gets reduced by factor of m. Also, the shifting data from one register to another is reduced that is the switching activity and ultimately the power consumption will get reduced as shown in fig.5

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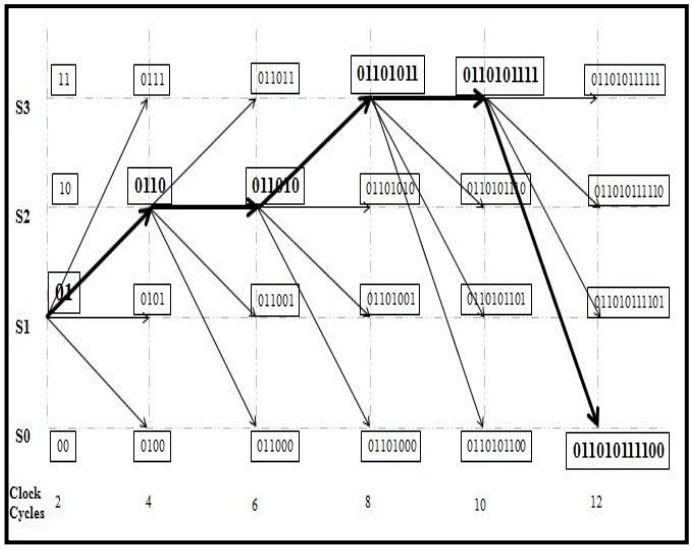


Figure 5. Hybrid Register Exchange Method

V. ASYNCHRONOUS VITERBI DECODER

All parts of a Synchronous design are clocked, even if they perform no useful function.The clock line itself is a heavy load, requiring large drivers, and a significant amount of power is wasted just in driving the clock line. There are synchronous solutions to these problems such as clock-gating. However, the solutions are complex

The efficient way for low power is asynchronous architecture, where timing is managed locally. Instead of providing a global clock we can use local clocks to reduce power consumption

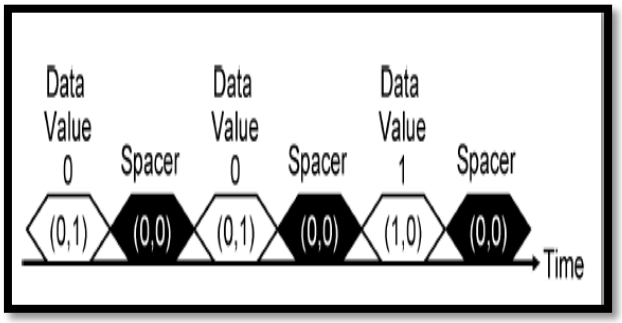
Asynchronous circuits are composed of blocks that communicate to each other using handshaking via asynchronous communication channels in order to perform the necessary synchronization, communication and sequencing of operations.

Power consumption can also be reduced further by using Handshaking Protocols. The appropriate data wire is sent high (the choice of wires determines the bit being transmitted.) Once the receiver has read the bit, the acknowledge is set high The data wires are reset. The acknowledge is reset Once this is complete the next bit of data can be transmitted along the channel.

There are two types of delay encoding:

I) **4 phase dual rail encoding** :

Each bit data is represented by two wires. "01"represents logic 0, while "10" represents logic 1. "00" state is a null state. Sender sends spacer (0, 0) after a data value. The receiver knows the arrival of a data value by detecting the change of either bit: 0 to 1. The drawback of the 4-phase dual-rail encoding is low throughput because of insertion of spacers.

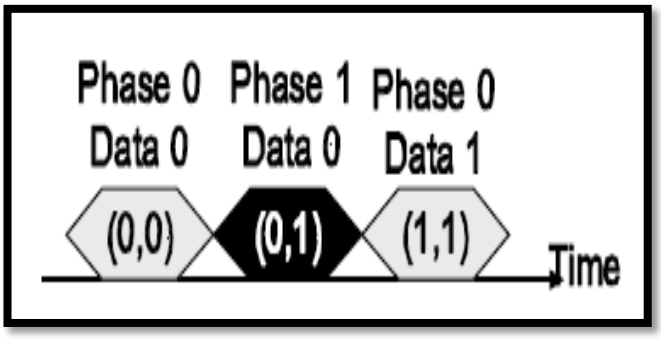


	Codeword (t, f)
Data 0	(0,1)
Data 1	(1,0)
Spacer	(0,0)

Figure 6. 4 phase dual Rail Encoding

II) Level-encoded dual-rail (LEDR)

LEDR signalling is a delay insensitive data encoding scheme that encodes two wires, or "rails", to encode one bit of data.In LEDR encoding, no spacer is required.Each data value has two types of code words with different phases. Here sender sends data values alternately in phase 0 and phase 1.Because no spacer is required, the number of signal transitions is half of four-phase dual-rail encoding.As a result, the throughput is high and the power consumption is small.



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		Code word (V, R)
Phase 0	Data 0	(0,0)
	Data 1	(1,1)
Phase 1	Data 0	(0,1)
	Data 1	(1,0)

Figure 7. LEDR encoding

The code word consists of V (Value bit) and R (Redundant bit). The value V is encoded as in a synchronous circuit. The redundant bit R is defined by EXOR-ing V and Phase so that R includes the information on Phase. The sender sends data values alternately in phase 0 and phase 1

we have implemented LEDR encoding to make the viterbi decoder asynchronous for futher reduction of dynamic power In designing of Asynchronous Viterbi decoder the system clock called global clock which is of 5 Mhz is divided into two local clocks which is of 2.5 Mhz .Both the local signals works on handshaking between all units of viterbi decoder and maintain synchronization to decode the sequence even if error bit occurs.At last the complete design is simulated and power analysis is done on Quartus Power play power analyzer and it is observed that the dynamic power is less in asynchronous system as compared to synchronous Viterbi decoder

VI. PROPOSED ARCHITECTURE OF ASYNCHRONOUS VITERBI DECODER

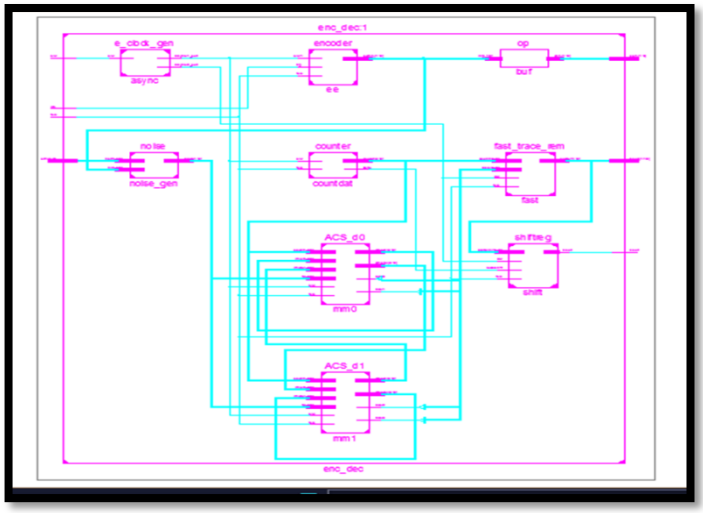

Figure 8 RTL View of Asynchronous Viterbi Decoder

As shown in figure 8 a controller named e_clock_gen has been designed which generates two local signals of 2.5 Mhz

VII. SIMULATION RESULTS:

As shown in figure 9 and 10, here 12 bit sequence 011010111100 has been applied and after 13th clock cycles we got the decoded data serially at Sout pin using REM and HREM decoding methods respectively.

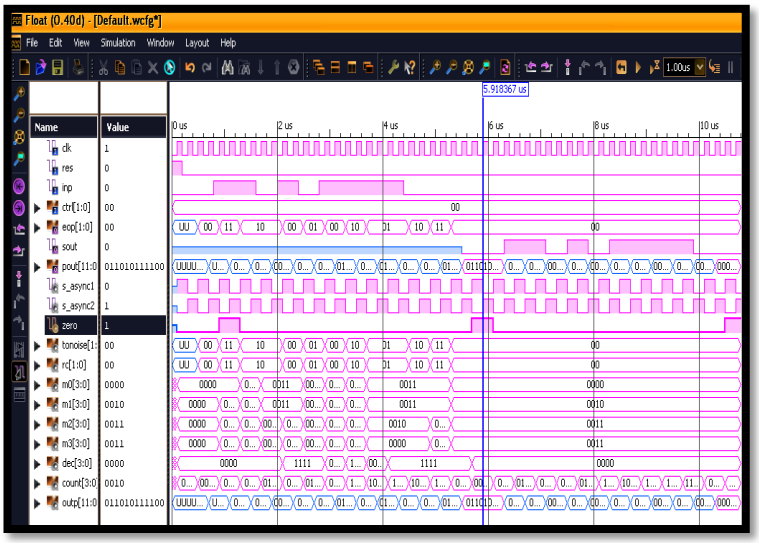

Figure 9 Asynchronous Viterbi decoder using REM

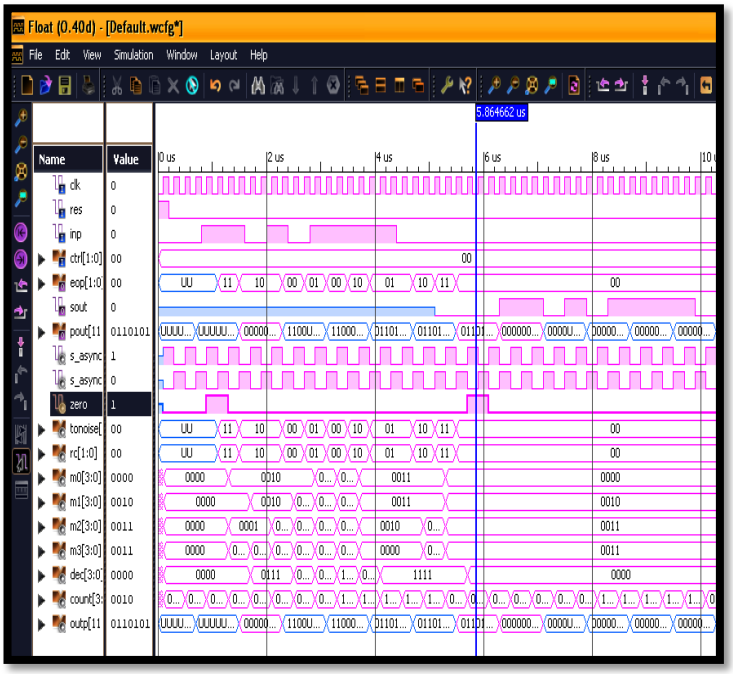

Figure 10 Asynchronous Viterbi decoder for HREM

TABLE I: Dynamic Power Analysis Using REM & HREM

Decoding Methods	Total Power (mW)	Dynamic Power (mW)	Static Power (mW)
Synchronous REM	64.94	0.29	58.84
Asynchronous REM	65.54	0.16	58.84
Synchronous HREM	64.74	0.17	58.84
Asynchronous HREM	64.67	0.10	58.84

VIII. CONCLUSION

In this paper we designed Low power Asynchronous viterbi decoder using LEDR encoding for Register Exchange and Hybrid Register Exchange methods for constraint length K=3 and code rate 1/2.The design of Asynchronous viterbi decoder for input bit sequence 011010111100 has been simulated and Power analysis is done using Quartus software.It has been observed that as the switching activity is less in HREM than REM the dynamic power for Asynchronous Viterbi decoder using HREM method is less as compared to REM.

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