Efficient Implementation of Multilevel inverter with new modulation scheme for Reducing THD

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***Abstract*—** This paper proposed an improved phase disposition pulse width modulation (PDPWM) for a modular multilevel inverter which is used for Photovoltaic grid connection. This new modulation method is based on selective virtual loop mapping, to achieve dynamic capacitor voltage balance without the help of an extra compensation signal. The concept of virtual submodule (VSM) is first established, and by changing the loop mapping relationships between the VSMs and the real sub-modules, the voltages of the upper/lower arm's capacitors can be well balanced. This method does not requiring sorting voltages from highest to lowest, and just identify the MIN and MAX capacitor voltage's index which makes it suitable for a modular multilevel converter with a large number of sub-modules in one arm. Compared to carrier phase-shifted PWM (CPSPWM), this method is more easily to be realized in field-programmable gate array and has much stronger dynamic regulation ability, and is conducive to the control of circulating current and Power quality injected into the grid. The maximum power point tracking is achieved with a fuzzy logic controller. The validity of the proposed system is confirmed by simulations.

***Index Terms*—** Cascaded multilevel inverter, Dynamic voltage balance, modular multilevel converter (MMC), phase disposition pulse width modulation (PDPWM), Photovoltaic (PV) grid-connected, selective virtual loop mapping (SVLM), Voltage Balancing, distributed maximum power point (MPP) tracking (MPPT) ,Total harmonic distortion(THD).

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I. INTRODUCTION

In recent years, with the development of a large-scale Photovoltaic (PV) power plant system, as well as smart grid and multilevel technologies, higher requirements in voltage level, modular structure, and flexibility and reliability of the next-generation large-scale PV grid-connected inverter have been put Forward [1]. The topology features include the following:

1) distributed location of capacitive energy storages.
2) Flterless configuration for standard machines or grid co n-verters [high-
level number, low total harmonic distortion(THD)].T he PV system should maintain the connection of the inverter and the grid in addition to providing support to the grid.
3) *Power quality control:* More stable power supply performance could be achieved by introducing suitable inverter control strategy including voltage stability, phase regulation, active filter [3], etc.

The aforementioned requirements drive the research and development of the next-generation PV inverter [1], and the topologies of utility PV inverters are moving toward multilevel structure [4], [5], which could provide better harmonic spectra and reduce the weight of the filtering components. In many of the multilevel structures, a modular multilevel converter (MMC) has attracted many researchers recently. MMC-related application research has mostly concentrated on high-voltage direct current transmission [6], high-power motor drives [7], integrated energy storage [8], and medium-voltage STATCOM [9]. The MMC used in the PV grid-connected system is just mentioned in [10] and [11]. The reasons of this situation are as follows: 1) MMC-related research is mostly in theoretical research stage [12], [13];

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2) the characteristic of the photovoltaic power generation is that PV panels are intermittent sources, and their output voltages continuously vary; the dc link's voltage has to be regulated to keep them working in maximum power point tracking (MPPT) status; 3) the dynamic voltage balance has to be considered in multilevel PWM, while the system stability would be damaged by adding improper signals to the reference voltage [14]; and

4) the unique circulating current of the MMC will increase the system losses and is not conducive for improving the efficiency of the inverter output [15], [16], and the most important point is that the uncontrolled circulating current threatens the stability of the MMC.

Among them, the first two points do not seem to be big problems, because as a new modular converter for medium- and high-voltage applications, the MMC has been tested and works well in a back-to-back structure and has much better four-quadrant performance. So, the third and fourth points are the keys to MMC used as a PV inverter. Many papers have discussed MMC modulation methods. The amplitude modulation [17], [18] has been widely used in the HV-dc system; its core idea is to first calculate how many sub-modules should be put into action, and the capacitors' sorting voltage and the final working sequence should be determined by the direction of the arm current. The method is simple and practical, but there are frequent sorting issues with the capacitor voltage which would be a burden to the controller if the number of sub-modules is large [19]. Phase-shifted pulse width modulation (PSPWM) is a more in-depth method and also studied in the field of MMC modulation [20], [21]. In order to balance the capacitor voltage, an extra signal generated by a PI regulator of each sub-module has to be added to both the upper and lower arms' modulation signals. It means that a specialized balance controller has to be designed and with the increase of levels, the difficulty of control will increase and bring the risk of instability. At the same time, some new PWM methods have been proposed with different purposes, for example, the fundamental switching frequency modulation [22] and the improved sub-module unified PWM (SUPWM) [23].

This paper proposes a new selective virtual loop mapping (SVLM) method based on phase disposition PWM (PDPWM) which has voltage balance capability. The concept of virtual sub module (VSM) is established, and by changing the mapping routines between the VSM and the real sub-module (RSM) with SVLM, the capacitor voltages of the upper and lower arms can be balanced even if the inverter loses its symmetry. The method has been designed to consider the following situations: 1) no extra signal should be added to the reference voltage to provide a good basis for the suppression of the circulating current; 2) the possibility of a large number of sub-modules in one arm;

3) retain the equivalent switching frequency of the PDPWM;

4) it could be easily realized in field-programmable gate array (FPGA) for a large-scale converter which has a large number of sub-modules. The method is verified through simulations and experiments.

II. MODULAR MULTILEVEL PV INVERTER

A. *Modulation Principles*

Fig. 1(ref. iosr journals paper id: 7584) shows the single-phase equivalent circuit of the MMC, which has two arms including the upper arm and the lower arm, with each arm having *N* sub-modules (SM), one buffer inductor *L*, and equivalent resistor *R*. The dc link of the MMC is floated or connected to high-voltage sources depending on the working purpose of the converter. The output of the converter is the connection point of the upper and lower arms. L_s is the ac-link inductor, and Z_0 is the equivalent impedance of the ac side.

The working states of SM are shown in Table I (ref. iosr journals, paper id: 7584). Each SM has two states ("ON" and "OFF"), and the corresponding output voltage (U_{sm}) of the SM is V_c or 0. The capacitor will charge

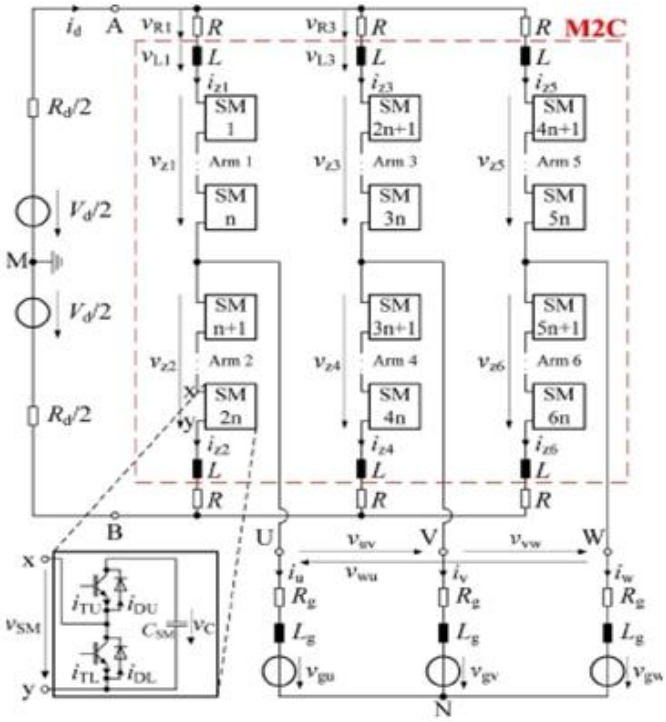

Fig.1. Simulation model for the M2C

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TABLE I HALF-BRIDGE SUBMODULE WORKING STATES

mode	S1	S2	Usm	Ism	state	capacitor
1	1	0	Vc	>0	on	Charging
2	1	0	Vc	<0	on	discharging
3	0	1	0	>0	off	Unchanged
4	0	1	0	<0	off	Unchanged

or discharge during the period of the "ON" state of the SM depending on the direction of I_{sm} . For example, if $I_{sm} > 0$, the capacitor would be charged, and if $I_{sm} < 0$, the capacitor would be discharged. The capacitor voltage will be kept while the SM is "OFF."

B. Basic Structure and Control

There are two structures which can be used in medium- and high-voltage PV grid-connected inverters with MMC: single-stage and two-stage structures. The series-connected PV modules of a single-stage structure access the dc link directly, while in a two-stage structure the procedure is different: PV panels could be connected to the dc link by cascaded dc/dc circuits [24], [25]. The differences are that voltage ripples of the single-stage structure are bigger than those of the two-stage structure, and the two-stage structure has more complex control [26].

Fig. 2(ref. Iosr journals, paper id: 7584) shows the control block diagram of a modular multi-level PV inverter where $U_{d\,cref}$ is the reference of the dc-link voltage and $U_{d\,c}$ is the real dc-link voltage; they are compared with each other to produce the active reference current $i_{d\ ref}$ after the PI controller. $i_{q\ ref}$ is the reactive reference current. U_s (a, b, c) is the ac-side grid voltage and I (a, b, c) is the output current of the MMC. S_j $(1,. . .,2N, j = a, b, c)$ are the PWM signals of the MMC.

It can be seen that the reference voltage can be acquired by decoupled control, and the circulating current suppression compensation signal should be added to it. Meanwhile, it is no longer possible to balance the system capacitor voltage dynamically

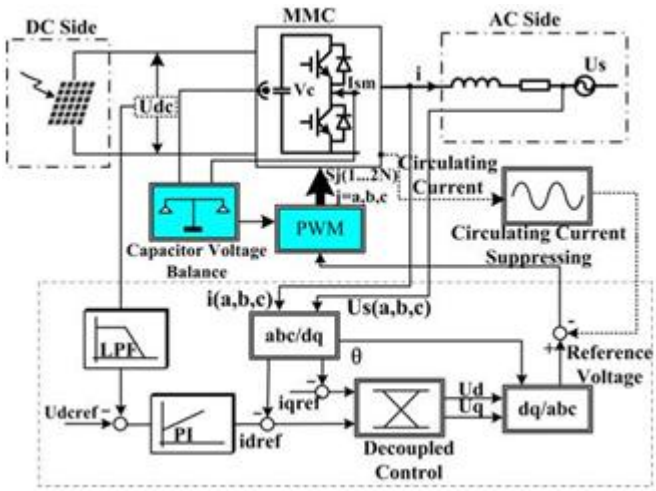

Fig. 2. Modular multilevel PV inverter overall control block diagram.

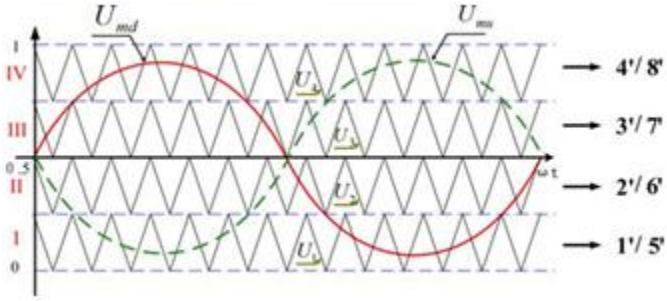

Fig. 3. Transfer relationships of VSM.

by generating the appropriate balance compensation signal, but solely by the adjustment of the PWM method. This approach has the advantage of not only avoiding excessive compensation sig-nal mutual interference (which increases system stability), but also provides a good basis for circulating current suppression and promotes high dc voltage utilization ratio.

II.COMPARISONS OF THE MMCC FAMILY

Terminology	SSBC (Fig. 2(a))	SDBC (Fig. 2(b))	DSCC (Fig. 3(a) or (b) with (c))	DSBC (Fig. 3(a) or (b) with (d))
Main objectives	Positive-sequence reactive power and/or active power	Negative-sequence reactive power and/or active power	Rectification and inversion Negative-sequence reactive power	Rectification and inversion Ac-ac direct conversion
Cell-count ratio	1	$\sqrt{3}$	4	2-4 (depend on circuit design)
Circulating current	No	One degree of freedom	Two or three degrees of freedom	Two or three degrees of freedom
Buffer inductor	No	No	One inductor per leg in Fig. 3(a) Two inductors per leg in Fig. 3(b)	One inductor per leg in Fig. 3(a) Two inductors per leg in Fig. 3(b)
Grid inductor	Yes	Yes	Yes in Fig. 3(a) No in Fig. 3(b)	Yes in Fig. 3(a) No in Fig. 3(b)
Motor drives	No, but limited exceptions exist.	No, but limited exceptions exist.	Fans and blowers	Fans and blowers
Grid applications	STATCOM (voltage regulation) Battery energy storage system	STATCOM (flicker compensation) Battery energy storage system	HVDC/BTB system STATCOM (flicker compensation)	Wind/solar power conditioning New matrix converter
Practicability	+++++	+++	++++	++

TableII summarizes comparisons among the four MMC members from various points of view. Generally, the SSBC ad SDBC are similar in application, while the DSCC and DSBC ae similar in circuit configuration. This suggests that a group of te SSBC and SDBC has a significant difference in performance ad application from that of the DSCC and DSBC. The differene results mainly from two additional dc or ac terminals existing n Fig. 3(a) and (b). The "cellcount ratio" in the third row of Table I means the ratio of the cell count of each MMCC member wih respect to that of the SSBC under the following assumption: the insulatedgate bipolar transistors (IGBTs) used in the four MMCC members have the same blocking voltage, and the four MMCC members have the same power and voltage ratings. As a result, the IGBTs have different current ratings because the count of the IGBTs is different each other. The "practicabilit" in the last row of Table I includes technical aspects as well s the market size of each member.

A. Three-Terminal and Five-Terminal Circuits

Both SSBC and SDBC are the socalled threeterminal circuit if the neutral point of star connection is neglected from the SSBC. This makes it impossible to apply both converters to motor drives as long as a single common dc soure is available. However, both converters are applicable to motor drives when available are galvanically isolated multiple c voltage sources based on battery modules.

On the other hand, both DSCC and DSBC are "five terminal circuits" because both are allowed to use the two neutral poins of starconfigured circuits as the two dc terminals. These termin- als can be connected to the dc output terminals of a three-phase diode rectifier. This makes it possible to use both DSCC and DSBC as multilevel inverters for motor drives.

B. No Circulating Current in the SSBC

The SSBC has the capability of controlling positivesequence leading and lagging reactive power. Unlike the SDBC, however, the SSBC has no capability of releasing negative-sequence re- active power to the grid or absorbing it from the grid, because no circulating current flows inside the SSBC. Therefore, appli- cations of the SSBC are limited to a STATCOM for positive- sequence reactive-power control, and a BESS devoting itself mainly to active-power control at the lowest cost among the four members. The reason is that the SSBC has a minimum cell count among the four MMCC family members, as shown in Table I.

C. Circulating Current in the SDBC, DSCC, and DSBC

The others, the SDBC, DSCC, and DSBC have the capability of controlling negative-sequence reactive power because they allow a current to circulate among three clusters for the SDBC and a current to circulate through the positive and negative arms in each leg for both DSCC and DSBC. The circulating current plays an essential role in exchanging active power among the three clusters and legs although the circulating current is accompanied by a slight increase in conducting and switching losses. The SDBC has one degree of freedom in the circulating current. The DSCC and DSBC have two degrees of freedom when nothing is installed on their dc terminals, or three degrees of freedom when either a dc voltage source or a dc-link capacitor is connected.

D. Differences Between the DSCC and the DSBC

The circuit configurations of the DSCC and DSBC look similarand their control systems are almost the same. However their applications are different from a practical point of view. The DSCC is applicable to mediumvoltage motor drives for fans, blowers, and compressors. It is also applicable to HVDC transmission systems, and a BTB

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systems for achieving fre- quency change between two power systems with different line frequencies, and/or asynchronous link between two power syst-ems with the same line frequency.

The DSBC is superior to the DSCC in terms of tolerating a broad range of variations in the dc-link voltage, because the DSBC has additional buck and boost functions of the dc-link voltage for rectification and inversion. Therefore, the DSBC is suitable to a power conditioning system (PCS) for renewable re- sources such as wind power and solar power, in which the dc-link input voltage varies with wind and weather conditions. More- over, the DSBC can act as a three-to-single-phase direct fre- quency changer that is similar to a traditional line-commutated cycloconverter using thyristors. However, the DSBC is different from the cycloconverter in terms of unity-power-factor operation at the input side, and three-phase sinusoidal current waveforms at both input and output sides.

IV. PHASE DISPOSITION PWM METHOD

As an important modulation method, carrier disposition (CD) PWM has been widely used in multilevel modulation, and it can be divided into three types: phase disposition (PD), phase opposition disposition (POD), and alternative phase opposition disposition (APOD). For simplicity, this paper will focus on the PDPWM to discuss MMC modulation. PDPWM has been studied for MMC modulation [27], [28]; in order to balance capacitor voltages, rotating carrier waves were used, but it seems that they can only work under symmetric condition.

For convenience, it is assumed that the number of RSMs of the upper and lower arms is 4 (N = 4). And the RSMs are numbered from 1 to 8 (from top to bottom).To improve the PDPWM, the concept of VSM can be first established, which means that the VSMs are not the RSMs, and the PWM output gained by the comparison of the modulation signals and the carriers will be transferred to the VSM at first, and VSMs are numbered by1 to 2N.The transfer relationships are illustratedasFigs.3and4.

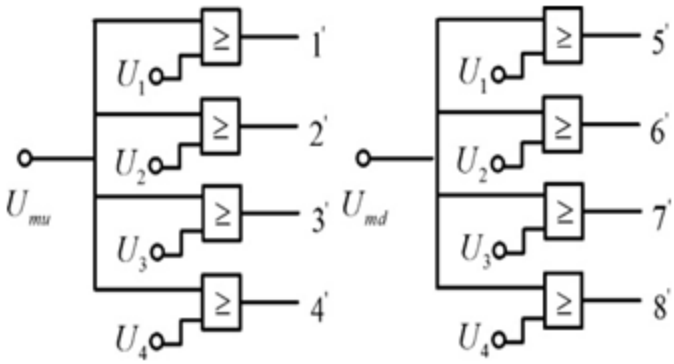

Fig. 4. VSM's input

TABLE III SWITCH COMBINATIONS OF VSM ($2N$ + 1 LEVEL)

Region	1'	2'	3'	4'	5'	6'	7'	8'	Range of Normalized Voltage
I	P1	0	0	0	P5	0	0	0	0 ~ 0.25
II	1	P2	0	0	1	P6	0	0	0.25 ~ 0.5
III	1	1	P3	0	1	1	P7	0	0.5~ 0.75
IV	1	1	1	P4	1	1	1	P8	0.75 ~ 1

P1–P8 is the corresponding PWM signal of each VSM's input.

TABLE IV SWITCH COMBINATIONS OF VSM (N + 1 LEVEL)

Region	1'	2'	3'	4'	5'	6'	7'	8'	Range of Normalized Voltage
I	P1	0	0	0	P5	1	1	1	0 ~ 0.25
II	1	P2	0	0	0	P6	1	1	0.25 ~ 0.5
III	1	1	P3	0	0	0	P7	1	0.5~ 0.75
IV	1	1	1	P4	0	0	0	P8	0.75 ~ 1

P5–P8 is the corresponding negated PWM signal of P1~P4 respectively.

According to Figs. 3(ref. iosr journals, paper id: 7584) and 4, $2N$ + 1 level modulation truth table can be shown as in Table II (ref. iosr journals, paper id: 7584). 1 to 4 are for the upper arm's VSMs, while 5 to 8 represent the lower arm's VSMs. Here, "1" means that the corresponding VSM is ON while "0" means that it is OFF. P1–P4 are the comparison results of the carriers and the modulation signals. The range of normalized voltage corresponds to Regions I–IV. In each region, each VSM has its own PWM signal. For example, when the modulation signal U_{mu} is in Region II, P2 and P6 will be transferred to VSMs 2 and 6 , while at the same time, "1" will be output to VSMs 1 and 5 , and "0" will be output to VSMs 3 , 4 , 7, and 8 . Other regions can also be analyzed like this.

Table III (ref. Iosr journals, paper id: 7584) shows the N + 1 level modulation, compared with Table II; the driving signals of the lower arm's VSMs are complementary to the upper arm.

Because the $2N$ + 1 level modulation has higher dc-link voltage ripple, this paper chooses the N + 1 level modulation as the PV grid-connected inverter's modulation method.

The driving signals of VSMs would be transferred to the RSM by the following mapping rules described in the next section.

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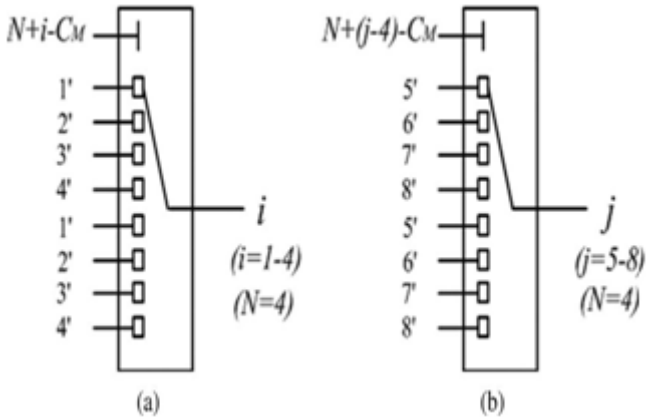

Fig. 5. VLM's mapping relationship. (a) Upper arm's mapping. (b) Lower arm's mapping.

IV.CAPACITOR VOLTAGE VIRTUAL LOOP MAPPING BALANCE CONTROL

To solve the submodule capacitor voltage balance control problems, there are two mechanisms: the virtual loop mapping (VLM) method and the enhanced SVLM based on the comparison of capacitor voltage MIN and MAX values.

The VLM's principle is using a count-up counter "C_M " to control the mapping relationships between the VSMs and the RSMs. The C_M 's working frequency can be set equal to the carrier frequency or less, and its counting range is $0 - (N - 1)$. Different counter number means different mappings. The VLM can be realized easily by using multiplexer with single-pass transistor in FPGA like Fig. 6(ref. iosr journals, paper id: 7584) ($N = 4$); the double input buffer (DIB) structure is also used here.

i And j in Fig. 5(ref. iosr journals, paper id: 7584) are the index numbers of the RSM, respectively, which work with the counter to realize the mapping between the VSMs and the RSMs. For example, if $C_M = 0$,

$N + i - C_M = 4 + i - 0 = 4 + i$, VSMs 1 -2 -3 -4 would be mapped to RSMs 1-2-3-4 as shown in Fig. 6(a); likely, if C_M=

1, $N + i - C_M = 4 + i - 1 = 3 + i$, VSMs 4 -1 -2 -3 would be mapped to RSMs 1-2-3-4 [see Fig. 6(b)], and so on.
The VLM's final results of both arms are illustrated in Fig.7 (ref. iosr journals, paper id: 7584). This method can achieve capacitor voltage balance in the case of system symmetry.

V. CAPACITOR VOLTAGE SVLM BALANCE CONTROL

A practical modulation method should not only be effective in a symmetrical system, but also have the ability to regulate dynamically and provide some error correction capabilities to ensure that the system works well under conditions such as error accumulation and device parameter deviation. For example, commonly used phase-shift PWM, by changing the modulation signals of the upper and lower arms to get the dynamic balance adjustment capacity of the capacitor voltage, will bring more harmonics to the arm current, change the circulating current' characteristics, and may cause instability. Therefore, changing the modulation signals to achieve the dynamic adjustment capability would be valid only to a certain extent.

The new method is mainly through the SVLM to achieve the effect of dynamic regulation ability; here, "selective" means just their corresponding index selectively. Before introducing

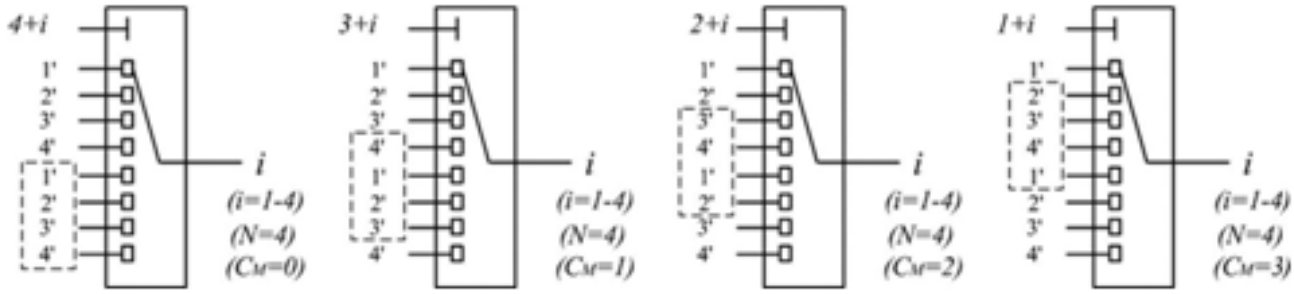

Fig 6. Upper arm's VLM procedures

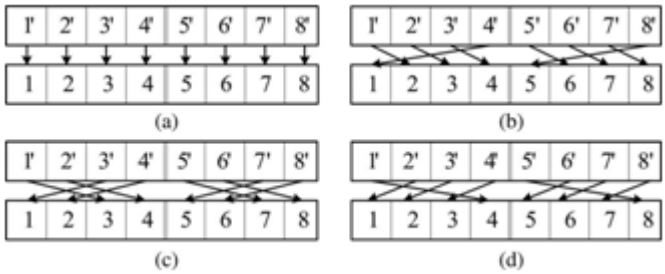

Fig. 7. VLM final results. (a) C_M = 0. (b) C_M = 1. (c) C_M = 2. (d) $C_{M=}3$

the SVLM rules, note that there are four interesting SMs in Table III(ref. iosr journals, paper id: 7584), which are 1 , 4 , 5 , and 8 . VSMs 1 and 8 output PWM in regions I and IV, respectively, and output "1" in other regions. Likewise, VSMs 4 and 5 output PWM in regions IV and I, and output "0" in other regions. Table I shows that if some capacitor voltage of the leg is less than the others (means needing more charge and less discharge), it would be right to map the SMs 1 and 8 to this submodule when the corresponding current I_{sm} is positive and mapping the SMs 4 and 5 to it when I_{sm} is negative.

To achieve the SVLM, it needs to sort the capacitor voltage as [29], [30] described, but frequent sorting is very time consuming, and requires more hardware resources, which would be a large burden especially for high-voltage applications needing more sub-modules. Other disadvantages of sorting are a reduction in system equivalent frequency and an increase in switching losses. Therefore, the actual method of selective mapping in this paper is just picking the MIN and MAX capacitor voltages and their corresponding index directly and make sure that it can be easily implemented in FPGA.

The rules of the SVLM are as follows (just taking the upper arm as an example).

1) First, all of the individual capacitor voltages are compared, and the corresponding RSM indexes of the maximum voltage and minimum voltage are obtained. The MIN index block diagram is shown in 8(a) (ref. iosr journals, paper id: 7584). 8(a) (N = 4). Y is an array, and Y (1) is the first element.$U_{dc1} - U_{dc4}$ are the SM's capacitor voltage of the upper arm separately and they are compared to each other at the same time which means that the time is limited. Y (1) would be equal to the capacitor index having the mini-mum voltage: for example, if the voltage of U_{dc3} is the minimum, Y (1) would be equal to 3. Priority check is just for the case of more than one input of X_1 –X_4 equal to 1, so that X_1 could be set up to the highest priority

TABLE IV PRIORITY CHECK AND INDEX NUMBER OUTPUT TRUTH TABLE OF Y (1)

X1	X2	X3	X4	Y(1)
1	x	x	x	1
0	1	x	x	2
0	0	1	x	3
0	0	0	1	4

x means any state.

TABLE V PRIORITY CHECK AND INDEX NUMBER OUTPUT TRUTH TABLE OF Y (2)

X1	X2	X3	X4	Y(2)
x	x	x	1	4
x	x	1	0	3
x	1	0	0	2
1	0	0	0	1

x means any state.

in the MIN check, while X_4 has the lowest priority. For the MAX check, "≤" would be replaced by "≥," while

Y (2) Provides the corresponding index of the maximum capacitor voltage [see Fig. 8(b)], and X_4 should have the highest priority while X_1 should have the lowest priority.

2) The corresponding truth table of the priority check and index number output function for Y (1) is shown in Table IV(ref. iosr journals, paper id: 7584).
Y (2) can be acquired by the same method (see Table V).

3) The other SMs' indexes except the minimum and maxi-mum capacitor voltages would also be assigned to the Y array by sequence after Y (2). For example, if SM 3 has

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the lowest voltage and SM 2 has the highest voltage, the Y array would be assigned like this, as shown in Fig. 9(ref. Iosr journals, paper id: 7584).

Change the mapping route as shown in Fig. 10(ref. iosr journals, paper id: 7584), N [Y (i)] is the multiport switch selector array, whose index is Y (i) (i = 1–4). *Flag I* is the symbol of the arm's current direction. If the upper arm's current is positive ($I_{jp} > 0$), *Flag I* = 0; N [Y (1)] would be equal to 3, which means that VSM 1 would be mapped to RSM 3. At the same time, N [Y (2)] would be equal to 4, and VSM 4 would be mapped to RSM 2. In contrast, if $I_{jp} < 0$, *Flag I* = 1, N [Y (1)] is

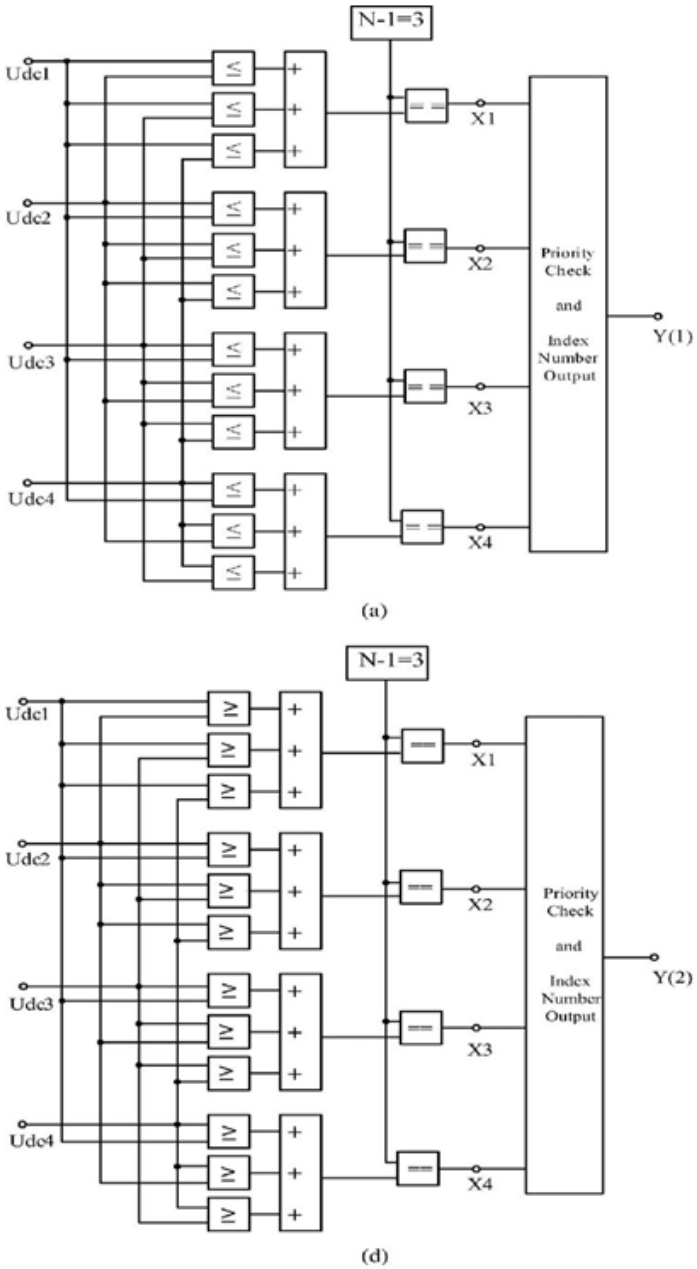

Fig. 8. Index acquirement method of the MIN and MAX voltages. (a) MIN block diagram. (b) MAX block diagram.

assigned to 2, and VSM 4 is mapped to RSM 3, while VSM 1 is mapped to RSM 2. The rest of the mappings follow the aforementioned VLM, as can be seen in Fig. 10(b). Just take Fig. 9 as an example.

If $I_{jp} > 0$

N [Y (1)] = N [3] = 3

N [Y (2)] = N [2] = 4.

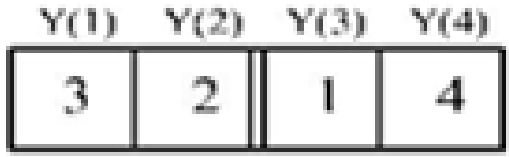

Fig. 9. Assignment of the Y array.

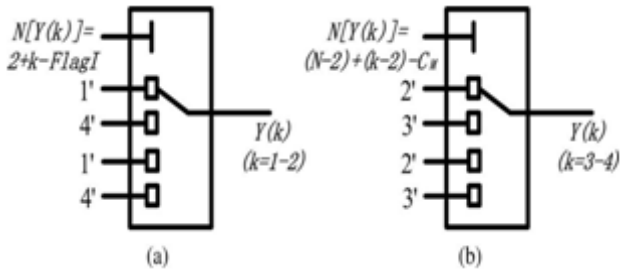

Fig. 10. Mapping route control of each RSM.

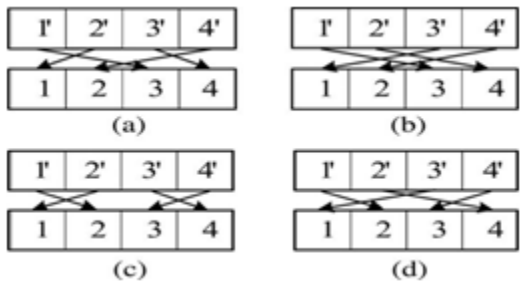

Fig. 11. SVLM. (a) C_M = 0. (b) C_M = 1. (c) C_M = 0. (d) C_M = 1.

If $I_{jp} < 0$

N [Y (1)] = N [3] = 2

N [Y (2)] = N [2] = 3.

At the same time, the rest of the RSMs would still follow the previously described VLM rule. But the maximum counter range of C_M would be set equal to N − 2.

If C_M = 0

N [Y (3)] = N [1] = 3

$N[Y(4)] = N[4] = 4.$

If $C_M = 1$
$N[Y(3)] = N[1] = 2$

$N[Y(4)] = N[4] = 3.$

5) The final mapping route would be as follows: $I_{jp} > 0 (j = a, b, c)$, SVLM is given in Fig. 11 (a) and (b) (ref. Iosr journals, paper id: 7584). $I_{jp} < 0 (j = a, b, c)$, SVLM is given in Fig. 11 (c) and (d).

6) In order to minimize the delay of the PWM signal, a

Synchronous sampling control should be adapted to the SVLM as shown in Fig. 12. U_{mu} is the reference voltage, and Y array is sampled at the intersection point of two triangular carriers. From Fig. 12, it is obvious that the whole processing time of the SVLM is made up of three parts: $t1$ corresponds to the processing time of steps 1 and 2 of the SVLM while $Y(1)$ and $Y(2)$ are acquired, and because all the comparisons are taking place in parallel, the delay would be limited and has no relationships to the number of SMs in one arm. $\Delta t2$ is the forming time of the Y array whose length depends on the modules in each arm (N), and $\Delta t3$ is the transmission delay of the mapping. It can be seen that the delay of $\Delta t3$ is limited which mainly

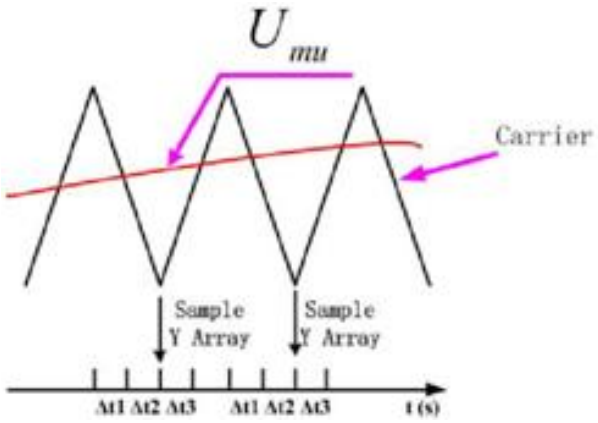

Fig. 12. Synchronous sampling control.

TABLE VI SIMULATION AND EXPERIMENT PARAMETERS

Parameters	Values
No. of PV panels	4
No. of Sub-modules in each arm	4
Sub-module Capacitor C	2200 uF
Arm Inductor L	2 mH
Arm Equivalent Resistance	0.1 Ω
AC Link Inductor L_S	5 mH
Carrier frequency	2400 Hz
AC system voltage Us (rms)	115 V
Power frequency	60 Hz
Transformer ratio	600 V/ 240 V

VI. SIMULATION AND EXPERIMENTS

A. Simulation

In order to verify the validity of the modulation method, a five-level MMC PV single-phase grid-connected simulation model reference to the experimental system was built, while the SVLM would be put into action at 0.5 s. In order to break the symmetry of the system, a resistor of 100 Ω was paralleled to the capacitor of SM 1. The relative simulation and experiment parameters are shown in Table VI. The PV panel is modelled according to the specification of the commercial PV panel from Sanyo, HIP-195BA19.

The control scheme can be designed as shown in Fig. 13. The output waveforms of the simulation system are shown in Fig. 14, and it was assumed that all the PV panels had the same working conditions: irradiance S = 1000 W/m^2 and ambient Fig. 14. Modular multilevel inverter output waveforms. (a) System voltage U_s and output current I_a . (b) Inverter output voltage U_a . depends on the hardware, while $t1$ and $t2$ have almost no impact on the real modulation process.

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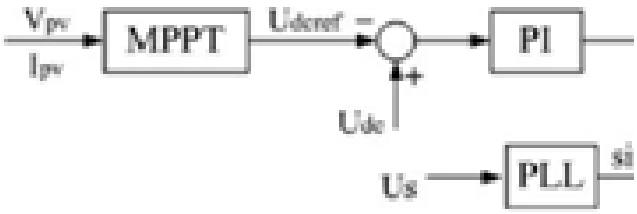

Fig. 13. Control scheme of the single-phase PV grid-connected inverter.

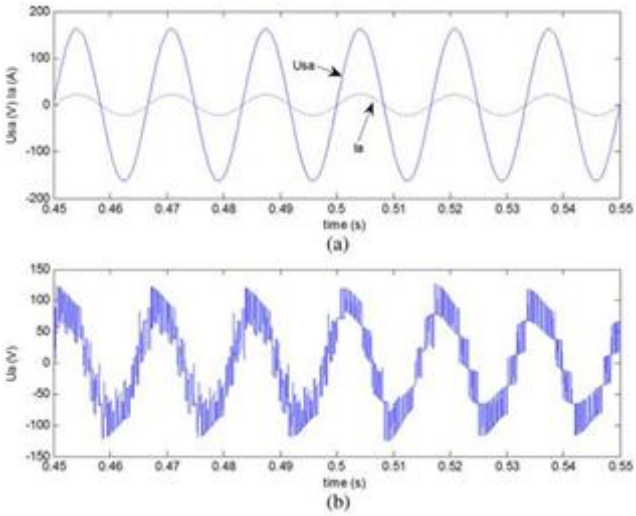

Fig. 15 shows the corresponding capacitor voltages of the upper and lower arms. Since a 100 Ω resistor was paralleled to capacitor 1 of SM 1, its voltage was the lowest one before 0.5s.

temperature 25 °C. Fig. 14(a) shows the system voltage $U_{s\,a}$ of the grid and the inverter output current I_a , which should be synchronous to the grid voltage. Fig. 14(b) shows the output voltage U_a of the modular multilevel inverter. It is clear that the output voltage's ripples were reduced after 0.5 s when the SVLM was ON.

capacitor 1 of SM 1, its voltage was the lowest one before 0.5 s.

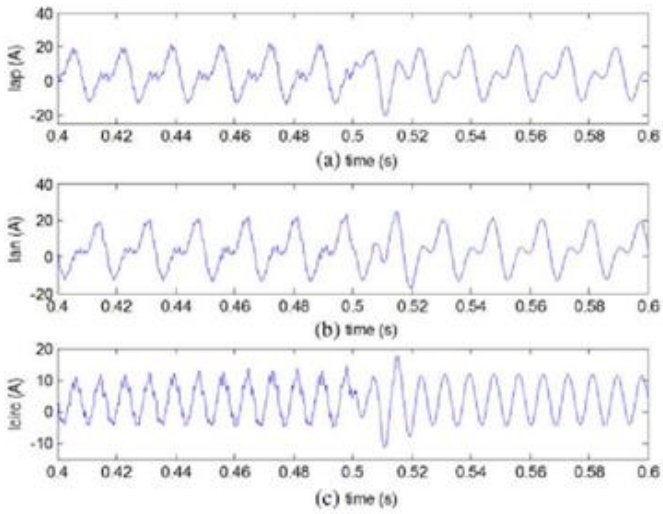

Fig. 16. Simulation showing the upper and lower arms' currents and the circulating current of the leg with the SVLM OFF and turned ON at 0.5 s. (a) Upper arm's current. (b) Lower arm's current. (c) Circulating current of the leg.

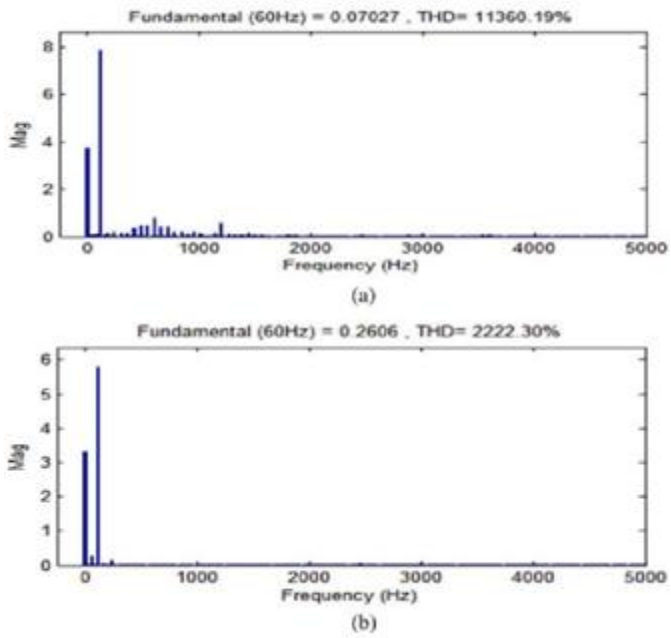

Fig. 17. Harmonics of the circulating current shown in Fig. 16(c). (a) SVLM is OFF. (b) SVLM is ON.

From Figs. 15(b) and (c), the capacitor voltages of the upper and lower arms are balanced quickly since the SVLM was in operation at 0.5 s.

Fig. 16(a) and (b) shows the upper/lower arm's current, and the corresponding circulating current is shown in (c).

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Obviously, the circulating current of the $N + 1$ level modulation mainly consists of dc and second harmonic. The spectrum of the circulating current before and after the SVLM is ON could be seen in Fig. 17, and the high-frequency components of the circulating current could be reduced with SVLM. From these simulation results, it is obvious that the SVLM can work well to achieve the capacitor voltage

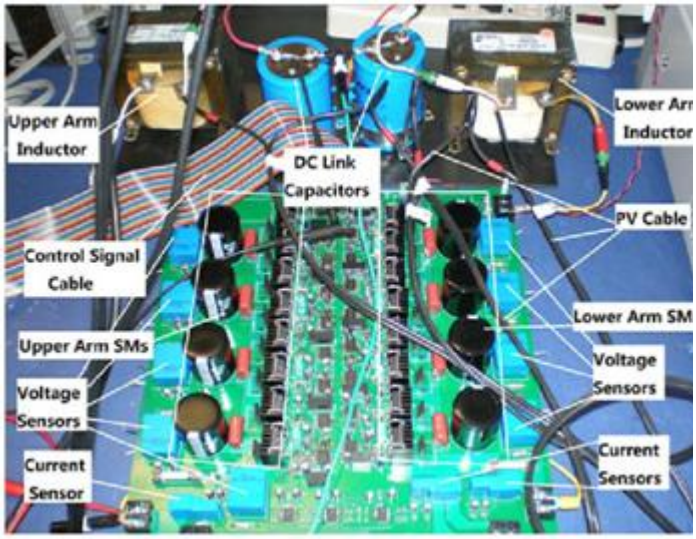

Fig. 18. Photographs of the experimental system.

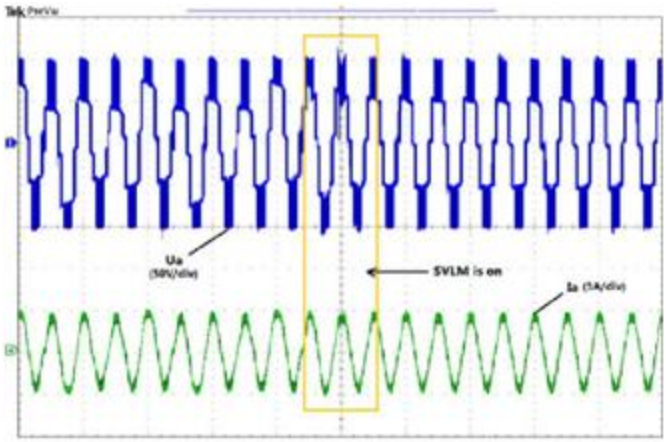

Fig. 19. Experimental output voltage and current of the converter with the SVLM OFF and ON (load is inductor and resistor).

balance. The difference of the capacitor voltage can be greatly reduced, and the system output voltage and current waveforms are improved. Since no additional signals are added to the reference volt-age, the overall characteristics of the MMC do not need to be changed, such as the internal circulating current, which can be observed in Fig. 16(c). This characteristic provides a good basis to eliminate the circulating current further.

B. Experiment

To test the ability of system balance with the new modulation method, a 160-Ω resistor was shunted to the submodule 3 capacitor. The MMC first worked under this unbalanced condition and turned ON the SVLM to balance the capacitor voltage in process. The output voltage and current of inductor and resistor load can be seen in Fig. 19; after the SVLM is turned ON, the voltage output waveform becomes flat, and the unbalance situation was corrected.

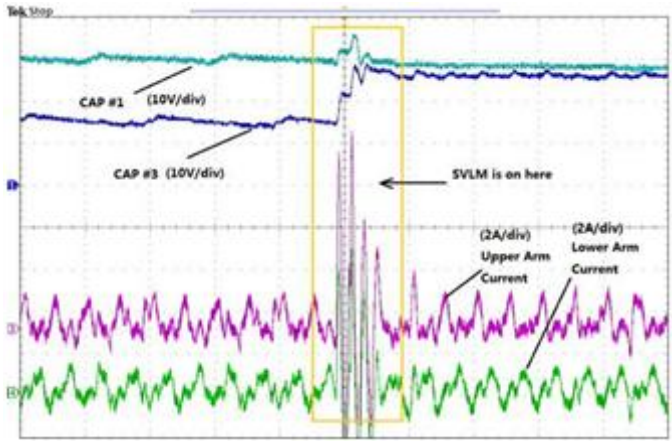

Fig. 20. Experimental capacitor voltage (CAP 1 and CAP 3), and the up-per/lower arm's current with SVLM OFF and ON.

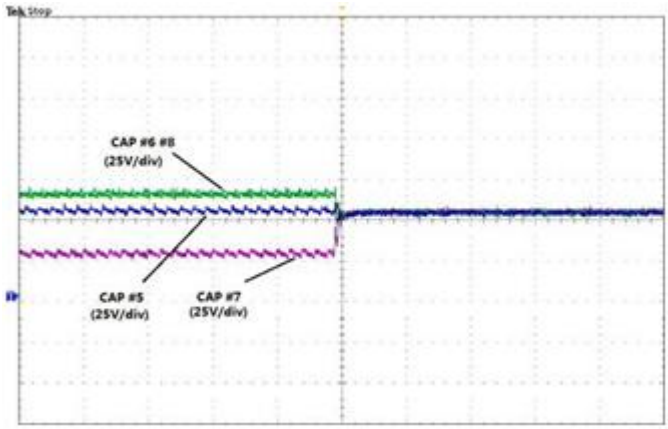

Fig. 21. Experimental capacitor voltage (CAPs 5 to 8) with SVLM OFF and ON.

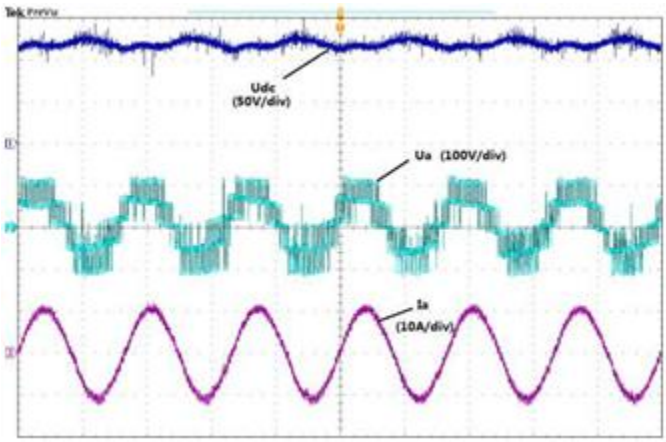

Fig.22. DC-link voltage, output voltage, and output current of the experimental inverter.

The variations of voltages of CAP 1 and CAP 3 are shown in Fig. 20. Obviously, both are close to each other after the SVLM is ON. The same situation also occurs in the lower arm's capacitors which can be seen in Fig. 21. The corresponding variations of the upper and lower arms' currents are also shown in Fig. 20.

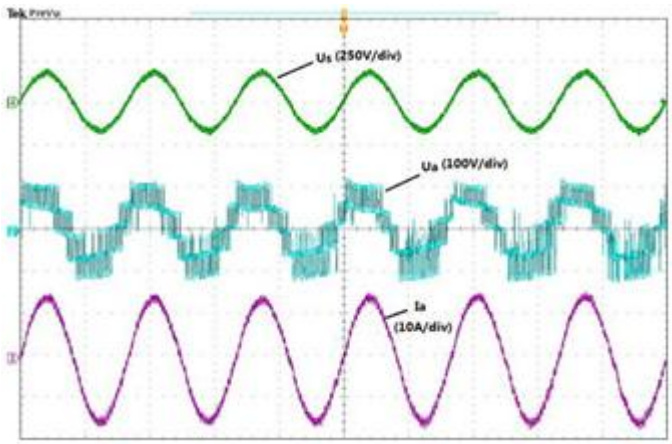

Fig. 23. Grid voltage, output voltage, and output current of the experimental inverter.

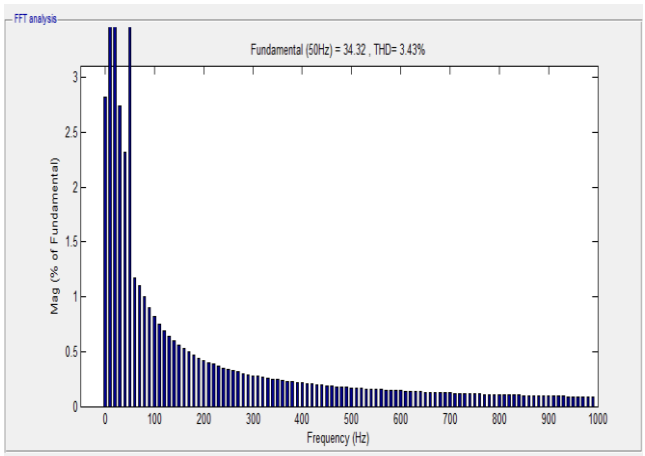

Fig. 24. Harmonic of the output current shown in Fig. 23.

Finally, the new modulation method was used in a PV grid-connected inverter, and the corresponding parameters are the same as those in Table V(ref. Iosr journals, paper id: 7584). Fig. 22 shows the dc-link voltage U_{dc} , the output voltage U_a , and the output current I_a of the inverter.

The experimental results also show that the grid current has the same frequency and phase as the grid voltage and has unity power factor, as shown in Fig. 23.

The THD of the grid current in Fig. 23 is 4.2%, as shown in Fig. 24, which is less than 5%, and meets the power quality standards, like IEEE1547 in the U.S. and IEC61727 in Europe.

VII. CONCLUSION

This paper first discussed the possibilities of the MMC being used as an interface between the grid and PV panels, and proposed an improved SVLM method based on the PD PWM. This method can produce $2N + 1$ and $N + 1$ level outputs in the MMC, and achieve submodule capacitor voltage dynamic balance compensation control while not changing the reference signal. The whole mapping rules are presented and it is easy to be implemented in FPGA. Simulation and experiments were carried out under the conditions of load and grid, and the effectiveness of the method was proved well.

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