Development of 100W Solid State Power Amplifier at 13.56±1MHz

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Abstract— Project aim is the development of a common source class B, cwrf amplifier by using MOSFET. The work includes literature survey, concept, simulation, design, fabrication and testing of the power amplifier. This single stage amplifier of more than 100W output and gain 13dB needs development in the frequency range of 13.56±1MHz. A temperature sensor at the heat sink mounting must be added along with necessary wiring to switch off the dc supply and thereby protecting the circuit in case of overheating. The ultimately developed amplifier needs testing for the frequency response, power gain and output wave shapes etc. by using a set of appropriate instruments.

Keywords- *Solid State Power Amplifier, L-section, MOSFET, Class B*

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I. INTRODUCTION

An amplifier is used to increases the voltage, current or power of a signal. Amplification can be done with a vacuum tube or transistor. In transistors, the electrons passes through the solid material therefore named solid state devices. In power amplifier, voltage and current level of the signal is increased. There are four types of the power amplifier namely class A, class B, class AB and class C. As specified, one MOSFET based class B power amplifier is planned to be used. In the output circuit, the amplified positive half cycle of the input signal is converted in to the full cycle by flywheel effect due to tank circuit.

II. DESIGN METHODOLOGY OF THE 100W SSPA

A. Specifications:

TABLE I. SPECIFICATONS REQUIREMENT OF THE 100W SSPA

Sr. No.	Parameters	Values
1.	Center Frequency	13.56MHz
2.	Bandwidth	±1MHz
3.	Output power	More than100W
4.	Gain	More than13dB
5.	Efficiency	More than 50%
6.	Harmonics	Less than 20dB

B. Selection of the appropiate transistor

The specifications of available MOSFETS in the required frequency range and having appropriate power ratings are studied. The MACOM make n-channel enhancement type MOSFET MRF151 is selected due to its suitable ratings. The stability factor of this MOSFET is found to be 3.1.

III. DESIGN OF THE INPUT CIRCUIT

From the manufacturer's data of MRF151, input impedance Z_{11} = (4.5 – j4.6)Ω and R_G = 50Ω. The source impedance is (50+j0)Ω and the load impedance is (4.5 – j4.6)Ω.
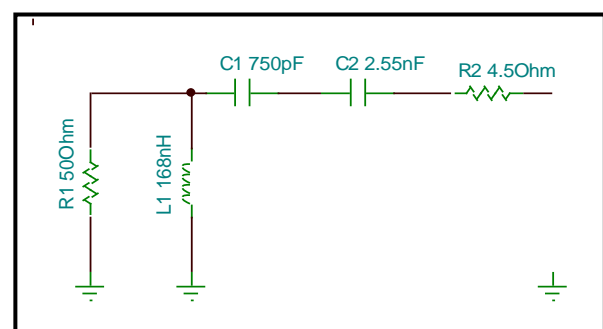

Figure 1: Circuit of input impedance matching

L-section is used for the impedance matching.

As R_G > R_L thus $Q = \sqrt{\frac{R_g}{R_L} - 1}$.

Using given values of R_G and R_L we get, Q = 3.18.

Now, $X_L = Q \times R_L$. Therefore, $X_L = 3.18 \times 4.5 = 14.31\Omega$.
Now, $X_C = R_G/Q = 50/3.18 = 15.72\Omega$.

$L = X_L/2\pi f = 14.31 / (2 \times 3.14 \times 13.56 \times 10^6) = 168nH$.
$C = 1/2\pi f X_C = 1 / (2 \times 3.14 \times 13.56 \times 10^6 \times 15.72) = 750pF$.

IV.   DESIGN OF THE OUTPUT CIRCUIT

A. To design the output matching circuit of high pass type:

From the manufacturer's data of MRF151, output impedance $Z_{22} = (7 - j3.4)\Omega$ and $R_L = 50\Omega$. The source impedance is $(7 - j3.4)\Omega$ and the load impedance is $(50+j0)\Omega$. L-section is used for the impedance matching.

As $R_L > R_G$, $Q = \sqrt{\dfrac{R_L}{R_g} - 1}$.

Using given values of R_G and R_L we get, Q = 2.48.

$X_C = Q \times R_G = 2.48 \times 7 = 17.35\Omega$.
$X_L = R_L / Q = 50 / 2 = 20.16\Omega$.

$L = X_L / 2\pi f = 20.16 / (2 \times 3.14 \times 13.56 \times 10^6) = 237nH$.
$C = 1 / 2\pi f X_C = 1 / (2 \times 3.14 \times 13.56 \times 10^6 \times 17.35) = 677pF$.
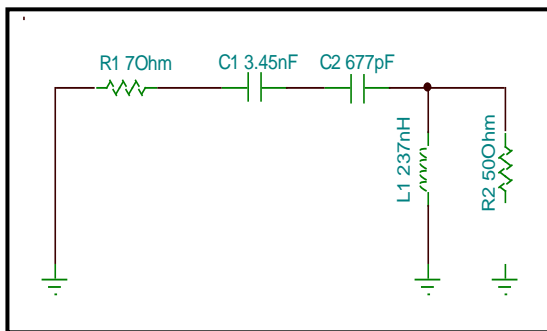

Figure 2: Circuit of output impedance matching of high pass type

B. To design the output matching circuit of low pass type:

As the manufacturer's data, basic circuit configuration and the concept remains unchanged therefore Q = 2.48 w.r.t. the high pass type matching circuit. Now,

$X_L = Q \times R_G = 2.48 \times 7 = 17.35\Omega$.
$X_C = R_L / Q = 50 / 2 = 20.16\Omega$.

$L = X_L / 2\pi f = 17.35 / (2 \times 3.14 \times 13.56 \times 10^6) = 204nH$.
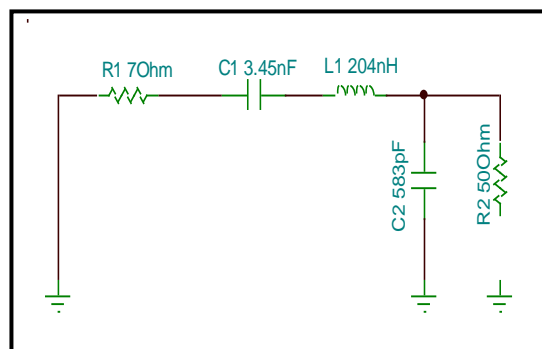$C = 1 / 2\pi f X_C = 1 / (2 \times 3.14 \times 13.56 \times 10^6 \times 20.16) = 583pF$.

Figure 3: Circuit of output impedance matching of low pass type

V.   SIMULATION OF THE INPUT CIRCUIT

In L-section impedance matching i.e. L1=184nH and C2=820pF should provide maximum power transfer at the frequency of operation. The input power P_{in} = 10mW is impedance matched and found transferring the output power P_{out} = 10mW as shown in Figure 4. This is observed that,

At the 50Ω source impedance when V_{peak} = 1V the Power = $V_{peak}^2 / R = (1/\sqrt{2})^2 / 50 = 0.01W$.

At the 4.5Ω MOSFET input when $V_{peak\ to\ peak}$ = 600.82mV, the power = $V_{p-p}^2 / 8R = (600.82 \times 10^{-3})^2 / (8 \times 4.5) = 0.01W$.
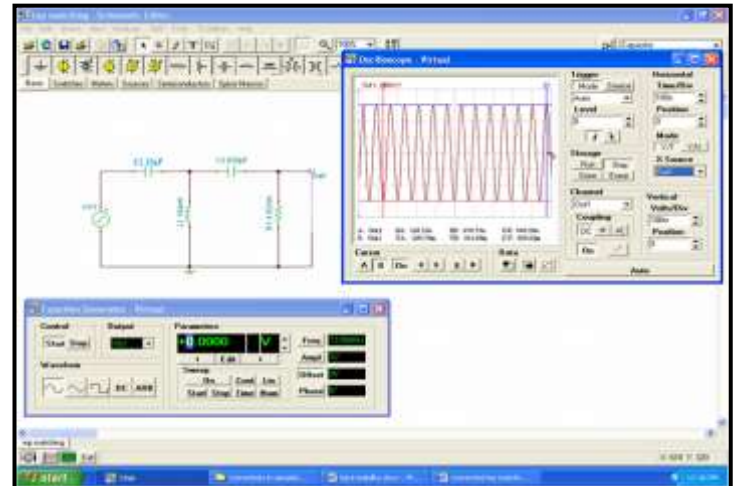

Figure 4: Power transfer of the input side circuit in the TINA-TI software

VI.   SIMULATION OF THE OUTPUT CIRCUIT

For maximum power transfer L1=250nH and C2=640pF are used as L-section. In Figure 5, the input power P_{in} = 10mW and the output power is P_{out} = 10mW. By using the calculated value of the L1 and C2, the maximum power is transferred. This is observed that,

At the 50Ω when V_{peak} = 1V, the Power=$(1/\sqrt{2})^2 / 50 = 0.01W$
At the output impedance of MOSFET 7Ω when $V_{peak\ to\ peak}$ = 708.48mV, the Power = $(708.48 \times 10^{-3})^2 / (8 \times 7) = 0.01W$.
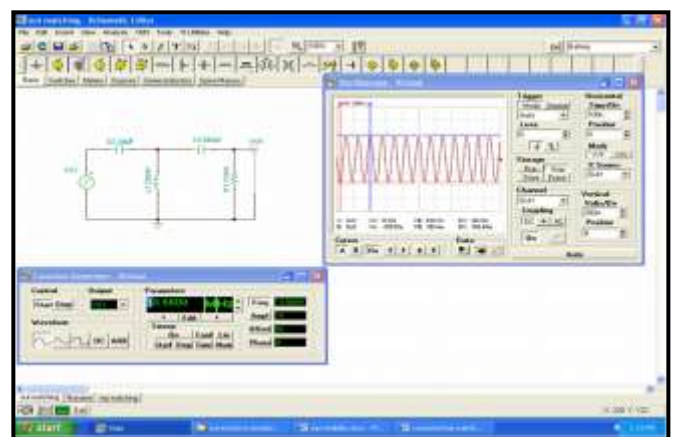

Figure 5: Power transfer in the output side circuit in the TINA-TI software

VII. DESIGN AND SIMULATION OF THE BIASING CIRCUIT

A. Input Biasing Circuit

The input biasing circuit is shown in the Figure 6. The 2.24V and 1.15V voltage variation is required and optimized by using the 10KΩ potentiometer (P1), 10KΩ (R1) and 470Ω (R3). We could get 2.24V and 1.15V at the output when 0% and 100% is set in the potentiometer as shown in the Figure 6 and 7 respectively.
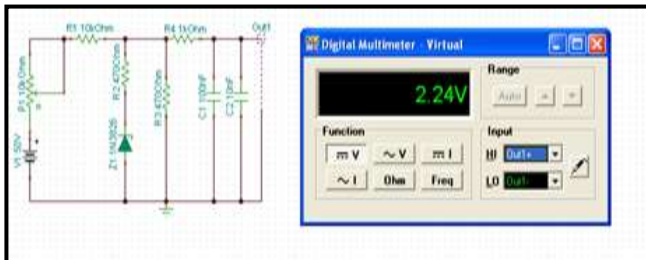

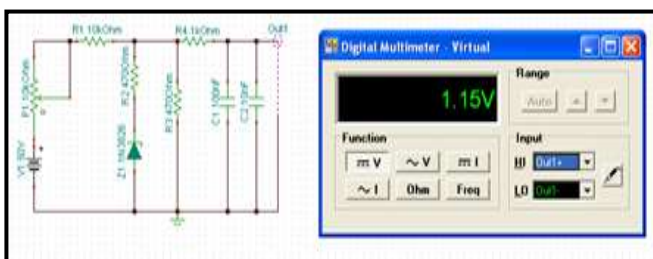Figure 6: Input biasing circuit with 0% setting in the potentiometer

Figure 7: Input biasing circuit with 100% setting in the potentiometer

B. Output biasing circuit

The components C7, C8, C9, C10 and R8 are used in the output biasing circuit. The value of R8 is calculated as following,

The estimated Efficiency $= \frac{P_{out\,(ac)}}{P_{in\,(dc)}} = 50\%$ whereas the P_{out} (ac) $= 100W$ thus P_{in} (dc) $= 200W$.

Now, P_{in} (dc) $= V_{DD} \times I_D$ thus $200 = 50 \times I_D$ therefore $I_D = 4A$.

Now from ohm's law, $R = \frac{V}{I} = (1/4) = 0.25\Omega$.

Figure 8: Schematic of the 100W solid state amplifier

C. Description of the components used in the amplifier circuit

C3, C4, R4, R3, Z1, R2, R5 and P1 are the input biasing components whereas R8, C7, C8, C9 and C10 are the output biasing components as shown in Figure 8. C1 and C6 capacitors are the coupling capacitors which pass the AC components and block the DC components. C3, C4, C7, C8, C9 and C10 capacitors are used for filtering purpose. C2 capacitor and L1 inductor are the input side matching components. C5 capacitor and L4 inductor are the output side matching components. R1 and R6 resistors are used for stability purpose. R4 resistor is current limiter resistor. Z1 Zener diode and R2 resistor are used as the protected components.

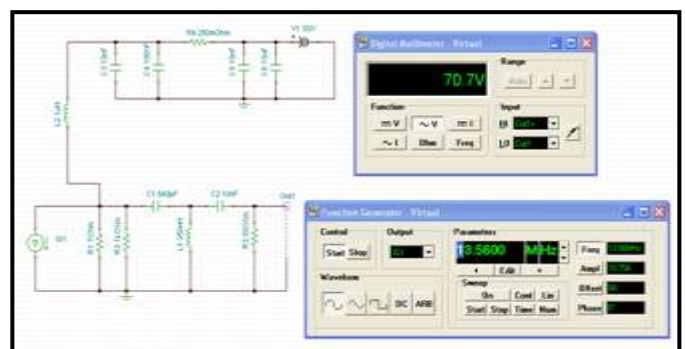## VIII. SIMULATION OF THE POWER AMPLIFIER CIRCUIT

Figure 9: Output matching and output biasing circuits in the TINA TI software

- Here, R = 50Ω and Output power = 100W.
- As P = (V^2/R) therefore 100 = (V^2/50) so V =70.71V.
- I_P = 10.75A and therefore $I_{rms} = I_p/\sqrt{2}$ = 7.60A.
- When $IG_{1(rms)}$ = 7.60A, the output voltage across 50Ω load = 70.7V.
- Trans conductance (ΔI/ΔV) for MRF151 =5mA/V thus, 5 = (7.60/ΔV) and   ΔV = (7.60/5) = 1.52V.
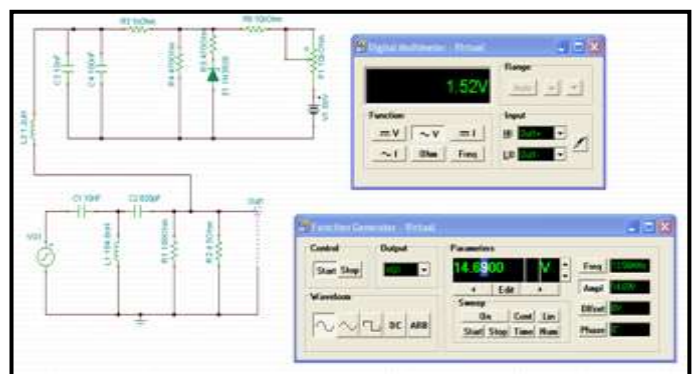

Figure 10: Input matching and input biasing circuits in the TINA TI software

- $VG_{1\,(P)}$ = 14.69V thus, $VG_{1\,(rms)} = (VG_{1\,(P)}/\sqrt{2})$ = (14.69/√2) = 10.4184V.
- $P_{in} = (V_{in}^2/R) = (10.4184)^2/50 = 2.1708W$.
- P_{out} = 100W.
- Gain = 10 × log (P_{out}/P_{in}) = 16.63dB.
- $P_{in\,(dc)} = V_{DD} \times I_D$ = 50 × 4 = 200W.
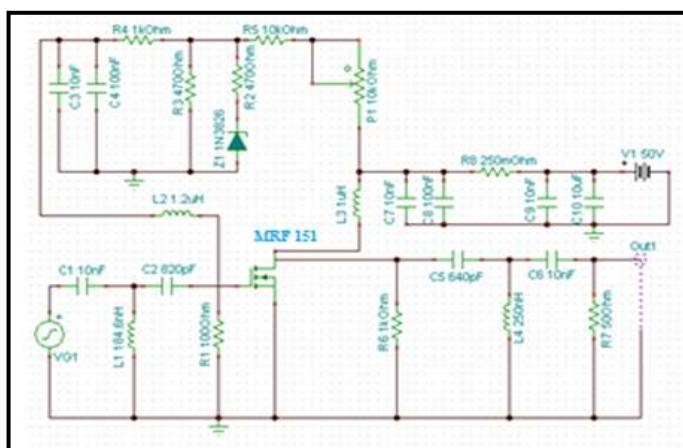- Efficiency = P_{out} (ac) / P_{in}(dc) = 50%.

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IX. FABRICATION AND TESTING OF THE 100W SSPA

The circuit is fabricated with MOSFET MRF151 mounted on a heat sink. The input and output circuits are fabricated on 1mm thick G10 insulation sheets mounted on each side of the MOSFET as shown in Figure 11. A thermal switch in series of the drain supply is mounted on the heat sink to cut off in case of overheating thus protecting the device above 65ºC.

Figure 11: Top view of the 100W SSPA hardware

Signal Generator, Dummy Load, RF Power Amplifier, and DC power supply are used to test the 100W SSPA as shown in Figure 12.
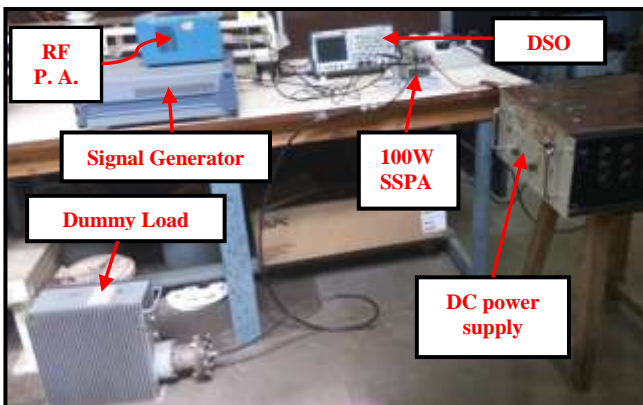

Figure 12: Test set up

TABLE II. TABLE OF THE CIRCUIT PARAMETERS AT PIN OF 0.16W

Frequency in (MHz)	Input voltage Vpp	Output voltage Vpp	I_D (DC) (A)	P_{in} (W)	P_{out} (W)	Gain (dB)
12.5	8	206	3.2	0.16	106.09	28.22
12.7	8	210	3.2	0.16	110.25	28.38
12.9	8	212	3.2	0.16	112.36	28.46
13.1	8	214	3.3	0.16	114.49	28.55
13.3	8	216	3.3	0.16	116.64	28.63
13.5	8	216	3.3	0.16	116.64	28.63
13.7	8	216	3.3	0.16	116.64	28.63
13.9	8	212	3.2	0.16	112.36	28.46
14.1	8	212	3.2	0.16	112.36	28.46
14.3	8	206	3.2	0.16	106.09	28.22
14.5	8	200	3	0.16	100	27.96

From the above given Table II, the P_{out} (ac) = 116.64W and the P_{in} (dc) = 50 × 3.3 = 165W at the 13.56MHz. Therefore,

The efficiency = $\frac{P_{out\ (ac)}}{P_{in\ (dc)}}$ = 70.69% and the power dissipation = 165 − 116.64 = 48.36W at the 13.56MHz.
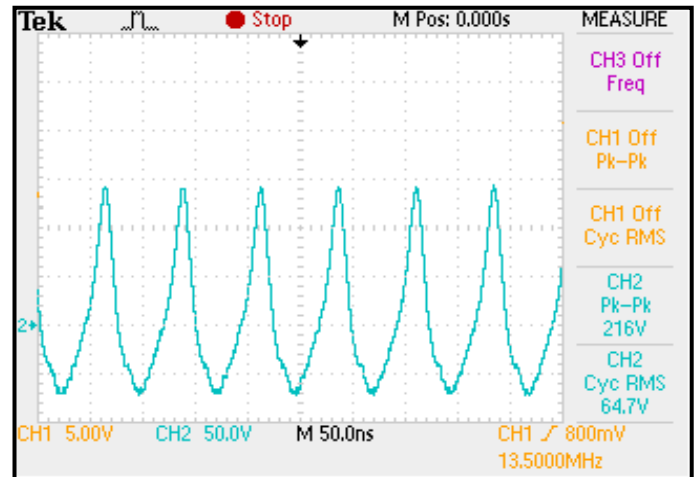

Figure 13: Waveform at 13.5MHz with output V_{pp} = 216V in the DSO

Now, the low pass output circuit is fabricated and used instead of the high pass type in the output matching circuit as shown in the Figure 14.

Figure 14: Circuit fabricated with low pass type of the output matching circuit

The second type of 100W SSPA is tested and results are shown in Table III on the next page. Results of the two different types of circuit with high and low pass output matching circuit are compared.

From the Table III, the P_{out} (ac) = 100W and the P_{in} (dc) = 50 × 3.4 = 170W at the 13.56MHz. Therefore,

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The efficiency $= \frac{P_{out\,(ac)}}{P_{in\,(dc)}} = 58.82\%$ and the power dissipation = $170 - 100 = 70W$ at the 13.56MHz.

Frequency in (MHz)	Input voltage Vpp	Output voltage Vpp	I_D (DC) (A)	P_{in} (W)	P_{out} (W)	Gain (dB)
12.5	8.32	192	3.3	0.17	92.16	27.34
12.7	8.32	194	3.3	0.17	94.09	27.43
12.9	8.32	196	3.4	0.17	96.04	27.52
13.1	8.32	198	3.4	0.17	98.01	27.61
13.3	8.32	198	3.4	0.17	98.01	27.61
13.5	8.32	200	3.4	0.17	100	27.7
13.7	8.32	200	3.4	0.17	100	27.7
13.9	8.32	198	3.3	0.17	98.01	27.61
14.1	8.32	196	3.3	0.17	96.04	27.52
14.3	8.32	194	3.3	0.17	94.09	27.43
14.5	8.32	192	3.2	0.17	92.16	27.34

The wave shape of the output signal and the bandwidth flatness is improved in the low pass type of the output matching circuit in comparison with the high pass type of the output matching circuit. The Efficiency is decreased in the low pass type of the output matching circuit compare to the high pass type of the output matching circuit.

Figure 15: Waveform at 13.5MHz with output V_{pp} = 200V in the DSO

CONCLUSION

This is concluded that selection of proper MOSFET with stability parameters of K = 3.1 is done based on the required specification. The impedance matching circuit and the biasing circuit were designed for optimum performance. The simulation results are found in agreement with the desired specification. All the components are fabricated on the G10 and the complete circuit was tested in the required frequency bandwidth of 13.56±1MHz. After proper optimization of the matching circuit the desired output (100W) was obtained at

13.56MHz. The response was within 0.36dB over the specified bandwidth.

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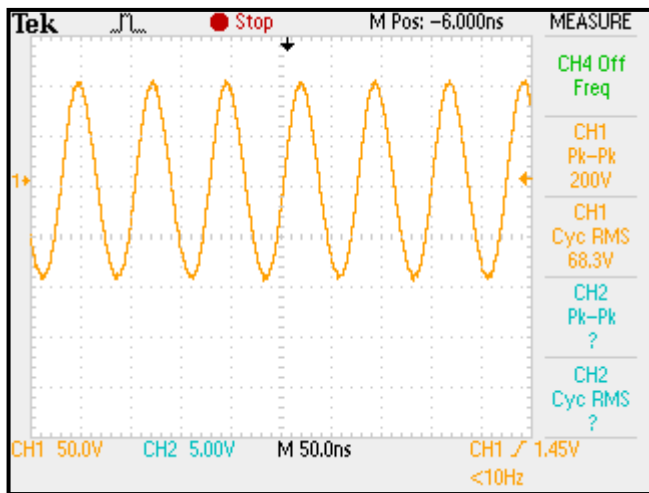[9] Jeremy Everard, "Fundamentals of RF Circuit Design", John Wiley & Sons, Ltd., 2001.

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