Review Paper on Frequency Multiplier at Terahertz Range

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Abstract: Frequency multiplier is an electronic circuit which generates the output frequency which is an integer multiple of the applied frequency. For this purpose, nonlinear devices such as BJT, FET, schottky diode, varactor diode, step recovery diode are used. The nonlinear region of their characteristics is utilized to design frequency multiplier. In terahertz range stability and broad bandwidth are required factors to design heterodyne receiver. For this purpose, only schottky diode is the best option because its cutoff frequency is so high and due to this reason switching frequency of this diode is high compared to its other comparable. The design of frequency multiplier consists of three parts namely the diode structure, input and output matching circuit. The detailed discussion about sources available at terahertz frequency range, different design methods of frequency multiplier with active and passive devices, comparison of available passive frequency multiplier are presented in this paper.

Keywords: *frequency multiplier, doubler, tripler, schottky diode, antiparallel diode pair, LO, HEMT, HBV*

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1. Introduction

Several recent articles have described the potential capability of terahertz technology and how developing this technology can lead to exciting scientific research for applications in variety of fields. One of most challenging aspects of Terahertz technology is the lack of compact, reliable efficient local oscillator (LO) sources in the terahertz range.

Sources available at Terahertz range and their limitations are given below:

FIR laser pumped by the gas laser: The power generation method for this type requires several tens of watts of DC power. It is bulky and works at discrete frequencies [1].
Limitation: It is used only at ground based applications where size and power are not an issue [1].
QCLs (quantum Cascade Lasers): They are ultra-compact milliwatt-level terahertz solid state sources. CW mode frequency is lower than 1.2 THz [1].
Limitations: It has tuning problem. It requires cryogenic cooling to approximately 4^0K for maximum output power [1].

These two sources known as photonic sources are used to generate LO in cryogenic heterodyne receiver. But the main problem is that their output power is in 1-2 THz range which is lower than the power produced by room temperature frequency multiplier [1]

Application of high frequency sources*:*

High *speed wireless communication*: It is used for high speed wireless data communication. This requires open free space path to high speed wireless communication system transferring data at rates of several tens of Gigabytes per seconds [1]

Imaging system: It's able to see through clothing to detect contraband or weapons.
Imaging RADAR: For this type of systems the signal to noise ratio and the standoff distance can be improved with higher power sources because spatial resolution is directly proportional to the frequency for a given aperture size.
Astrophysics: Heterodyne spectrometer is needed to measure Doppler velocities in the interstellar medium and star forming regions with resolution around 1 km/s.

Frequencies ranging from below 100 GHz to at least 5 THz are needed to identify the spectral signature of a wide range of molecules, isotopomers, atoms and ions as well as temperature, density pressure, mass and dynamics of the system observed

This article will describe the technologies developed to build frequency multiplier for solid state LO above 100 GHz for a space borne radio telescope. This will address some of the most important questions in cosmology and galaxy evolution.

High frequency signals can be generated either using high frequency oscillator or cascading a low frequency source with frequency multipliers. It is difficult to build and realize a high frequency oscillator due to degraded performance such as stability, accuracy and phase noise. To overcome these problems low frequency low phase noise VCO in conjunction with the frequency multiplier is the most preferred and the proposed method [4][6] for our research work.

2. Frequency Multiplier

Frequency multiplier is an electronics circuit that generates an output signal whose output frequency is a harmonic (multiple) of its input frequency. Frequency multiplier consists of a

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nonlinear circuit that distorts the input signal and consequently generates harmonics of the input signal. At output side bandpass filter is used to select the desired harmonic frequency and remove the unwanted fundamental and other harmonics from the output [2]

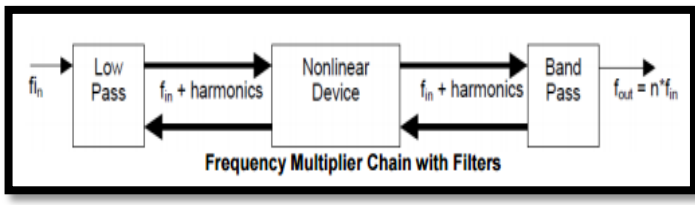

Figure 2.1: frequency multiplier basic block diagram [2]

Many types of the frequency multipliers such as doubler and Tripler, quadrupler have been reported. They can be implemented using passive or active circuits.

***There are 2 Types of Frequency Multipliers for design based on the solid state devices*:**
Active Multiplier and Passive Multiplier

The active multipliers using transistors have the advantage of providing conversion gain, but the broadband bandwidth is difficult to achieve due to the stability and power consumption problem. On the other hand, passive multipliers using diodes as a nonlinear deice which provides broader bandwidth and good stability in millimeter wave range.

Inp-based high electron mobility transistors (HEMTs) have demonstrated excellent millimeter-wave characteristics, such as low noise figure, and high gain. However, the main drawback of the Inp-substrate is the high cost and limited wafer size availabilities [8]

Traditionally, the schottky diode has been the device of choice for the multiplying element and it is still the most common multiplying element available at millimeter wavelength. Recently heterostructure barrier varactors (HBV) or on metamorphic high electron mobility transistors (HEMT) have been developed rapidly. HBVs reach very high efficiencies and output levels but are inherently narrowband devices [4]. HEMT based active multiplier provides very good conversion efficiencies and can be implemented on the same chip with amplifier elements. A disadvantage with active devises is that they cannot usually handle large input power and are not as stable as passive multipliers [8].

Active Multiplier

An active frequency multiplier generates harmonics by rectifying the sinusoidal input signal. The principal of operation is that the active devices such as a FET or BJT are biased near its pinch-off point of DC load line. The input sinusoidal turns the device on over part of its cycle. The fraction of the time that it is on, compared to the entire period called is its duty cycle. By adjusting the duty cycle we can maximize the desired output harmonics generated. The higher the harmonic, the shorter the duty cycle must be. For a doubler, the optimum is around 30%, and for a tripler is about 20%. [3]

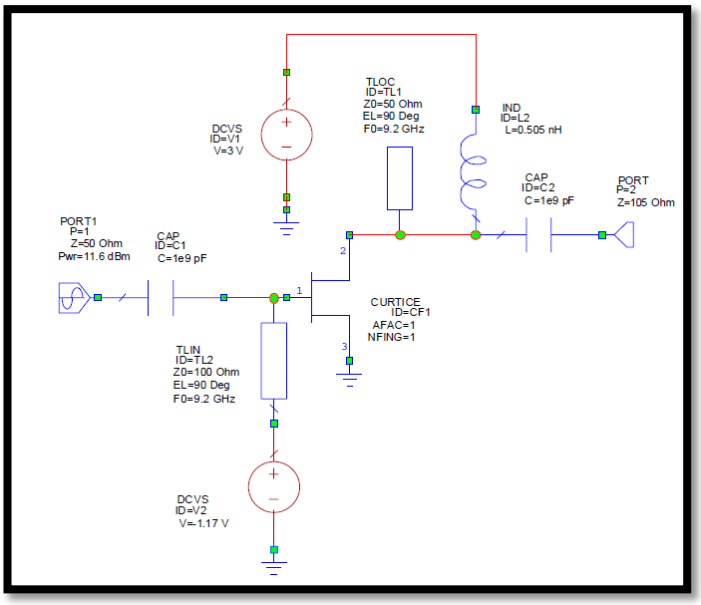

Figure 2.2: ideal circuit of active frequency multiplier [3]

As shown in figure, gate is driven by an RF source. Gate bias voltage is somewhat below (more negative) than pinch-off. So FET conducts only for the period when the gate voltage is above the voltagev_p. This whole period is known as duty cycle. Duty cycle of the drain current pulses can be adjusted by changing the DC gate biasv_{gg}. A shorter duty-cycle is necessary for higher harmonics because as per the generation of harmonics, number of harmonics is directly proportional to the distortion in applied sinusoidal signal. So, for more harmonics in active multiplier it requires more negative gate voltage v_{gg} and great RF input required. As we continue to decrease the duty cycle in this manner, eventually the negative peaks of the gate voltage reach the gate breakdown voltage [3]

The most important characteristic of active multiplier is the possibility of obtaining conversion gain instead of loss. HEMT's have relatively low values of I_{max} and I_{max} is proportional to gate width. Output power depends largely on the size of the device. There is a tradeoff between power against gain. To achieve gain at higher output frequency, C_{gs} must be reduced and this requires a narrow device. A narrow device results in lower output power. [2]

FET and BJT frequency multipliers can be made very broadband, but again there is a price, increasing the bandwidth reduces conversion gain. As with other FET circuits, the FET's input Q may be very high, and if the multiplier's

bandwidth is more than few percent, the input may be impossible to match over the whole band. [3]

So, the active multipliers are narrowband and it has some stability problem. Active multiplier cannot be higher order multiplier because if the order of multiplication is high then providing the required matching for higher frequency is difficult. To overcome these all problems, we go with the passive multiplier.

Passive Multiplier

There are number of efficient ways to generate harmonics with passive devices. The dominant devices are schottky-barrier diode, varactor diode and step-recovery diode. According to diode their resistive or capacitive nonlinearity are used to generate harmonics of input sinusoidal signal.

Resistive frequency multiplier: Resistive frequency multipliers use the nonlinear I/V characteristic of a schottky barrier diode to distort a sinusoidal waveform. This distortion generates the harmonics. The optimum efficiency of a resistive frequency multiplier can be no greater than $1/n^2$, where n is the harmonic number [3]. Resistive multiplier has broader bandwidth because schottky diode is used as a resistive device and it has inherently very broadband.

Varactor multiplier: The nonlinearity of capacitance C/V is used to distort the sinusoidal signal. But one problem is that designing a varactor multiplier is the diode's weak reactive nonlinearity. Without some tricks, the multiplier does not generate harmonics beyond the second. A varactor is capable of higher efficiency and power than a resistive multiplier. If the current in the diode is sinusoidal, the charge function will vary in the same way, and the junction voltage will be roughly proportional to the square of the charge. This means that the varactor multiplier will generates only second harmonics efficiently. For higher harmonics, an idler, a short circuit resonator tuned to the second harmonic in parallel with the diode is used. This idler allows a second harmonic current to circulate through the diode and to mix with the fundamental, producing a third harmonic. [2]

Step-recovery diode multiplier: A SRD frequency multiplier is a reactive device, but it operates somewhat differently from a conventional varactor multiplier. SRDs are generating high harmonics from a relatively low frequency excitation. SRDs can generate large pulses a few tens of picoseconds large. Because SRD multipliers invariably are high order, conversion loss can be high. In SRD does not require any type of idler to generate higher order harmonics. SRDs use the diode's diffusion capacitance for charge storage nonlinearity to generate harmonics. [2]

From above all multipliers, SRD multiplier and varactors are prone to instability. They also are sensitive to circuit parameters, and requires a high tolerance for frustration. For terahertz application only schottky diode multiplier are used because the switching speed of schottky diode is higher than all other devices. In schottky diode, only majority carriers are participating in any conduction process so, depletion region created at the junction is very narrow. Voltage required to remove this stored charge in the depletion region is very small. So cut-in voltage of schottky diode is very less and switching speed of that diode is high which meets the requirement to design multiplier at terahertz frequency range.

3. Schottky diode frequency multiplier

For millimeter and submillimeter wave frequency multipliers, schottky planar varactors are still providing the best performance in terms of efficiency, output power, and instantaneous bandwidth [5]. Planar schottky diodes were introduced over a decade ago [9], [10] and now have been successfully demonstrated well into the terahertz range, replacing whisker-contacted schottky diode [2]

Schottky based multipliers can be divided into reactive (varactors diodes) and resistive (varistor diodes) multipliers. Mixed mode of operation is also possible. Varactors multipliers have larger efficiencies and produce more output power than multipliers based on resistive schottky diodes. Resistive multipliers on the other hand have smaller capacitance variation and thus can be designed to cover wider bandwidths than varactors multipliers [7].

Passive multiplier has more advantages over on active multiplier. Passive multiplier using schottky diode handle large input power and it is stable for high frequency. To design a MMIC frequency multiplier for a frequency higher than 100 GHz BES process by United Monolithic Semiconductors (UMS) is use. The main component of BES process is schottky diode because schottky diode's switching frequency is higher than all other diodes.

Diode is nonlinear device so it used to design frequency multiplier and its current equation is given by

$$I_D = I_s[\exp\left(\frac{q\,V_j}{\eta kT}\right) - 1] \qquad (1)$$

Where $\frac{k\,T}{q} = 25.8$ mV for T= 293 K (absolute temperature)

V_j = junction voltage

k = Boltzmann's constant

I_s = saturation current

η= ideality factor

In paper [11] the authors have discussed three types of structures to design a multiplier using schottky diode. First one is common balanced tripler whose block diagram is shown in figure 3.1. As shown in this figure on chip capacitor is required for applying DC bias to the schottky diode. Constrained by the technological level, the on chip capacitor cannot be achieved.

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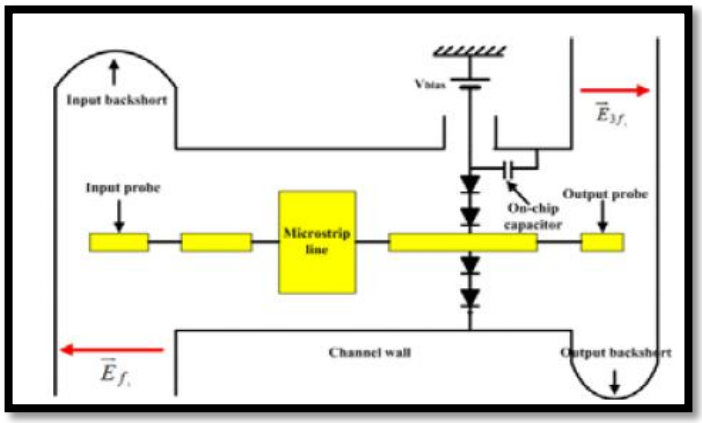

Figure 3.1: block diagram of common balanced tripler [11]

To overcome on chip capacitor problem, a tripler is implemented without bias circuit [12] which is shown in below figure 3.2. Here diodes are connected in anti-parallel form. So the even harmonics of the input signal are trapped in a virtual short circuit formed by the diodes and suppressed. And at output side only odd harmonics of the applied signal is available. The disadvantages of this scheme are that the efficiency is relatively low, and heat accumulation happens in the schottky junction when high input power is added due to the poor thermal conductivity of quartz glass [11].

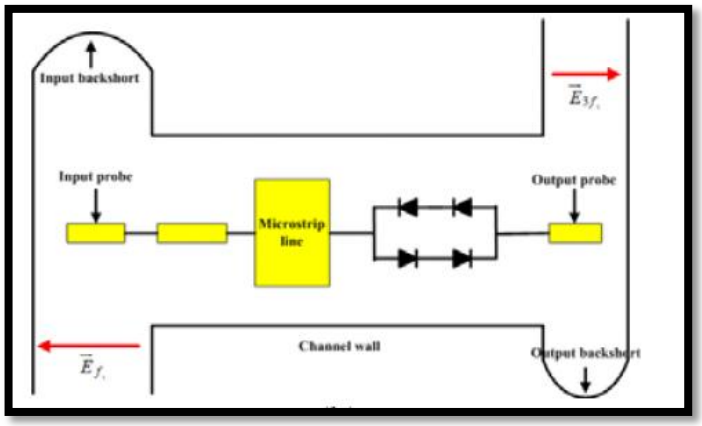

Figure 3.2: block diagram of tripler without bias circuit [11]

To overcome these problems, an unbalanced scheme discussed in [12] with a pair of schottky diode is in parallel is adopted is shown in figure. Because of this type of structure, even harmonics are not suppressed; hence the design process gets more difficult.

Design methodology: usually, the first step in the design of frequency multiplier is to determine the characteristics of the diodes along with the operating conditions that best suits the application. Such as a doping level, diode dimensions, and the bias voltage for a given input power once these parameters are fixed and the optimum embedding impedances of the diodes are determined, a linear circuit can be synthesized [5].

For schottky varactor diode's cutoff frequency should be much higher than the operating frequency [11].

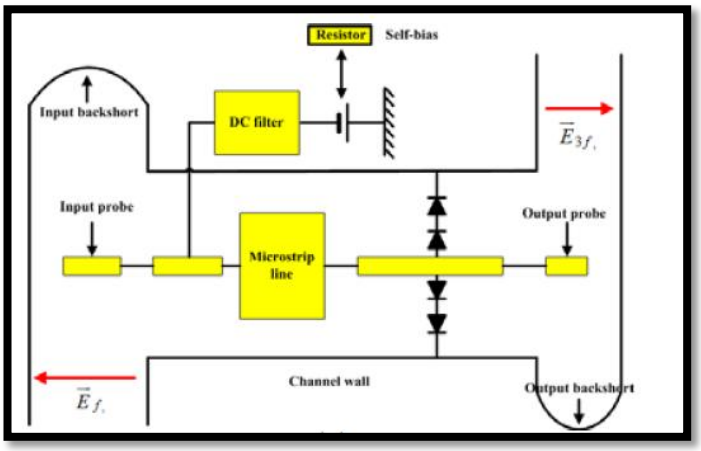

Figure 3.3: block diagram of unbalanced tripler with bias circuit [11]

The input circuit as well as the output circuit, consists of the Microstrip-waveguide transition and matching circuit [5].The input and output circuits must fulfill demanding criteria. First, the circuits must obviously let the wanted signal to pass and second, to provide a reasonably large reactive load at other frequencies. In addition, the circuit elements should be as small as possible to minimize the chip size and transmission line losses

The tripler consists of input output matching circuits, separates bias routes for both diodes and of a diode pair. In order to suppress the coupled slotline mode and to obtain a symmetric coplanar mode, the circuit was designed to be as symmetric as possible [8].

The input and output circuits must fulfill a demanding criteria. First, the circuits must obviously let the wanted signal to pass and second, to provide a reasonably large reactive load at other frequencies. In addition, the circuit elements should be as small as possible to minimize the chip size and transmission line losses. [11] The input circuit, as well as the output circuit, consists of the waveguide-Microstrip transition and matching circuit. The input circuit consist a low pass filter whose cutoff frequency ω_0 and DC block capacitor. At output side, the short circuit idlers are used for all unwanted harmonics which behave as short circuit for unwanted harmonics and open circuit for wanted harmonic

For schematic simulation process the tripler is divided into two parts: a linear network, which is analyzed using Ansys High Frequency Structure Simulator (HFSS) in consideration of the parasitic effects, and nonlinear behavior of the schottky varactor diode, solved by Agilent Advanced Design Simulator (ADS). [11]

Paper	Input frequency (GHz)	Output frequency (GHz)	Input power (dBm)	Output power (dBm)	Conversion loss (dB)	Efficiency (%)
[7]	25-23	75-140	17	-2.4	19.5	1.12
[4]	25-37	75-110	16	-3.7 to 2	14 to 19.7	1.5
[11]	75	225	23.8	-12.3	11.4	7.3
[6]	20-35	60-110	12	-3	15	-

Table 3.1: summary of the performance of previously designed tripler and this work

Conclusion: Available frequency sources and their limitations are discussed in this paper. Frequency multiplier is used to multiply low frequency LO source by any integer multiple and convert it into the high frequency. Using frequency multiplier all problems occurring in direct high LO source is removed. As per requirement of terahertz band only passive multiplier is used because stability and frequency bandwidth of passive multiplier is better than the active multiplier. In multiplier design we use diode structure to generate harmonics and to select desired one bandpass filter used at the output side. This diode multiplier demonstrates a broadband LO source with compact chip size

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