A Review: Implementation of Reed Solomon Error Correction & Detection for Wireless Network 802.16

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Abstract- *The reed Solomon (255,239) are error-correcting & detecting code.* Reed-Solomon codes are the most frequently used digital error control. It is also called as forword error code. The main part of reed-Solomon encoder is the linear feedback shift register that is implemented using VHDL A pipelined RS decoders is proposed of reducing the hardware complexity use the pipelined GFmultiplier in the syndrome computation block, KES block, Forney block, Chien search block and error correction block for provides low complexity the extended inversion less Massey-Berlekamp algorithm is used. The extended inversion less Massey-Berlekamp algorithm overcomes both the error locator polynomial and the error evaluator polynomial at the same time.

Keywords— *Reed-Solomon codes; code generator polynomials; syndrome; Berlekamp Massey; Chien; IEEE 802.16; VHDL;FPGA*

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I. INTRODUCTION

Digital communication system is used to transport an information bearing signal from the source to a user destination via a communication channel. A code is the set of all the encoded words, the code word that an encoder can produce. When actual set of data encoded it becomes a code.

This paper introduced error codes. If source transmits n bits, then the n-m bits will be redundant or parity bits. These redundant bits allow one to recover the original message in the case when noise corrupts the data during transmission and causes some bits of the code in the error. These codes are more efficient codes than other multi-error detection and correction codes [4].

II. LITERATURE SURVEY This chapter represents an overview of background research to the project. The literature also gives the brief idea about the technical, operational and economical feasibility study.

a. Kenny Chung ChungWai, Dr. Shanchieh Jay Yang" Authors introduced a FPGA implementation of Reed Solomon. It is synthesized to Altera's Stratix II and benchmarks are run against Altera's Reed Solomon code. Author was designed Xelic's encoder which is measured to be about half the size of Altera's encoder.[1]

b. Joaquin Garcia, Rene Cumplido

Author introduced OFDM using System generator and Matlab&Simulink.The results on hand show that it is possible to implement an OFDM modulator for IEEE Std.802.16 using Virtex II. In this paper the author implement configurable system that can be implemented for different modulation technique. The future work of this paper is Implementation of the FEC modulator, demodulator.

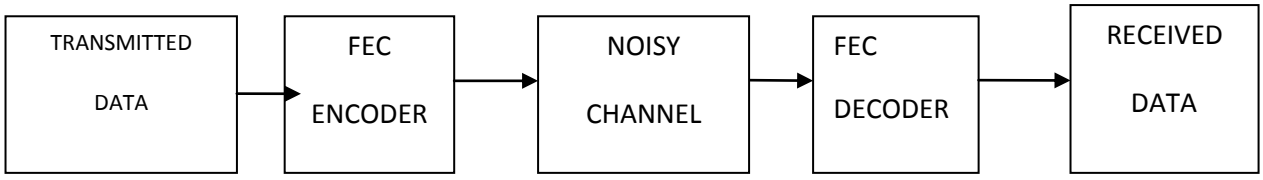


Figure1.1 forword error correction concept

c. K. Harikrishna, T. Rama Rao,
Authors K. Harikrishna, T. Rama Rao, and Vladimir A. Labay, introduced a high level implementation of a high performance FFT for OFDM modulator and demodulator of 802.16d. The design has been coded in Verilog and besieged into Xilinx Spartan3 field programmable gate arrays. The design of the FFT is implemented and applied to fix WiMAX—IEEE 802.16d communication standard.

d. MiljkoBobrek, Kenyon H. Clark,
Authors introduced FPGA implementation of the Reed-Solomon decoder for used in IEEE 802.16 WiMAX systems.The decoder is based on RS (255,239) code. It is additionally shortened and punctured according to the

WiMAX specifications. A Simulink model was used for simulation and hardware implementation. It is based on the System Generator library of low-level Xilinx blocks

e. M.A. Mohamed, A.S. Samarah

Author introduced the design and implementation of OFDM system. Author has tested system performance by considering various design parameters using MAT-LAB 2011. All modules are coded using VHDL pro-gramming language.

f. Yuval Cassuto, JehoshuaBruck

Authors introduced the number of monomials required to interrupt a received word in an algebraic list decoder for Reed–Solomon codes depends on the instantaneous channel error. On the basis of logical side, this paper studies the dependence of interpolation costs on instan-taneous errors, in both hard- and soft-decision

g. Li Chen et.al.

Author introduced algebraic soft-decision decoding (ASD) algorithm. They are a polynomial-time soft de-coding algorithm for Reed- Solomon (RS) codes. It breaks both the 11 algebraic hard decision decoding (AHD) and the conventional unique decoding algo-rithms; this paper proposes a progressive ASD (PASD) algorithm that enables the conventional ASD algorithm to perform decoding with an adjustable designed fac-torization output list size (OLS).

h. F. Abdelkefi, J. Ayadi

Authors introduced a novel efficient algorithm for the opinion of sparse channel impulse response (CIR) is addressed for OFDM systems. The innovation of this algorithm comes from the fact that it equivalently see the CIR estimation problem as a decoding one. To do so, it uses first the channel sparsely through the model-ing of the sparse CIR as a Bernoulli-Gaussian process. Then, using the relationship between the Reed-Solomon codes and the OFDM modulator it efficiently estimates the sparse CIR using directly the decoding of the OFDM received signal. The obtain simulation results highlight that using the planned algorithm gives good estimation performance in terms of mean squares error on the sparse CIR estimates. Which concludes that us-ing a multicarrier OFDM transmission system, pilot tones can be seen as virtual RS code words.

Li Liet. al.

Author Li Li, introduced Reed-Solomon (RS) codes. These codes are widely used as forward correction codes (FEC) in digital communication and storage sys-tems. Correcting errors of RS codes have been exten-sively calculated in both academia and industry. How-ever, for burst-error correction, the research is still lim-ited due to its ultra-high computation complexity. Then, based on the planned algorithm, a unified VLSI archi-tecture that is capable of correcting burst errors, as well as random errors and erasures, is firstly presented for multimode decoding requirements.

j. Xinmiao Zhang, Yu Zheng

Authors introduced a model to reduce the complexity of algebraic soft-decision decoding (ASD) of Reed–Solomon (RS) codes; re-encoding and 12 coordinate transformation can be applied. For an (n, k) code, the re-encoding was implemented as applying erasure de-coding to the k most reliable code positions previously .Such re-encoding can occupy a significant part of the overall decoder are. As a result, the proposed decoder can achieve much higher efficiency than prior designs. Our future work will exploit if systematic re-encoding can be employed in general ASD decoders.

k. J.-I. Park, H. Lee

Authors,introduced a new area-efficient truncated in-version less Berlekamp-Massey architecture for the Reed-Solomon (RS) decoder, where RS decoder is one of the forward error correction techniques. The area-efficient feature of the proposed architecture is obtained by truncating redundant processing elements in the key equation solver (KES) block using the BM algorithm. This enhances the hardware utilization of the processing elements used to solve the key equation and reduces the hardware complication of the KES block.

l. Christian scholar,

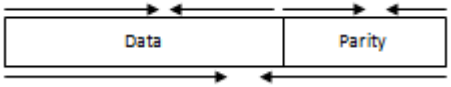
Author introduced VHDL code generator for Reed-Solomon decoders using Euclid's algorithm. The VHDL code is synthesizable, and area and speed met-rics for several decoder designs is presented, targeted to Xilinx Field Programmable Gate Arrays. The core gen-erator also generates the vectors for the test bench. The code generator is capable of generating VHDL code for most binary FEC decoder, such as Hamming, Cyclical Redundancy Check (CRC), and BCH codes. In the de-sign of the Reed-Solomon decoder, a bank of Galois multipliers is used, as opposed to a dedicated multiplier where it is needed.This result is less area, but requires tristate buses and reliable scheduling of the steps to avoid collisions.

m. Jong Kang Park

Author introduced a program that generates synthesiz-able VHDL code for Reed-Solomon decoder is pre-sented. Erasure decoding is supported. The method of solving the key equation is the inversion less Massey-Berlekamp algorithm, or a modified version called the reformulated inversion less Massey-Berlekamp algo-rithm. The choice of the algorithm is user controlled. The area and speed metrics are provided for several de-signs. The average throughput achieved is 500Mbits/second in ASIC.This is comparable to the re-sults achieved by the code generator of the thesis when applied to Xilinx FPGAs.

2.2 Reed-Solomon Theory

2.3 A Reed-Solomon code is a block code and can be specified as RS (n,k) as shown in Figure 2.1. The variable 'n' is the size of the codeword with the unit of symbols 'k' is the number of data symbols and 2t is the number of parity symbols. Each symbol contains 'm' number of bits.



RS codes are generally represented as an RS (n, k), with m-bit symbols, where

Block Length : n

No. of Original Message symbols: k Number of Parity Digits: n - k = 2t Minimum Distance: d = 2t + 1.

The relationship between the symbol size, m, and the size of the codeword n, is given by

$n=2^m$.

1.1 Error Detection & Correction Schemes

Error detection and correction or error controls are techniques that enable reliable delivery of digital data over unreliable communication channel [3]. Many communication channels are subject to channel noise, and thus errors may be introduced during transmission from the source to a receiver. Error detection techniques allow detecting such errors, while error correction enables reconstruction of the original data. The overall classification of error detection & correction schemes is shown in figure1.2

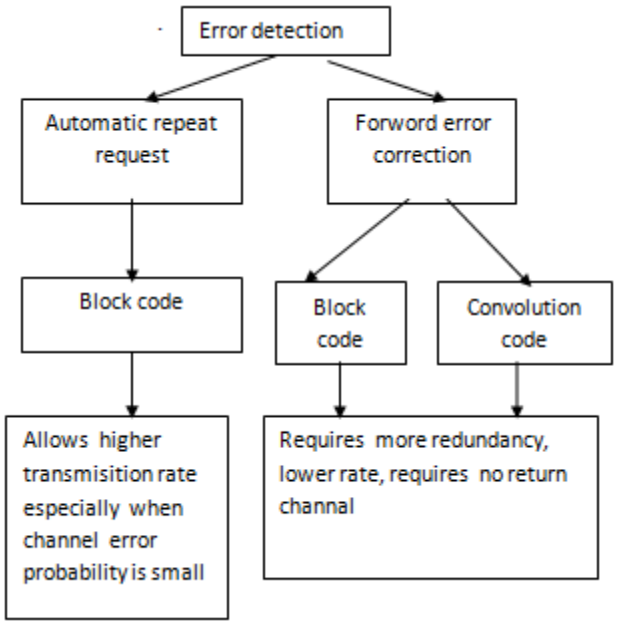


Figure 1.2: Overall classification of error detection & correction schemes [1]

Different errors correcting codes can be used depending on the properties of the system and the application in which the error correcting is to be introduced. Generally error – correcting codes have been classified into block codes and convolutional codes. The distinguishing feature for the classification is the presence or absence of memory in the encoders for the two codes.

PROBLEM STATEMENT

It has been noticed that the present Reed-Solomon Decoder are very large in area and their speed is not too fast. Since Galois field inverters are very complex, several times more so than a Galois field multiplier, a key solver that eliminates the need for such an inverter can yield savings in decoder latency. Such an algorithm is the inversion less massey-berlekamp algorithm by Reed, Shih and Truong [6]. However, the drawback to this algorithm is that it only computes the error – locator polynomial.In the inversion less massey-berlekamp algorithm, the error- evaluator polynomial is computed then by multiplying the error – locator polynomial by the syndrome polynomial. This results in extra latency of the order of the error-locator polynomial, and as a result an extra number of gates and registers are needed.

V. PROPOSED WORK

In this paper, the extended inversion less Massey-Berlekamp algorithm is used. The extended inversion less Massey-Berlekamp algorithm overcomes the extra latency by computing both the error - locator polynomial and the error – evaluator polynomial at the same time. In this thesis, (255,239) reed Solomon codes have been designed. A pipelined RS decoders is proposed with the aim of reducing the hardware complexity and improving the clock frequency in the RS decoders. This design also use the pipelined GF multiplier in the syndrome computation block, KES block, Forney block, Chien search block and error correction block for the enhanced clock frequency and provides low complexity as compared to the conventional ME algorithm architectures.

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