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Layout and Analysis of different Current Mirror using 45nm Technology

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***Abstract*—** This paper proposes new current mirror layout strategies of the circuits which are designed by 45nm technology in Pspice using Tanner Eda tool. Layout strategies help to reduce the matching sensitivity to the linear parameter gradients. The performance of circuit is also analyzed with the help of waveforms generated in W-edit window by varying the input voltage and current values or by changing the arrangement of Mosfet. Simulation results show a significant improvement in matching characteristics of the proposed structures over what is achievable with existing layout techniques in demanding applications.[21]

***Keywords*—** *Current mirror layout strategies, matching performance linear parameter gradients*.

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I. Introduction

Current mirror circuits are widely used, especially within integrated circuit technology. The mirror circuit generally consists of two transistors, although other devices such as FETs can be used, and some configurations do use more than two devices in the overall circuit to obtain better performance. The current mirror circuit gains its name because it copies or mirrors the current flowing in one active device in another, keeping the output current constant regardless of loading. The current being mirrored can be a constant current, or it can be a varying signal dependent upon the requirement and hence the circuit. Conceptually, an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well or it is a current-controlled current source (CCCS). The current mirror is used to provide bias currents and active loads to circuits [22]

II. Different Current mirrors and Their Layouts

1. Simple current mirror: This invention relates to current mirrors and particularly to a low-voltage current mirror realized in bipolar technology. Simple current mirrors, for example the simple current mirror shown in Figure 1 shows is well known in the art. However, such arrangements are often insufficiently accurate, particularly when realized with low gain elements such as two lateral pnp or npn transistors M1(i.e. MNMOS_2) and M2(i.e. MNMOS_1). The ratio of output current I2 to input current I1 of the simple current mirror 2 is given by β, where β is the current gain of the transistors. Thus, for small values of β the accuracy of the simple current mirror is poor.

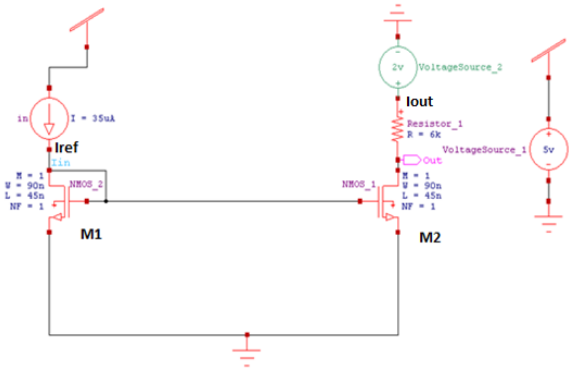

Fig 1: Simple current mirror circuit

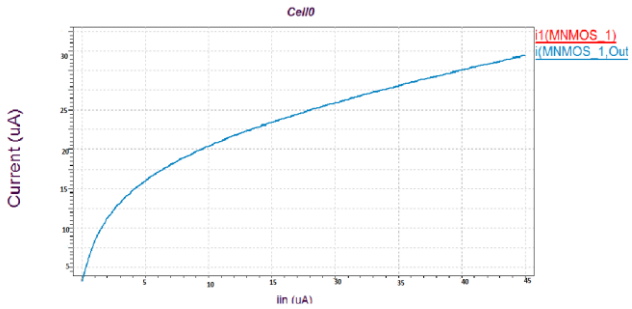

Fig 2: Simulated wave for simple current mirror

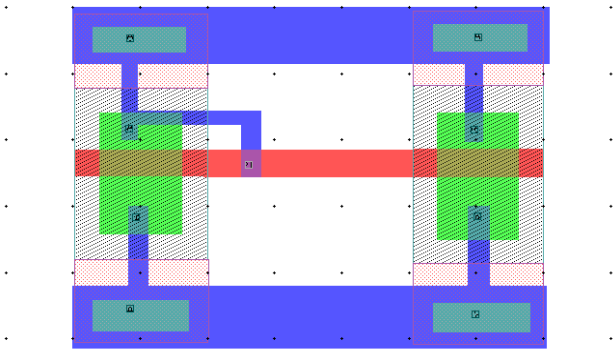

Fig 3: Layout of for simple current mirror designed in L-edit using N-channel MOSFET

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2. Conventional Regulated Cascode current mirror: Current mirrors are frequently used in analog and mixed signal circuit design and because they appear so simple, their importance is sometimes overlooked [1]. The design of an improved regulated cascode current mirror that offers very higher resolution and high speed. This can be accomplished by a feedback loop consisting of an amplifier and M2 (i.e. NMOS_1) as source follower, thereby increasing the output resistance (ideally infinite). The performance of the circuit was analyzed using simulations based on a 45nm technology. This circuit has a limitation that the minimum level of output swing is limited, because drain-source voltage of M1 never touches.

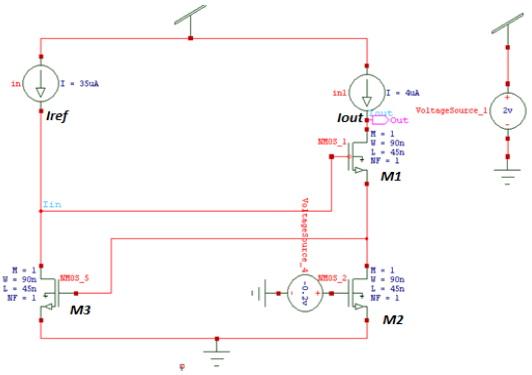

Fig 4: Conventional Regulated Cascode current mirror circuit

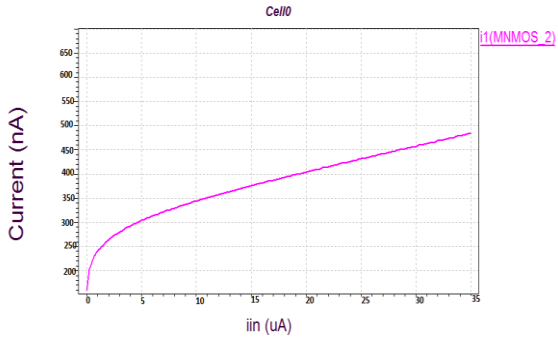

Fig 5: Simulated result for Conventional Regulated Cascode current mirror circuit

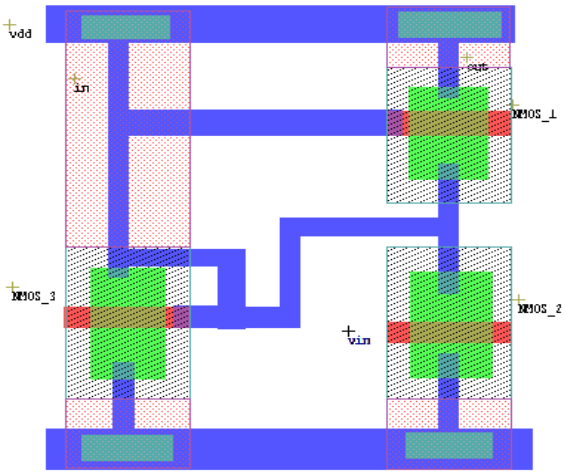

Fig-6 Layout of Conventional Regulated Cascode current mirror circuit designed in L-edit using N-channel MOSFET

3. Cascode current mirror

A cascoded current mirror device is disclosed that is capable of producing an output current that is a direct function of an input current received by that device. The cascoded current mirror includes at least two portions connected together in a cascode manner. Provision is also made for feedback connection between those portions. This feedback connection can, for example, be a buffering connection. Voltage signals are generated by this device that can be used to drive and control additional output stages. Each such additional output stage is capable of producing an additional output current.[2]

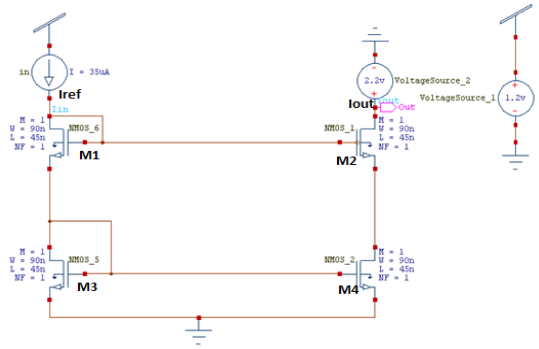

Fig 7: Cascode current mirror circuit

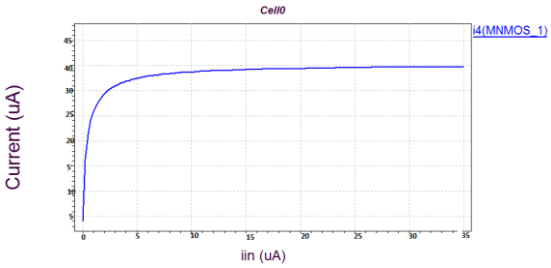

Fig 8: Simulated result for Cascode current mirror

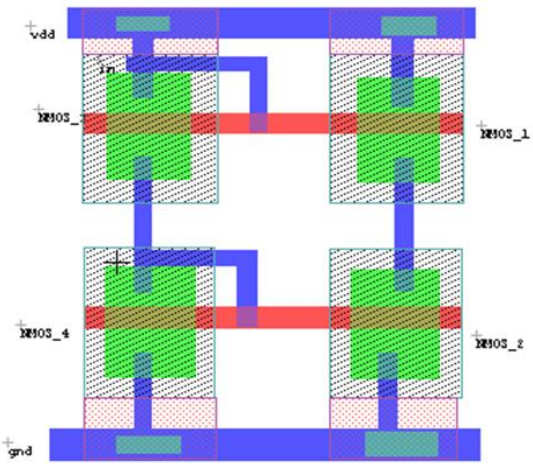

Fig- 9 Layout of Cascode current mirror designed in L-edit using N-channel MOSFET

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4. Triple Cascode Current Mirror

A triple cascoded mirror active load includes three transistors M1, M3 and M5 in a first leg and three transistors M2, M4 and M5 in an output leg connected to an output node IOUT. The first leg receives a current on an input node Iref on the drain of transistor. Transistor M1 has the gate thereof connected to the drain of transistor M3 with the gates of transistors M6 and M4 connected together and to a bias voltage. Transistor M1 is mirrored to transistor M2 by connecting the gates thereof together. Similarly, the gates of transistors M5 and M6 are connected together and also to the node Iref. In this manner, the node Iref receives a low impedance on the input there to, whereas the gate of transistor M2 sees a high impedance thereto and with only two transistors, transistors M3 and M5, disposed in a loop as a rationed cascoded configuration.[3]

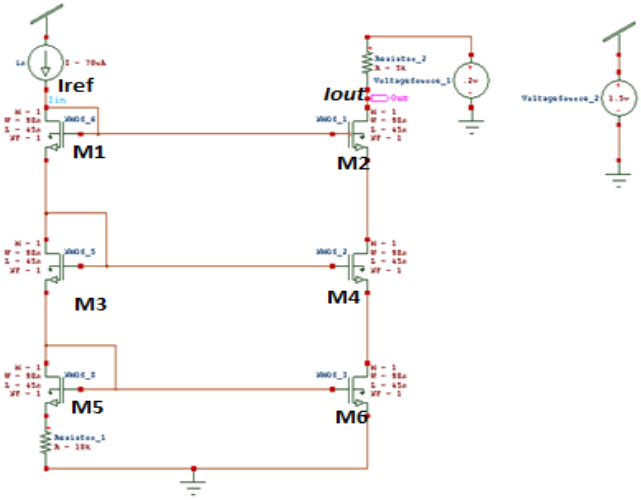

Fig 10: Triple Cascode current mirror circuit

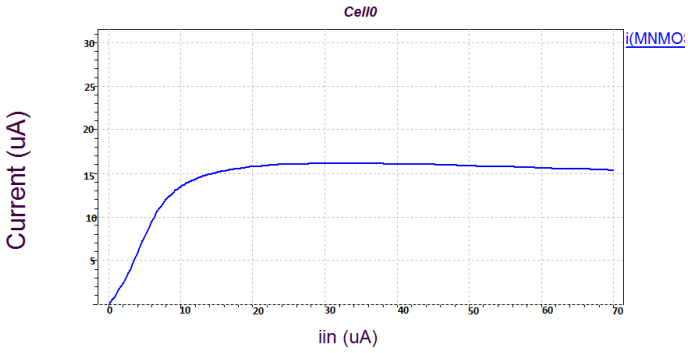

Fig 11: Simulated result for Triple Cascode current mirror

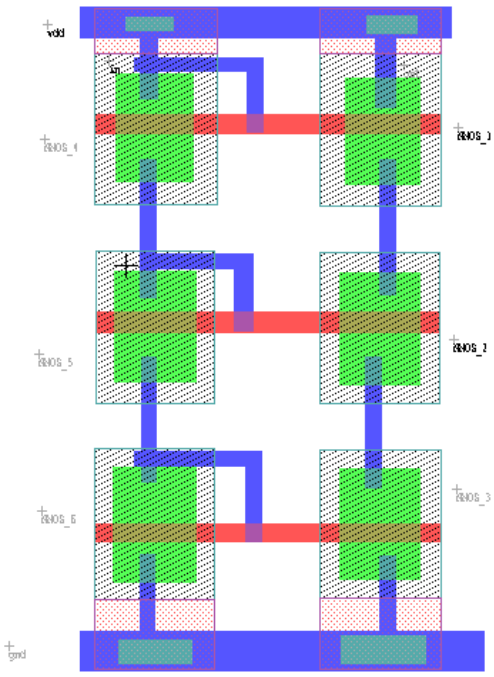

Fig – 12 Layout for Triple Cascode current mirror designed in L-edit using N-channel MOSFET

5. Wilson current mirror: In this current mirror Shunt-series negative feedback technique is used to improve the output impedance and stabilize the output drain current [10]. In contrast to other existing implementations, it does not require a static current flow and can therefore offer considerable static power savings. [4]

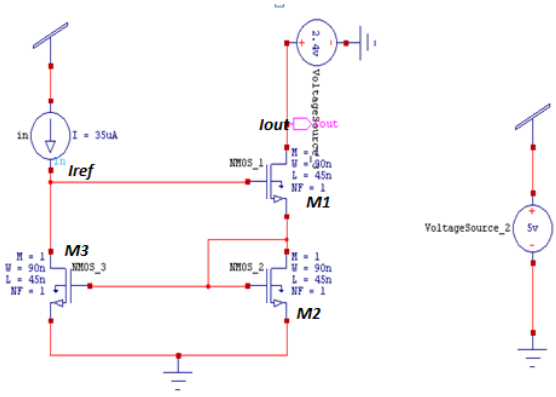

Fig 13: Wilson current mirror circui

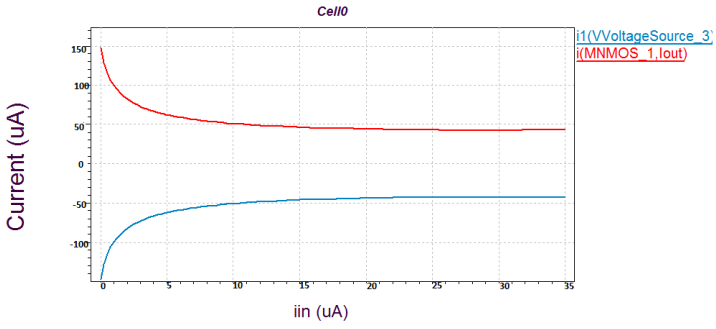

Fig 14: Simulation Results of Wilson Current Mirror

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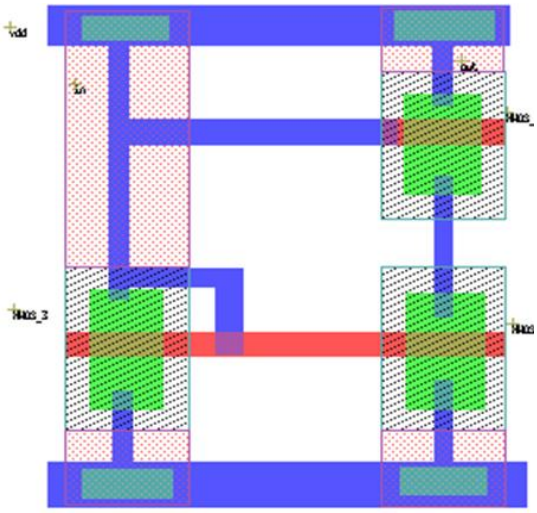

Fig-15 Layout of Wilson Current Mirror designed in L-edit using N-channel MOSFET

6. Low Voltage current mirror: A highly accurate current mirror for IC implementation is comprised of low beta transistors and operates on a low supply voltage by utilizing a bias network with a balance sensing feedback network to control the bias voltage. The output current of one of the mirror transistors is compared with the reference current and the level of the current is then forced to equal the reference by means of the bias voltage adjustment .[23]

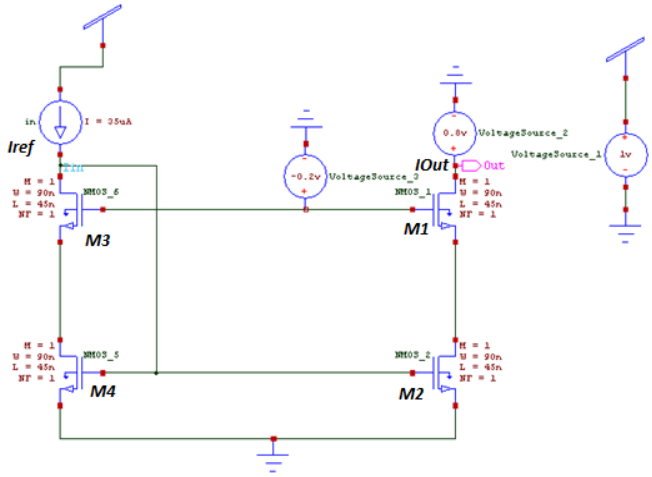

Fig 16: low voltage current mirror circuit

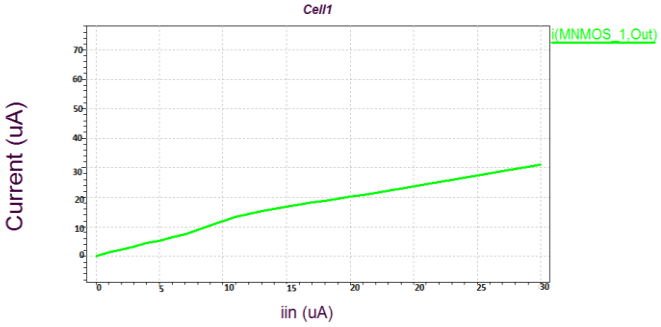

Fig 17: Simulation Results of low voltage Current Mirror

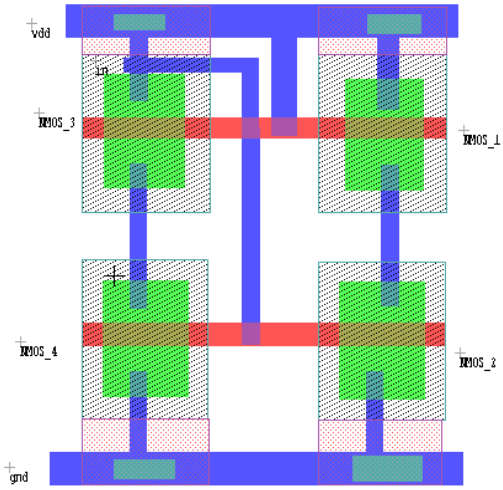

Fig-18 Layout of low voltage Current Mirror designed in L-edit using N-channel MOSFET

III. Conclusion

Simulation of various adder structures have been done using TANNER EDA v14 tool using CMOS 45 nm technology. Here we are using NMOS transistors because PMOS transistors are slower in comparison to NMOS transistors. The W/L ratio of NMOS is 90/45nm is taken. And the average power dissipation, slew rate and transconducatnce of the carry signal have been measured with variation of the supply voltage and current.

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