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Design of Dual and Swing Restored Complementary Pass Transistor Logic for Low Power Ripple Carry Array Multiplier

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Abstract: In a conventional array multiplier many number of CMOS structures are used in designing. Here this paper presents a multiplier that uses an alternative internal logic structure in designing. The project uses pass transistors logic designs leading to reduction of power usage.

Keywords: *Pass Transistor Logic (PTL), Ripple Carry Array Multiplier (RCAM), Dual Pass Transistor (DPT), Complementary Pass Transistor Logic (CPL)*

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1. INTRODUCTION

A multiplier is an interesting design example because it affords a rich set of design choices. Energy efficiency is one of the required features for modern electronic systems. Power reduction is a serious concern now days. As the MOS devices are wide spread, there is high need for circuits which consume less power, mainly for portable devices which run on batteries, like Laptops and hand-held computers.

The Pass-Transistor Logic (PTL) is a better way to implement circuits designed for low power applications. The paper replaces the static CMOS in ripple carry array multiplier with an equivalent circuit, so that we can easily feed the schematic representation of a multiplier efficiently in a FPGA.

The paper reports the design and performance comparison and transient analysis of the multiplier implemented with CMOS logic and pass transistors (dual pass transistor and swing restored complementary pass logic) styles order to reduce power consumption. The half adder in Multiplication is the fundamental arithmetic operation that is broadly used in many VLSI systems. For simplicity this paper presents 2×2 ripple carry array multiplier using the above shown module.

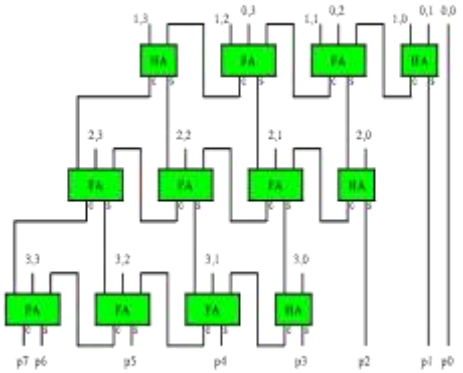


Fig. 1: 4×4 Ripple Carry Array multiplier

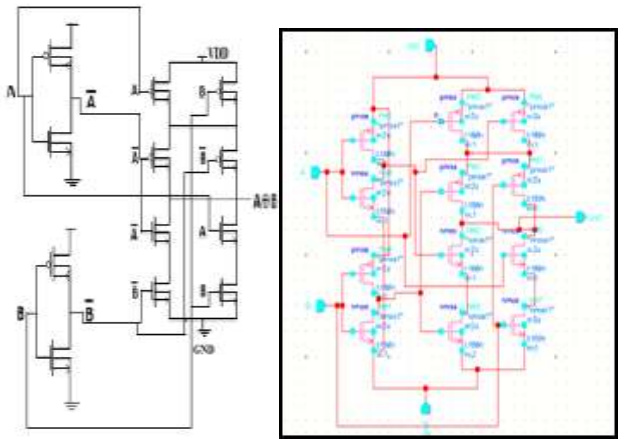
1.1 Operation of RCAM

Ripple Carry Adder Multiplier (RCAM) module, works on the basic principle of the partial product of present stage added with partial product of the previous stage and carry bits are properly propagated. The carry terms C0 to C3 are obtained. The paper presents two high speed and low power array multiplier cells designed with alternative internal logic structure.

2. SCHEMATIC REPRESENTATION

2.1 Conventional RCAM Optimization

The half adder in the multiplier is formed by two main blocks. In Fig 2.Block 2.1, 2.2 represents XOR & AND gate to obtain sum and carry respectively. Regarding the optimization of RCAM the previous papers published only using standard CMOS [1].In this logic design the usage of transistor and the power consumption is also more.



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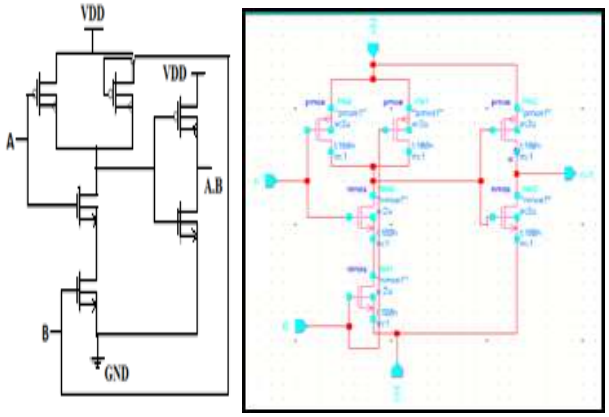
Block 2.1XOR (sum)



Block 2.2 AND (carry)

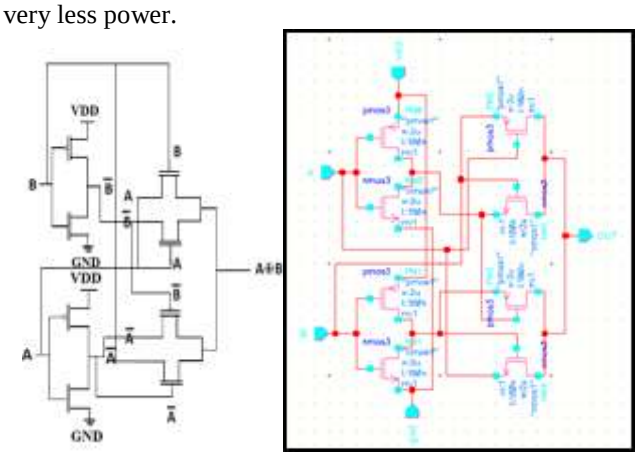
Fig. 2: RCAM designed with CMOS logic.

In order to reduce the number of transistors and power consumption it is necessary to develop a new logic structure.

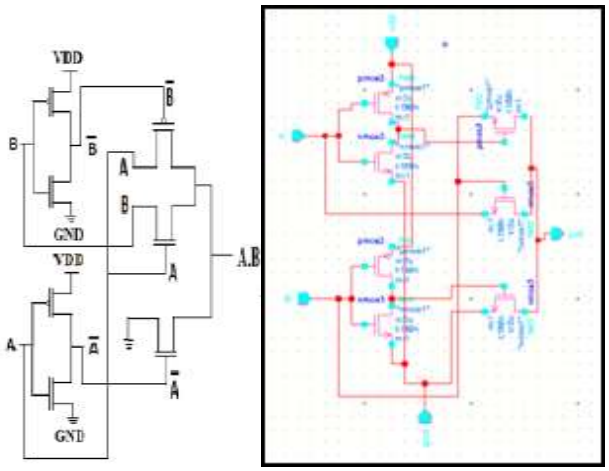
This paper presents different options for logic design like Dual Pass Transistor (DPL) and Swing Restored Complementary Pass Transistor Logic (SR-CPL).This logic structures are used to build the RCAM effectively.

2.2 Proposed Logic Structure 1: Dual Pass Transistor Logic

To avoid problems of reduced noise margins in CPL, twin PMOS transistor branches are added to N-tree in DPL. This addition results in increased input capacitances. However its symmetrical arrangement and double transmission characteristics compensate for the speed degradation arising from increased loading. The full swing operation improves circuit performance at reduced supply voltage with limited threshold voltage scaling. The main advantage of the DPL is that the two inputs can be applied to the transistor at the same time and it can work with the very less power.



Block 3.1: XOR (sum)



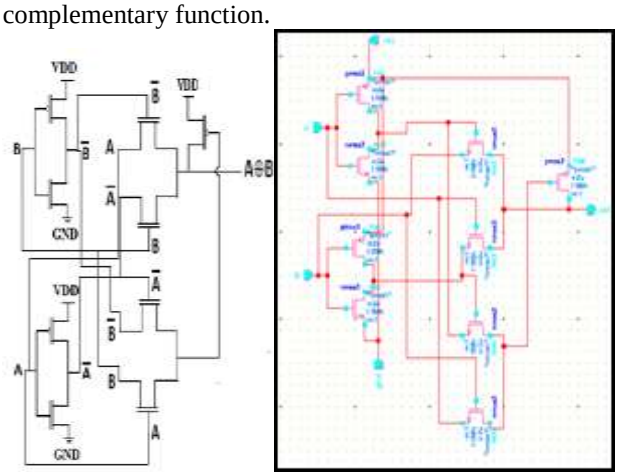
Block 3.2: AND (carry)

Fig. 3: RCAM designed with DPL

To obtain the balance delay in sum and carry output and the pass transistor powerless/groundless logic is designed in order to reduce the power consumption. The resultant multiplier seems to be more efficient on regards of power consumption and delay when compared with other ones reported previously. This stimulation environment has been used for comparing the RCAM with its output power.

2.3 Proposed Logic Structure 2: Swing Restored Complementary Pass Transistor Logic

The swing restored complementary pass transistor works with the basic principle of complementary pass transistor. The complementary principle holds in CPL since the pass variables are directly passed from the inputs to the outputs, so an inversion of the pass variables gives complementary function.



Block 4.1: XOR (sum)

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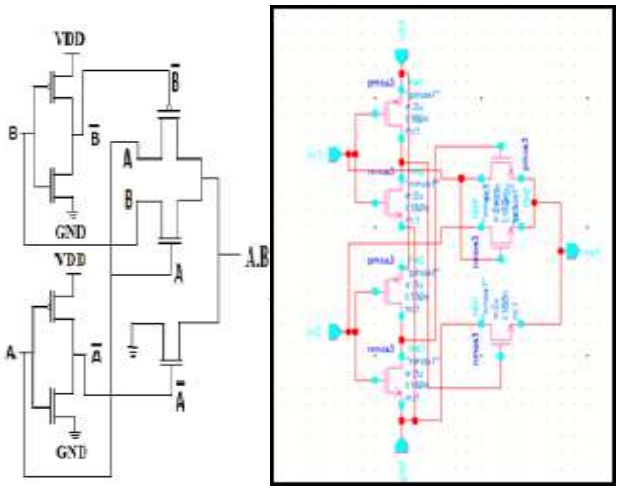

Block 4.2: AND (carry)

Fig. 4: RCAM designed with SR-CPL

The features and advantages of this logic structure are as follows.

i. The capacitive load for the input has been reduced, as it is connected only to some transistor gates and no longer to some drain or source terminals. Thus, the overall delay for larger modules where the signal falls on the critical path can be reduced.

ii. The propagation delay for the *So* and *Co* outputs can be tuned up individually by adjusting the XOR and the AND gates.

iii. The inclusion of the half adder outputs can be implemented by interchanging the XOR signals, and the AND gates to NAND gates at the input of the multipliers, improving in this way the performance for load-sensitive applications

3. LAYOUT REPRESENTATION

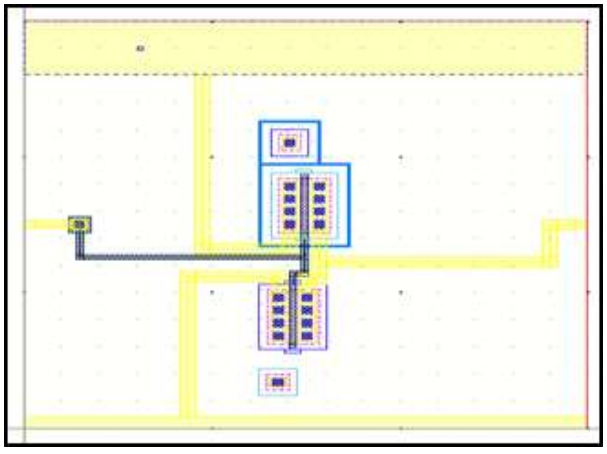

Fig. 5: Layout of DPL NOT gate

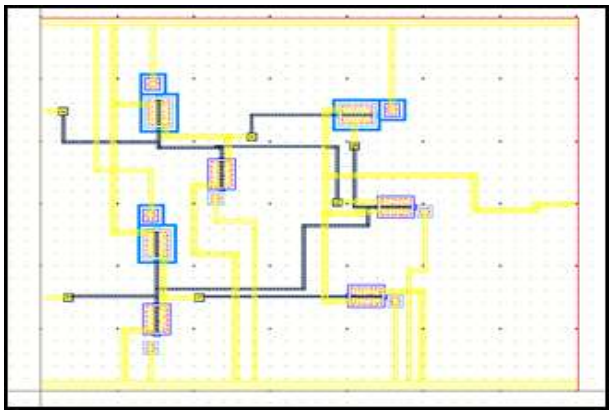

Fig. 6: Layout of DPL AND gate

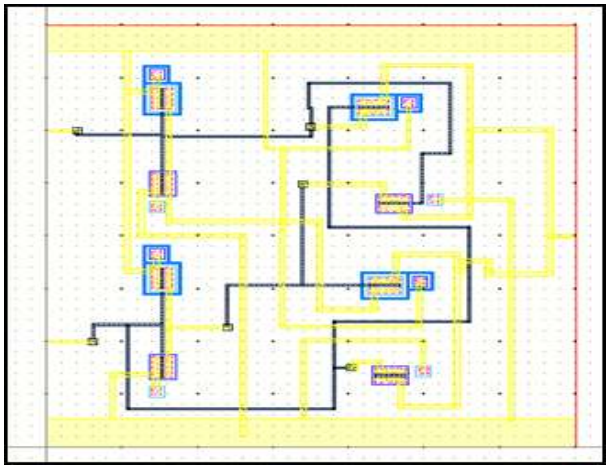

Fig. 7: Layout of DPL EXOR gate

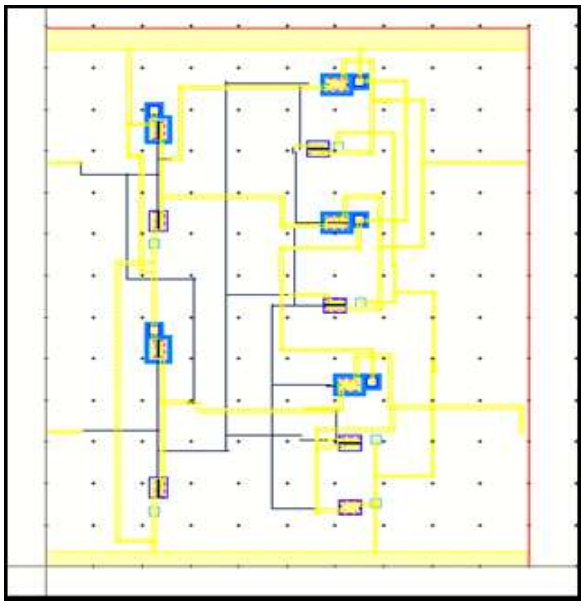

Fig. 8: Layout of DPL half adder

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4. WORK AND TEST METHODOLOGY

i. Design of conventional half adder, RCAM using Cadence Virtuoso [1].
ii. Simulation of the conventional Ripple Carry Array Multiplier to get outputs for multiplication operation for many bit number [2].
iii. Power analysis for the conventional RCAM circuit [3].
iv. Design of new model of RCAM using cadence virtuoso [4].
v. Simulation of the new model of RCAM to get outputs for multiplication operation [5].
vi. Power analysis for the new model of RCAM [6].

5. SIMULATION ENVIRONMENT

The stimulation environment has been used for comparing the RCAM analysed. The main advantage of using this stimulation environment is that the following power components are taken into account. Table 2 shows the performance analysis of the RCAM using DPL, SR-CPL

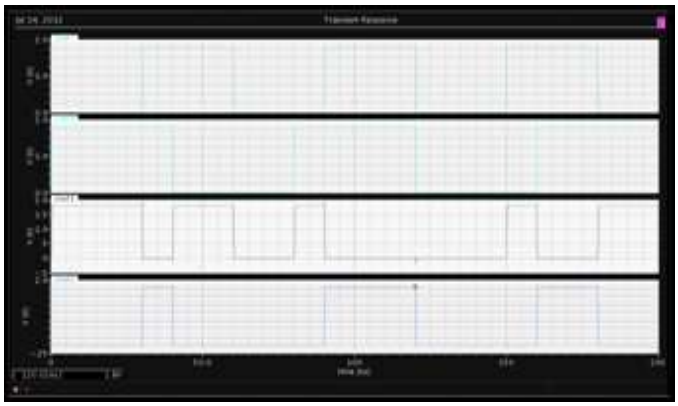

Fig. 9: Simulation of RCAM using DPL

The above shown figure represents the transient analysis of RCAM using DPL logic

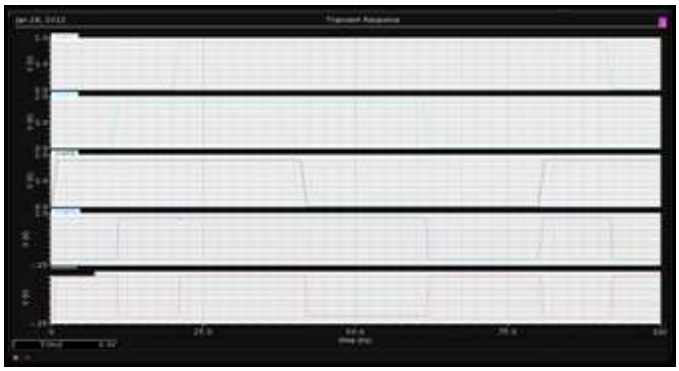

Fig. 10: Simulation of RCAM using SR-CPL

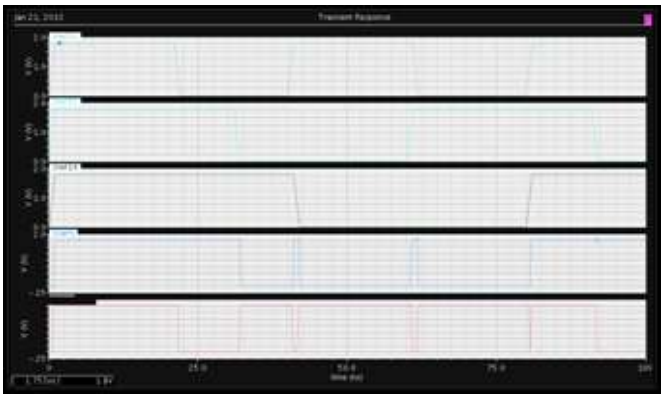

Fig. 11: Simulation of RCAM using CMOS

The above shown figure represents the transient analysis of RCAM using SR-CPL logic.
The above shown figure represents the power analysis of RCAM using DPL logic.

6. RESULT ANALYSIS

The resultant RCAM show to be more efficient on regards of power consumption, reduction in number of transistors when compared with CMOS logic structure.

The number of transistor of transistor in CMOS is 56; whereas the DPL has only 27.Thus 29 transistors can be reduced and the static power of .99pW is also reduced.

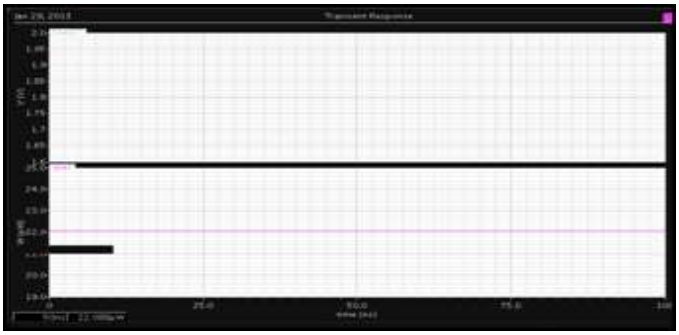

Fig. 12: Power analysis of RCAM using DPL

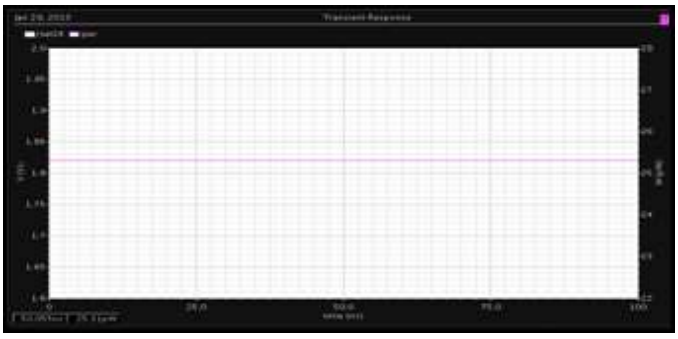

Fig. 13: Power Analysis of RCAM using SR-CPL

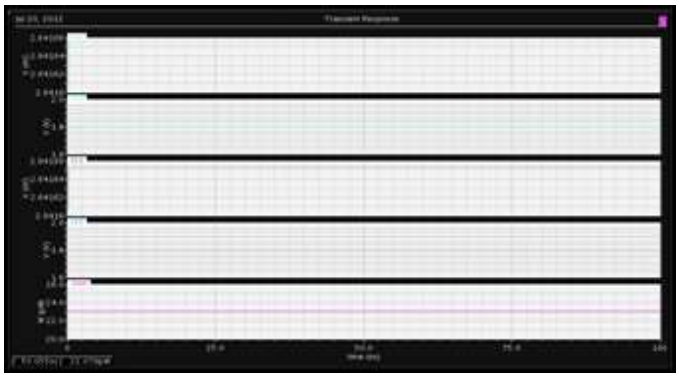

Fig. 14: Power Analysis of RCAM using CMOS

Not only the number of transistor reduces but also static power consumption can be reduced to the notable amount. When 2×2 RCAM is used the static power consumed by the CMOS is 23.08pw but by the DPL logic it only uses 22.09pw, thus about .99pw power is reduced. Similarly if, 4×4, 8×8 RCAM is built using DPL then 1.98pw, 3.96pw static power can be reduced. Therefore if multiplier block gets increased the static power dissipation of the CMOS gets increased instead the DPL logic uses the less power when compared to CMOS.

Tab. 1 : Analysis of Different Bit multiplier

MULTIPLIER	NO.OF TRANSISTOR			STATIC POWER(pW)	
MODEL	CMOS	DPL	SRCPL	CMOS	DPL
2×2	56	34	36	23.07	22.08
4×4	504	316	304	46.16	44.18

7. CONCLUSION

An alternative internal logic structure for designing Ripple Carry Array Multiplier is introduced; they are pass transistor logic design (Dual Pass Transistor Logic and Swing Restored Complementary Pass Transistor Logic). These logic are designed with 180nm technology, stimulated and compared against CMOS logic. The usage of the DPL in RCAM definitely leads to reduction in number of transistor and static power consumption.

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