Multi level DVR with Energy Storage System for Power Quality Improvement

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Abstract: - In this Paper, DVR of different voltage injection schemes is used to mitigate Sag, Swell and compensate Harmonics. The Reference Voltage signals are generated by SRF theory and unit vector template generation is used to estimate the load voltages. The performance of DVR is compared when BESS and Capacitor are used as source for the VSC.

The power quality issues such as Sag, Swell and Harmonics are compensated using Multi level Neutral Point Clamped inverter based DVR employing SPWM, SVPWM modulation techniques. In order to evaluate the performance of DVR, simulations are carried out using MATLAB/SIMULINK software.

Keyword: *DVR, Sag, Swell, Harmonics, BESS (battery energy storage system), SPWM, SVPWM, THD.*

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1. INTRODUCTION

An ideal distribution power system should provide constant energy flow with pure sinusoidal voltage to the customers at the load side. However, in practical situations, mostly in case of distribution systems, that have many nonlinear loads, these affects the quality of supply. Due to the presence of these non-linear loads, supply waveforms purity is lost in several places. so that power quality issues are produced[1], [2].

Voltage sags (dips) are one of the most occurring power quality problems. The decrement in magnitude of voltage of short duration between 0.1 to 0.9 when compared with nominal voltage from 0.5 sec's to few sec's. They occur more repeatedly and hence cause severe issues and economical losses. There are several methods to mitigate voltage sag in power systems. Of these, DVR and STATCOM are better suitable devices, these are performed using VSC principle [2].

Swell is the opposite form of a Sag, it is an increment in voltage (AC) for a time period of 0.5sec to 1 minute. For swells, rapid reduction in large load, a 1-phase fault that occur on 3- phase systems are common sources. due to swells electrical contact degradation, light flickering, and semiconductor damage in electronics cause failures in hard server. The solution for swells is UPS (uninterrupted power supply) Solutions [3].

A harmonic (unwanted signals) is given as " A periodic component of the sinusoidal quantity/wave that is having frequency which is the positive integral(whole-number) multiple of a fundamental(original) frequency." Some referrals having "pure" or "clean" power that are not having harmonics. But they exist only in the laboratory [4].

This paper is structured as follows: Section 2 describes briefly the operation of DVR. Section 3 presents the principle of operation of NPC inverter. Section 4, Presents the space vector pulse width modulation (SVPWM) Technique, PD (phase disposition) technique and SRF theory. Section 5 contains the proposed system of the DVR output voltage. Section 6 represents results of simulations and analysis for different configurations of DVR and the output results and conclusion in Section 7.

2. OPERATION OF DVR

The DVR can regulate the load voltage from the problems such as sag, swell, and harmonics in the supply voltages. Hence, it can protect the critical consumer loads from tripping and consequent losses.

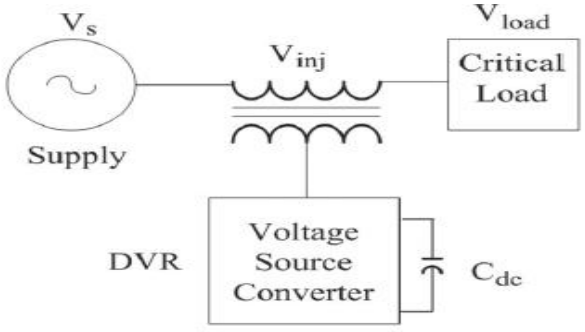

Fig1(a)

The schematic of a DVR-connected system is shown in Fig. 1(a). The voltage Vinj is inserted such that the load voltage Vload is constant in magnitude and is undistorted, although the supply voltage Vs is not constant in magnitude or distorte

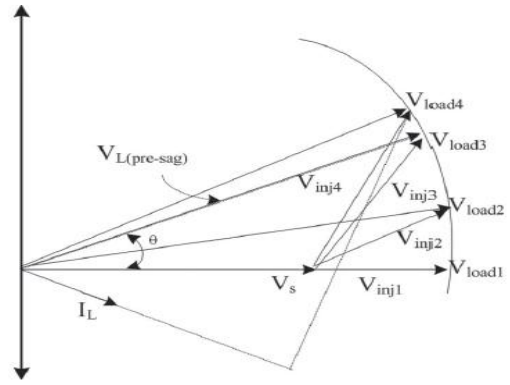

Fig 1(b) phasor diagram of different voltage injection schemes

During the voltage sag, the voltage is reduced to Vs with a phase lag angle of θ. Now, the DVR injects a voltage such that the load voltage magnitude is maintained at the pre-sag condition. According to the phase angle of the load voltage, the injection of voltages can be realized in four ways. Vinj1 represents the voltage injected in-phase with the supply voltage. The DVR is operated in this scheme with a battery energy storage system (BESS).With the injection of *V*inj2, the load voltage magnitude remains same but it leads *Vs* by a small angle. In *V*inj3, the load voltage retains the same phase as that of the pre-sag condition, which may be an optimum angle considering the energy source. *V*inj4 is the condition where the injected voltage is in Quadrature with the current, and this case is suitable for a capacitor-supported DVR as this injection involves no active power.

3. NPC INVERTER

The NPC inverter is used because All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back inter-connection;

The three level inverter offers several advantages over the common two level inverter such as reduced harmonics and Efficiency is high for fundamental frequency switching.

Figure2 shows the circuit configuration of the NPC inverter. Each leg has four IGBTs connected in series. The applied voltage on the IGBT is one-half that of the conventional two level inverter. The bus voltage is split in two by the connection of equal series connected bus capacitors. Each leg is completed by the addition of two clamp diodes. The NPC inverter can produce three voltage levels in the output I,e.+ Vdc, 0, -Vdc.

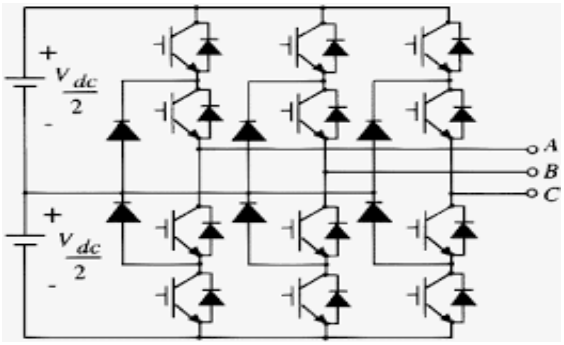

Fig2: NPC inverter

4. CONTROL STRATEGIES

4.1 Space Vector PWM (SVPWM)

The space vector PWM (SVPWM) is an alternative method used to control three-phase inverters.This method gives the both voltage magnitude and angle shift information. SV-PWM is to translates phase voltage (phase to neutral) references, coming from the controller, into modulation times/duty-cycles to be applied to the PWM peripheral. It is used to maximize DC bus voltage exploitation and minimization of the harmonic content.

4.2 Phase Disposition (PD)

The Carrier-based implementation the phase disposition PWM scheme is used. Fig.3 demonstrates the sine- triangle method for a seven-level inverter. Therein, the R-phase modulation signal is compared with six (m-1 in general) triangle waveforms. In the carrier-based implementation at every instant of time the modulation signals are compared with the carrier and depending on which is greater, the definition of the switching pulses is generated. Amplitude of modulation index ma = 2 A m / (m-1) Ac

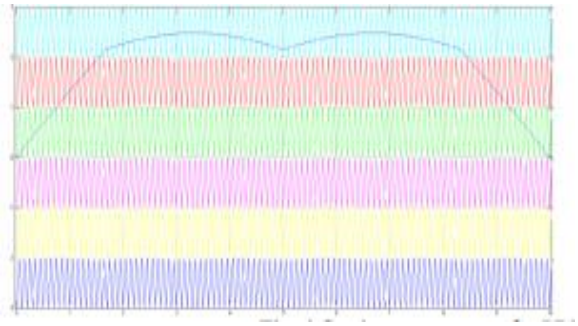

Fig3: PDPWM with SVPWM reference

4.3SRF Theory

The dqo transform (often called the park transform) is a space vector transformation of three phase time domain signals from a stationary phase coordinate system (ABC) to a rotating coordinate system (dq0).The transform applied to time-domain voltages in the natural frame (i.e.V_a, V_b, V_c) is as follows

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \text{.....(1)}$$

Where θ is the angle between the rotating and fixed coordinate system at each time t and is an initial phase shift of the voltage. The inverse transformation from the dqo frame to the natural abc frame

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix}\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} \text{.....(2)}$$

As in the Clarke Transform, it is interesting to note that the 0-component above is the same as the zero sequence component in the symmetrical components transform. For example, voltages the zero sequence component for both the dqo and symmetrical components transform is

$$\frac{1}{3} = (V_a + V_b + V_c) \text{ ……..(3)}$$

The dqo transform of balanced three-phase voltages The following equations take a two-phase quadrature voltage along the stationary frame and transforms it into a two-phase synchronous frame (with reference frame aligned to the voltage):

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 0 \\ -\sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} \text{ ……..(4)}$$

Note that in the dqo frame, the 0-component is the same as that in the αβ0 frame. Moreover, as in the Clarke transform, the 0-component is zero for balanced three-phase systems. Therefore in balanced systems, zero sequence component is omitted

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} = \begin{bmatrix} V_m \cos(\omega t) \\ V_m \sin(\omega t) \\ 0 \end{bmatrix} \text{ ……(5)}$$

The dqo transform of this voltage is:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \text{ ……(6)}$$

The inverse transform is as follows:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} V_d \\ q \end{bmatrix} \text{ ……(7)}$$

The dqo transformation can be similarly applied to the current. From a two-phase quadrature stationary (αβ0) current of them form (where δ is the angle at which the current lags the voltage):

$$\begin{bmatrix} I_\alpha \\ I_\beta \\ I_0 \end{bmatrix} = \begin{bmatrix} I_m \cos(\omega t - \delta) \\ I_m \sin(\omega t - \delta) \\ 0 \end{bmatrix} \text{ ……(8)}$$

Then transform it into a two- phase synchronous (dq0) frame:

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} \text{ ……(9)}$$

5. PROPOSED WORK

In this proposed work, three level inverter based DVR with BESS and capacitor support using SVPWM and SPWM techniques is implemented to mitigate sag, swell and compensate harmonics. The three level inverter offers several advantages over the common two level inverter such as reduced harmonics and high efficiency for fundamental switching frequency. The performance of NPC based 3-level inverter based DVR with BESS and capacitor support is compared when employing SVPWM and SPWM techniques.

6. SIMULATION RESULTS

6.1 THREE-LEVEL INVERTER BASED DVR WITH SPWM

6.1(A) capacitor supported DVR with 3-level SPWM

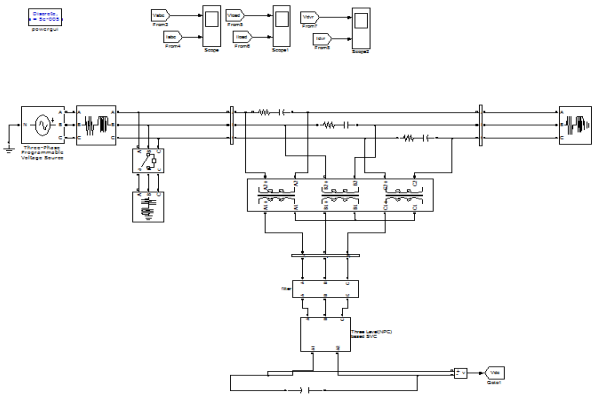

Fig 6.1(a): MATLAB simulation Circuit DVR supported system

6.1.1 Sag compensation

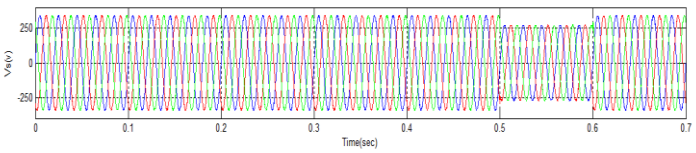

Fig 6.1(b): source voltage with sag

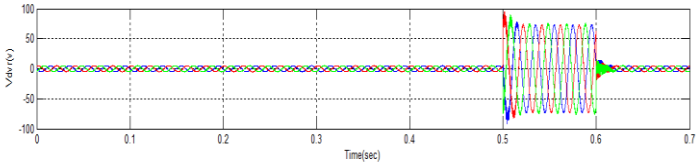

Fig6.1(c): DVR injected voltage

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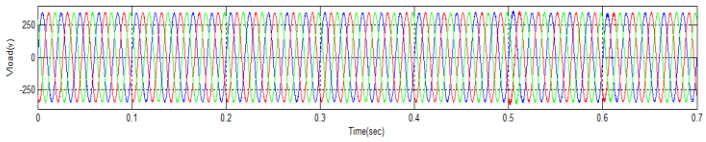

Fig6.1(d): Load voltage

THD analysis of load voltage

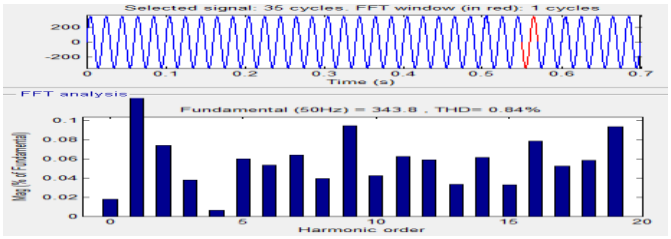

Fig 6.1(e): Sag at load voltage

Fig 6.1(b) shows Sag created in the supply voltage from 0.5 sec to 0.6sec. The load voltage is maintained constant by injecting proper compensation voltage by the DVR as shown in Fig 6.1(c),The regulated load voltage with constant amplitude is shown in Fig 6.1(d).

6.1.2 Swell compensation

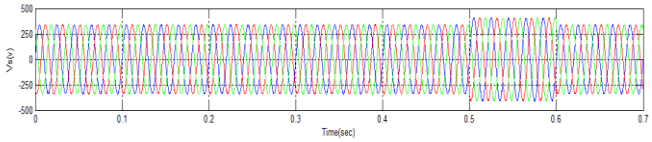

Fig 6.1(f): source voltage

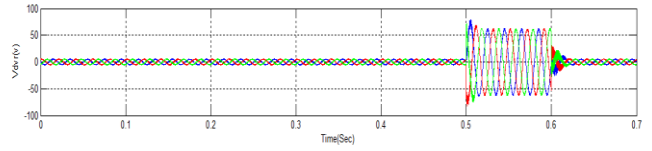

Fig 6.1(g): DVR injected voltage

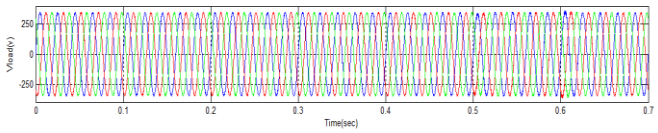

Fig 6.1(h): Load voltage

THD analysis of load voltage

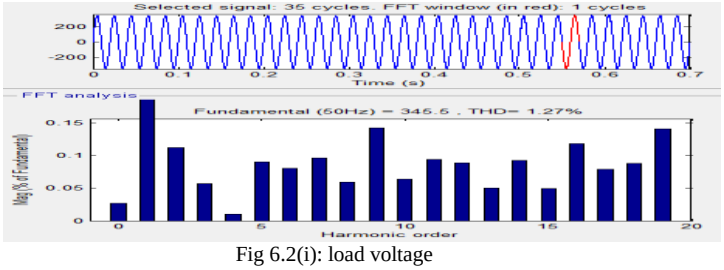

Fig 6.2(i): load voltage

Fig 6.1(f) shows Swell created in the supply voltage from 0.5 sec to 0.6sec. The load voltage is maintained constant by injecting proper compensation voltage by the DVR as shown in Fig 6.1(g),The regulated load voltage with constant amplitude is shown in Fig6.1(h).

6.1 (b) BESS supported DVR with 3-level SPWM

6.1.3 Harmonic compensation

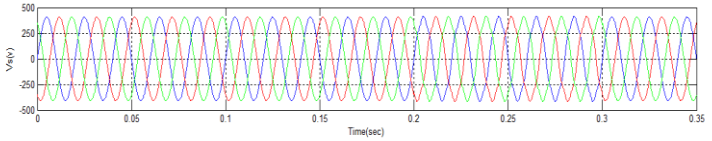

Fig 6.1(j): Source voltage with harmonics

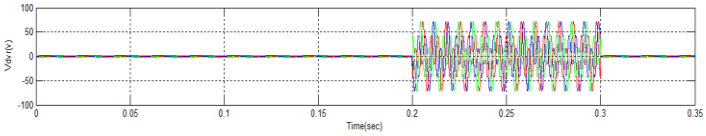

Fig 6.1(k): DVR injected voltage

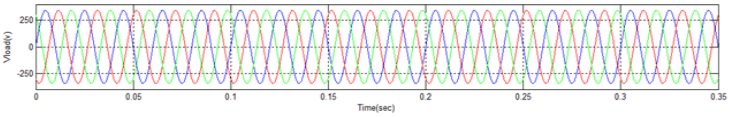

Fig 6.1(l): Load voltage

THD analysis of load voltage

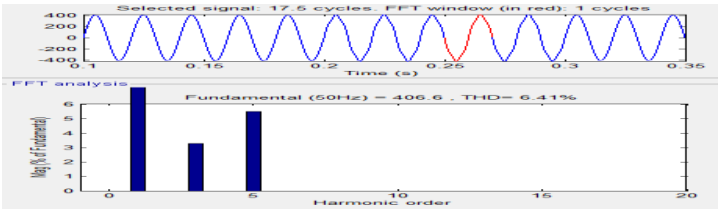

Fig 6.1(m): source voltage

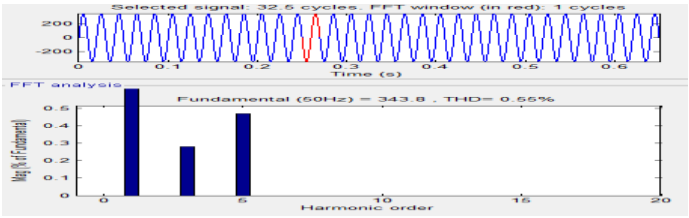

Fig6.2(n): Load voltage.

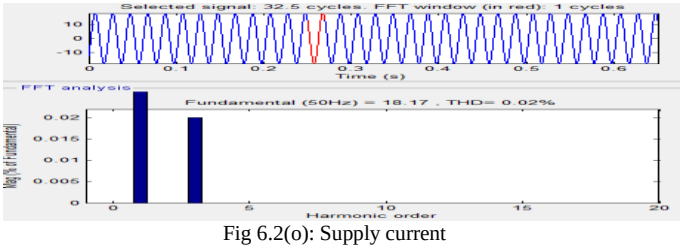

Fig 6.2(o): Supply current

The compensation of harmonics in the supply voltage is demonstrated in Fig 6.1(j),(k),(l), at 0.2sec, the supply voltage is distorted and continued for five cycles. The load voltage is maintained sinusoidal by injecting proper compensation voltage by the DVR

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6.1.4 Sag and swell compensation

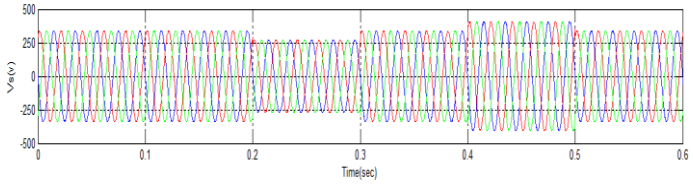

Fig 6.1(p): Load voltage with sag and swell

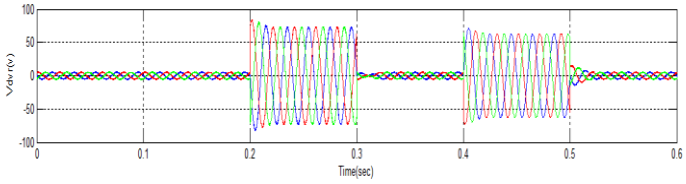

Fig 6.1(q): DVR injected voltage

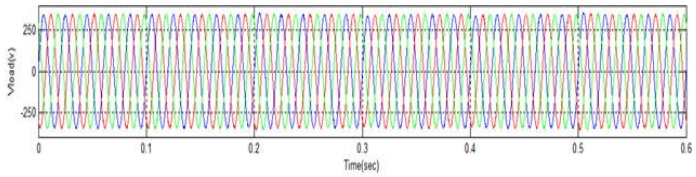

Fig 6.1(r): Load voltage

THD analysis of load voltage

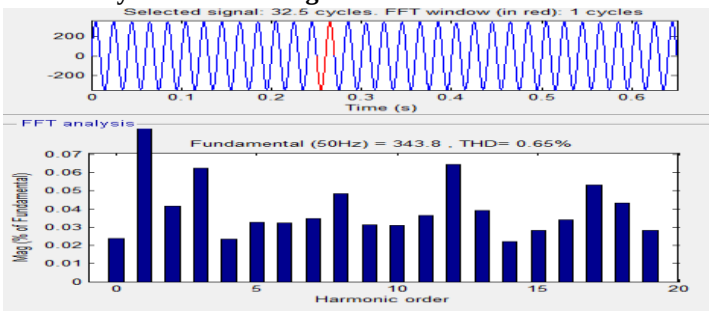

Fig 6.1(s): Sag at load voltage

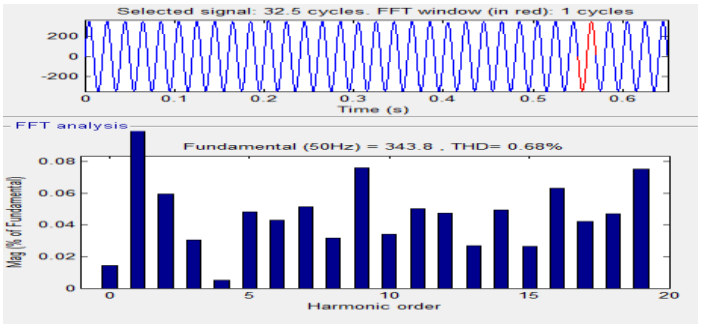

Fig 6.1(t): Swell at load voltage

The Fig6.1(p) shows that, at 0.2sec to 0.3 sec Sag, and at 0.4sec to 0.5sec swell is created in the supply voltage, The load voltage is maintained sinusoidal by injecting proper compensation voltage by the DVR shown in Fig6.1(q), The load voltage is regulating to constant amplitude in Fig6.1(r).

6.2 THREE-LEVEL INVERTER BASED DVR WITH SVPWM

6.2(A) capacitor supported DVR with 3-level SVPWM

6.2.1 Sag compensation

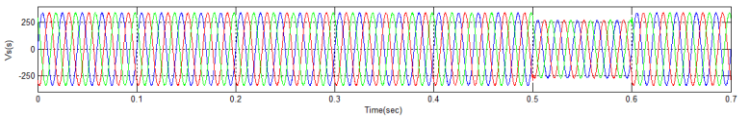

Fig 6.2(a): source voltage

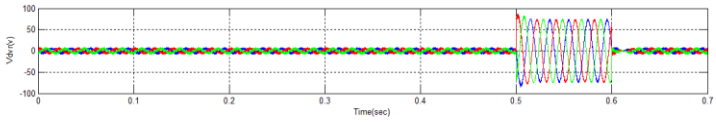

Fig6.2(b): DVR injected voltage

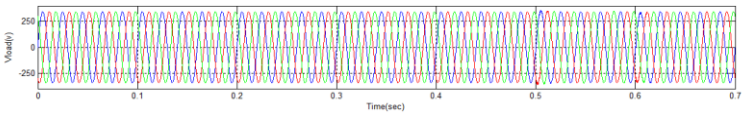

Fig6.2(c): Load voltage

THD for capacitor sag

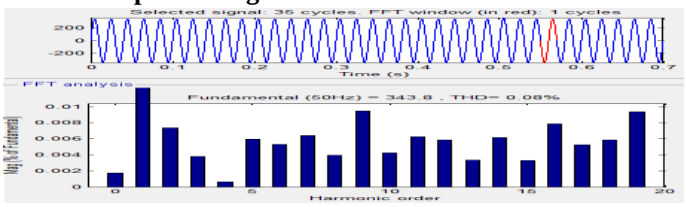

Fig6.2(d): Sag at load voltage

Fig 6.2(a) shows Sag created in the supply voltage from 0.5 sec to 0.6sec. The load voltage is maintained constant by injecting proper compensation voltage by the DVR as shown in Fig 6.2(b),The regulated load voltage with constant amplitude is shown in Fig 6.2(c).

6.2.2 Swell compensation

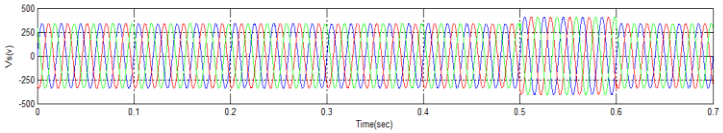

Fig 6.2(e): source voltage

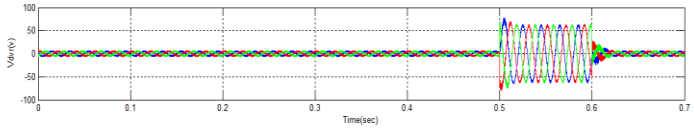

Fig 6.2(f): DVR injected voltage

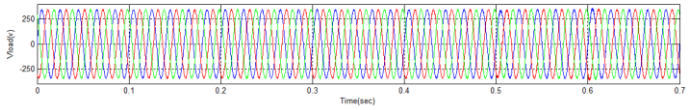

Fig 6.2(g): Load voltage

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THD for capacitor swell

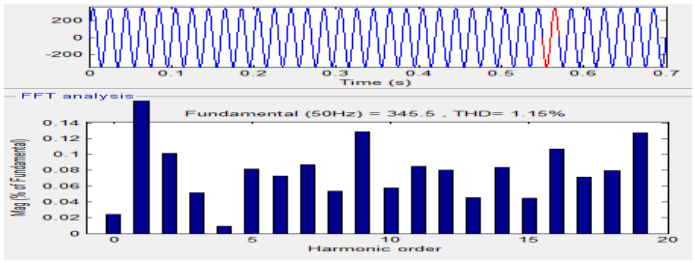

Fig6.2(h): swell at load voltage

Fig 6.2(e) shows Swell created in the supply voltage from 0.5 sec to 0.6sec. The load voltage is maintained constant by injecting proper compensation voltage by the DVR as shown in Fig 6.2(f),The regulated load voltage with constant amplitude is shown in Fig6.2(g).

6.2(b) BESS supported DVR with 3-level SVPWM

6.2.3 Harmonics compensation

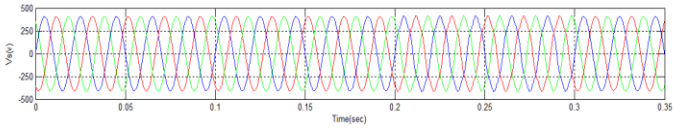

Fig 6.2(i): Source voltage

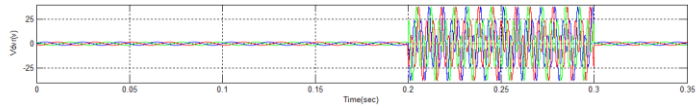

Fig 6.2(j): DVR injected voltage

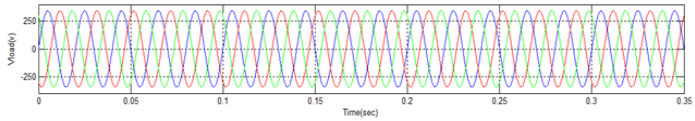

Fig6.2(k): Load voltage

➢ **THD for BESS harmonics**

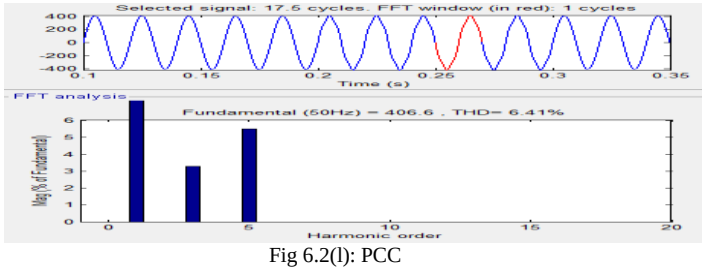

Fig 6.2(l): PCC voltage

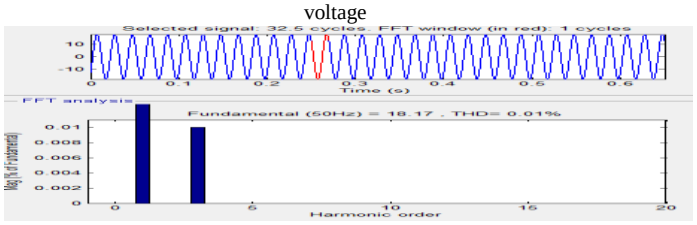

Fig 6.2(m): Supply current

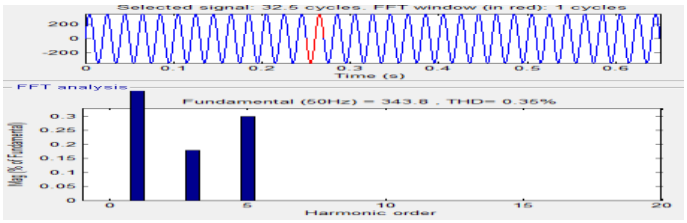

Fig 6.2(n): Load voltage

The compensation of harmonics in the supply voltage is demonstrated in Fig 6.2(i),(j),(k), at 0.2sec, the supply voltage is distorted and continued for five cycles. The load voltage is maintained constant by injecting proper compensation voltage by the DVR

6.2.4 Sag and Swell compensation

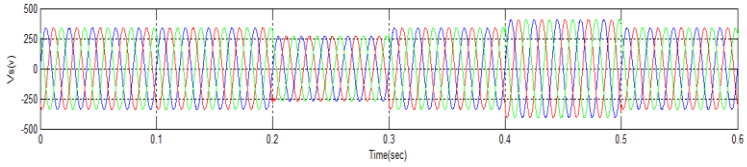

Fig 6.2(o): Source voltage

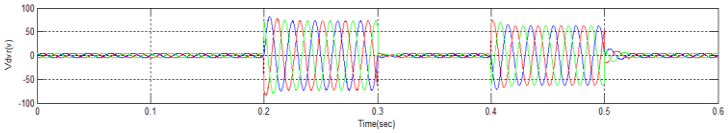

Fig 6.2(p): DVR injected voltage

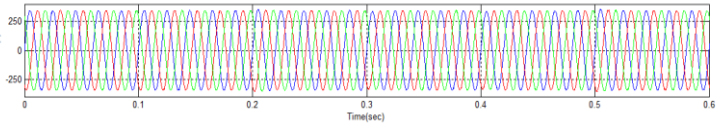

Fig 6.2(q): Load voltage

➢ **THD for BESS sag and swell**

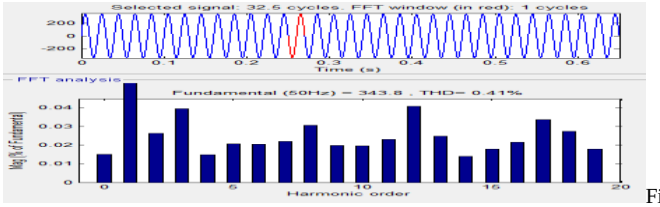

Fig 6.2(r): Sag at load voltage

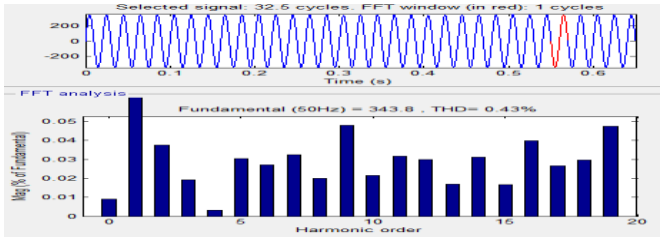

Fig6.2(s): Swell at load voltage

Table-1 BESS Harmonic compensation

	2-level BESS with SPWM	3-level BESS with SPWM
Source voltage	6.41	6.41
Load voltage	0.55	0.35
Source current	0.02	0.01

Table-2 Sag and swell mitigation

	3-level SPWM		3-level SVPWM	
	Capacitor supported	BESS supported	Capacitor supported	BESS supported
Sag	0.84	0.65	0.08	0.41
Swell	1.27	0.68	1.15	0.43

7. SIMULATION ANALYSIS

The performance of the DVR is demonstrated for different power quality disturbances such as voltage sag, swell and Harmonics. The above outputs shows the transient performance of the system under voltage sag, voltage swell and Harmonic conditions. It is observed that the load voltage is regulated to constant amplitude under both sag and swell conditions.

In order to evaluate the performance of DVR for harmonic compensation, harmonics are injected into the supply voltage. The load voltage is maintained sinusoidal by injecting proper compensation voltage by the DVR, which is clear from the simulation results.

From the results of table 1 it is clear that the load voltage THD is less in case of 3-level BESS supported DVR with SVPWM compared to 3-level BESS supported DVR with SPWM. From table2 it is clear that during sag and swell conditions the THD in load voltage is less in case of 3-level BESS supported DVR with SVPWM compared to all other topologies i.e 3-level capacitor supported DVR with SVPWM, 3-level Capacitor & BESS supported DVR with SPWM.

Hence it is concluded that a 3-level BESS supported DVR with SVPWM performance is efficient compared to 3-level DVR with SPWM in the mitigation of Power Quality issues.

Conclusion

The performance of DVR is evaluated with various injection schemes i.e Capacitor supported and BESS supported system. A comparison of BESS and Capacitor supported three level inverter based DVR using SPWM& SVPWM techniques in mitigating power quality issues is presented. A 3-level BESS supported DVR with SVPWM inverter gives better performance compared to 3-level BESS & Capacitor supported DVR with SPWM & 3-level SVPWM Capacitor supported DVR. Also 3-level SVPWM inverter performs well compared to 3-level SPWM inverter.

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