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Design of Frequency Divider (FD/2 and FD 2/3) Circuits for a Phase Locked Loop

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Abstract— This paper reports on three design of Frequency Divider (FD/2) and Frequency Divider (FD 2/3) circuits. Tanner EDA tool developed on 130nm CMOS technology with a voltage supply of 1.3 V is used to build, model, and compare all circuits. For the FD/2 circuit, E-TSPC Pass Transistor logic uses 1.77 µW, whereas TSPC logic consumes 5.57 µW for the FD 2/3 circuit. It implies that the TSPC logic is the best solution since it meets the speed and power consumption requirements.

Keywords— Frequency Divider, Pass Transistor, Power, Speed, Phase Locked Loop.

I. INTRODUCTION

The development of VLSI technology in the recent days proves to be the primary factor in the field of electronics industry. The integrated circuit plays the vital role in all types of electronic applications, which leads to the industrialization. PLL system design which is commonly used in microprocessors generates a clock at high frequency from an external clock of lower frequency. The PLL is also acts as a clock recovery circuit to generate a clock signal. The generated clock signal is transmitted in serial without synchronization clock. For the PLL to act as a frequency synthesizer, the speed, power consumption and the number of division ratios of the frequency divider are connected to PLL.

To build a PLL, you need the following components: the Charge Pump, the Phase Frequency Detector, the Loop Filter, and the VCD (FD). Fig. 1 is a block schematic of the PLL, as shown.

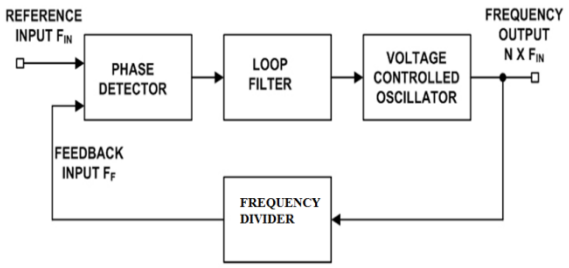

Fig 1. Block Diagram of PLL

It has two inputs, which are connected to the PFD. The reference clock and feedback signal are the two types. UP or DOWN pulse are the two PFD output signals which depend on whether the feedback signal leads or lags the reference signal. The phase difference between the two clock signals is proportional to both output signals. The charge pump translates these pulses in to current that moves into or out of the loop filter. The current gets integrated by the loop filter and generates a voltage which serves as the control for VCO. Increasing the VCO's frequency is easy thanks to the PFD's UP pulse, which "pump" up the control voltage. The FD circuit multiplies the VCO output by the specified bus multiplier.

The closed loop of the FD circuit in the PLL system reduces the frequency of the VCO, resulting in a lower frequency. With the help of the D flip-flop, we can create a frequency divider circuit. This frequency divider circuit, which reduces the frequency of the local oscillator, provides the synthesiser with programmability. Low-power PLL implementation relies on first-stage power reduction of the frequency divider, which is critical to both high-speed performance and low power consumption. Application areas include clock generating, frequency synthesiser, and timing-recovery circuits.

The remainder of the article shows the following; Section II briefs the circuit FD/2. Section III briefs the circuit FD 2/3

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section IV shows the results and discussion and conclusion in section V .

II. FREQUENCY DIVIDER (FD/2) CIRCUIT

To create an output signal, an FD/2 circuit takes the frequency of the input signal. Using the input frequency, half of the output frequency is created.

A. Master Slave FD/2 circuit

The Master Slave FD/2 circuit [1] uses a two-stage regenerative FD to perform the divide-by-two frequency divider step. The Master Slave FD/2 circuit employs an analogue differential latch. A regenerative loop (M3 and M4) and two pull-up devices each are included in the master and slave latches (M9 and M10). There is a regenerative loop in the master latch as well (M3) (M5 and M6 in the master and M11 and M12 in the slave). The master is in the sensing mode when CK is at a high level, and M5 and M6 are deactivated (M5 is disabled). For the same purpose, the slave is configured to store data by turning on M11 and M12. When CK drops, the opposite happens. Stacked or pass transistors aren't used in this circuit, and the gate channel capacitance of the PMOS transistors doesn't have much of an impact on the critical path. In the nodes X1, Y1, X2 and Y2, these devices are (velocity) saturated at virtually the whole voltage swing. Figure 2 shows the schematic representation of MS FD/2 circuit.

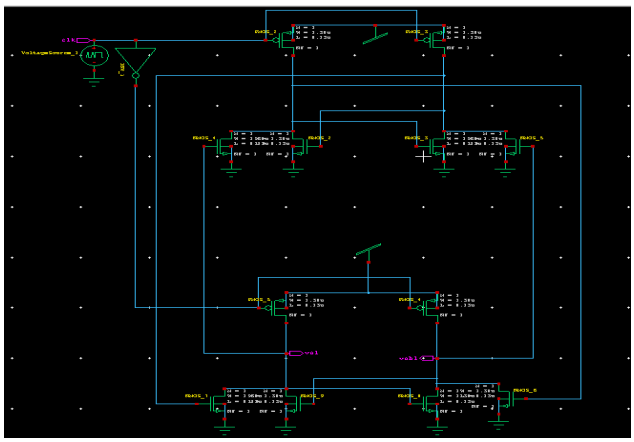

Fig 2. MS FD/2 circuit

B. True Single Phase Logic FD/2 circuit

As may be shown in Figure 3 [2], the TSPC logic [8] FD/2 circuit is shown. To decrease internal node capacitance, input clock-operated transistors are placed closest to the power rails. The MS FD/2 circuit has nine transistors, while these have just nine. Transistor-to-transistor contacts are greatly decreased. There is a direct correlation between reduced connecting capacitance between transistors and lower power consumption, as shown by this graph. As a result, the first level of the PLL uses this dynamic divider. The input node (in) has a total capacitance of 15 fF, which includes the 4.5 fF connector capacitance. A post-layout parasitic extraction is required to collect this information for use in the final product. When the divider is connected to the following step, the average current use is about 250 nA. The differential VCO's output is used to drive the divider's low input capacitance.

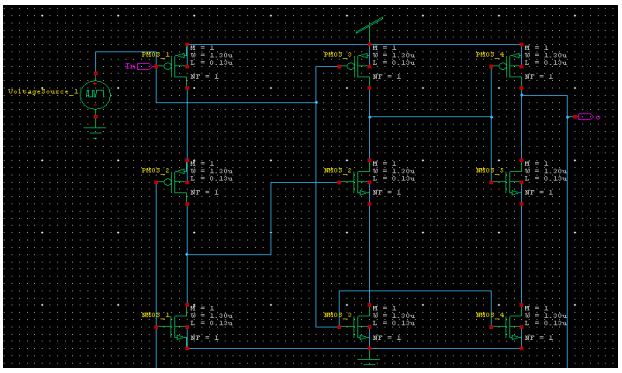

Fig 3. TSPC FD/2 circuit

C. Current Mode Logic (CML) FD/2 circuit

Figure 4 shows the CML differential DLC family [6] used to create the frequency extension circuit's latch gates. There are several uses for the CML in high-speed integrated systems, including as telecommunications, where it can transport data at rates ranging from 312.5 Mbit/s to 3.125 Gbit/s (serial data transceivers, frequency synthesizers, etc.). CML circuits are more efficient than static CMOS circuits because they have a smaller output voltage swing. The input transistors of the differential pair are also able to switch current more quickly because of this. Passing (I) and latching (II) are the two main functions of the CML-based FD/2 circuit (Q). Since they feature a 90-degree phase-shift quadrature output signal with a 50% duty cycle, the passing stage (I) output delays the latching stage (Q).

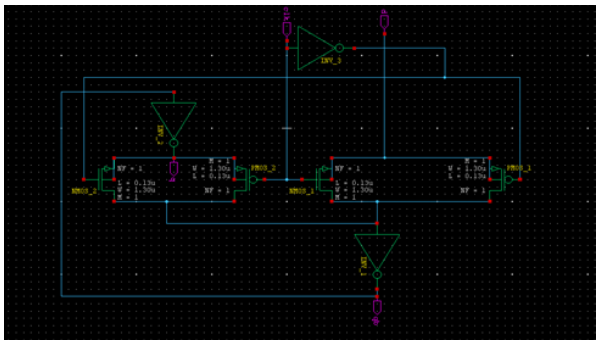

Fig 4. CML FD/2 circuit

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III. FREQUENCY DIVIDER (FD 2/3) TOPOLOGY

When given an input signal, an FD 2/3 circuit outputs a signal with a frequency that is 2/3 the frequency of the input signal. Extensive TSPC reasoning (E-TSPC) Composition rules for single-phase circuits are included in FD 2/3, an extension of TSPC logic.

A. Multiband FD 2/3 circuit

Figure 5 depicts the wideband single-phase FD 2/3 circuit [4] with its two DFFs and two NOR logic gate. FFs include these components. DFF1's final stage is linked to the first NOR gate, while DFF2's initial stage is connected to the second NOR gate. Using DFF1, the short-circuit power may be eliminated by using transistors M2, M25, M4, and M8. Signal MC, a signal logic, maintains the swiching between division ratios of 2 and 3. When MC changes from "0" to "1," nodes S1, S2 and S3 in DFF1 are reset to "0," while transistors M2, M4, and M8 in DFF1 are similarly reset to "0." Since node S3 is "0" and Qb is the next input to the NOR gate in DFF2, the wideband divider in DFF2 operates in divide-by-2 mode.

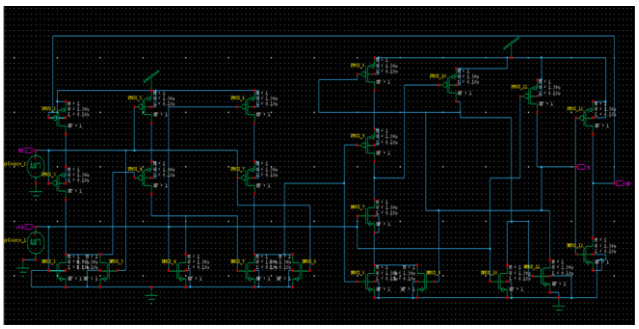

Fig 5. Multiband FD 2/3 circuit

B. MS FD 2/3 circuit

The E-TSPC logic-based MS FD 2/3 circuit architecture is shown schematically in Figure 6 [5]. Negative feedback is used to drive the two D FFs in a Master Slave setup. The FF's initial stage uses more power than its counterpart in terms of design. Pull-up paths use more power as a result, and when the clock signal changes to "1," the SCC is repeatedly drawn. The critical pathway delay caused by the two FFs and the control logic determines the divider's maximum operating frequency. In FD 2/3 logic, an inverter is required between FF1 and FF2, despite the simplicity of the circuit. Parallel transistors are created when control logic and FF are joined, and the increased parasitic capacitance has a negative impact on both speed and power.

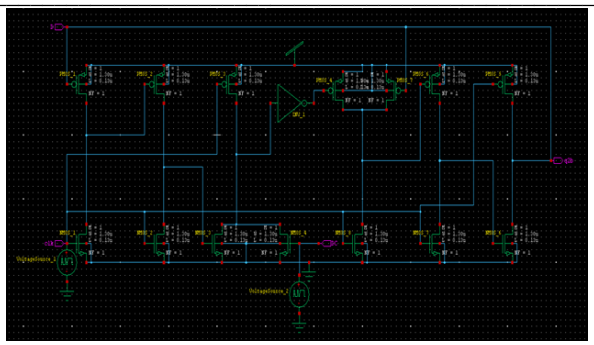

Fig 6. MS FD 2/3 circuit

C. Pass Transistor FD 2/3 circuit

E-TSPC FFs have a minimum height in transistor stacking and so they are useful for low voltage operations.One PMOS transistor is also required for generating low voltage. The switch is a PMOS transistor that receives its driving signal from the divide control signal. Wired-AND logic is used to create the AND gate and its input inverter, which has the benefit of not requiring any additional transistors. The suggested design method is much more impressive than just adding a single pass transistor to the circuit (PT). Logic embedding does not affect the E-TSPC FF architecture in any way. Both speed and power remain identical in the logic incorporated FF architecture, indicating its superiority in terms of performance. Two E-TSPC FF divide-by-3 outputs are swapped for an inverter in the proposed design shown in Figure 7, giving rise to three E-TSPC FF divide-by-3 outputs in total. Final stage of circuit: two D-latch pseudo PMOS inverters are followed by two pseudo PMOS inverters [5]. When the clock signal is one, the outputs of the two inverters are pre-discharged to zero, resulting in a zero voltage at the outputs of the two inverters. It is possible to overcome parasitic capacitance by turning off both the D-PMOS latches and the NMOS transistors at the same time. After setting the clock signal to zero, the D-latch becomes a pseudo-NMOS inverter, enabling the other inverter to be recognised as a legitimate evaluation result.

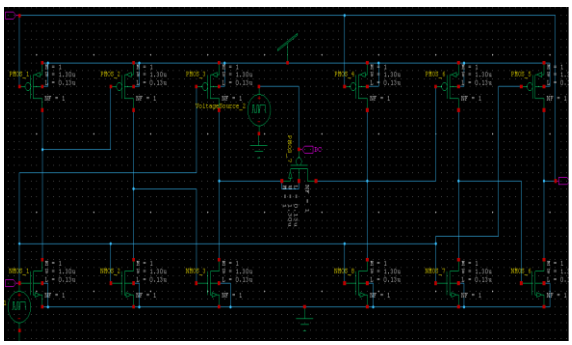

Fig 7. MS FD 2/3 circuit

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IV. SIMULATION RESULTS AND DISCUSSION

Simulations are done in 0.13µm of CMOS technology where V_s of 1.3V in Tanner EDA V15 is used. The simulated output waveforms of FD/2 and FD 2/3 circuits are presented in figure 8 and 9 respectively .

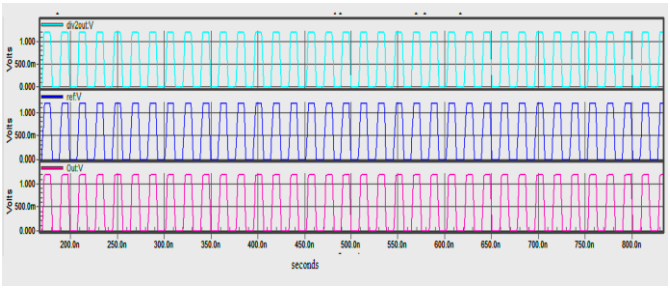

Fig 8. CML FD/2 circuit

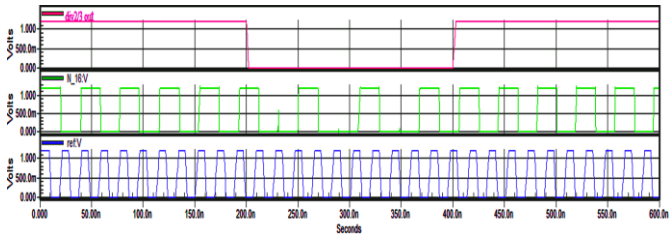

Fig 9. PT FD 2/3 circuit

Table I lists the comparison of FD/2 circuits. The chart in the Figure 10 illustrates power and speed of FD/2 circuits.

TABLE I
OBSERVED PARAMETER VALUES FOR FD/2 CIRCUITS

Sl. no	Parameters	Frequency Divider (FD)/2		
		MS	TSPC	CML
1	Transistor Count	12	9	4
2	Maximum Power Consumption (µW)	5.27	1.77	3.95
3	Speed (GHz)	1.5	3	3.5

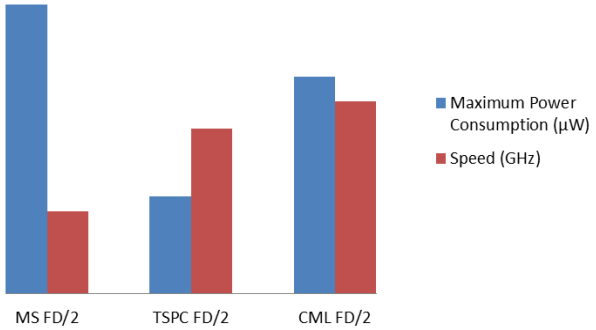

Fig 10. Comparison of FD/2 circuits

It is observed from results that the CML FD/2 is faster when compared to other FD/2 circuits but it consumes more power than TSPC logic since latch is being used. On the other hand, TSPC FD/2 is most suitable for high speed and high frequency applications because it requires only one single clock phase and has only nine transistors. So, the TSPC divider is apparent for use when compared to static divider while working at higher frequencies.

Table II lists the comparison of FD 2/3 circuits. The chart in the Figure 11 illustrates power and speed of FD 2/3 circuits.

By employing Pass Transistor logic instead of other logics, the FD 2/3 circuit consumes less power than other logics since it uses fewer transistors and eliminates superfluous transistors.

TABLE II
OBSERVED PARAMETER VALUES FOR FD 2/3 CIRCUITS

Sl. no	Parameter	E- TSPC Frequency Divider (FD) 2/3		
		Multi band	MS	PT
1	Transistor Count	22	14	13
2	Maximum Power Consumption (µW)	6.25	6.39	5.57
3	Speed (GHz)	2.5	2.5	3

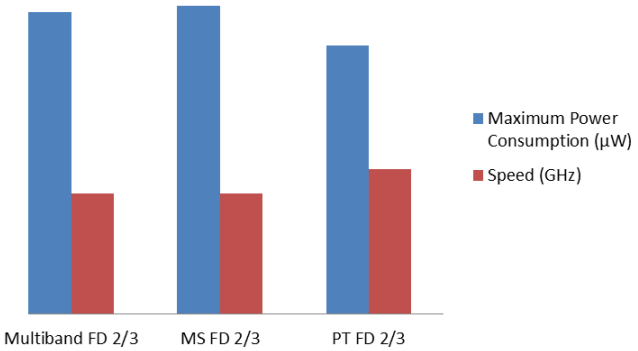

Fig 11. Comparison of FD 2/3 circuits

V. CONCLUSION

In this study, the concept of different methodologies has been discussed. When compared to the other techniques, this class of circuits uses slightly more transistors and indicates the advantages of power consumption. With 1.3V supply voltage, FD/2 circuit of TSPC logic requires less power consumption of 1.77 µW and FD 2/3 circuit of PT logic requires 5.57 µW when compared with other logics. The consumption of power

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and the voltage supply are reduced in this circuit defined. This circuit is coupled with PLL to perform as frequency synthesizers and also improved to increase the speed.

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