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Analysis of Drop Out and Load Current for on Chip Voltage Regulators

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Abstract. LDO (Low Drop-Out) Voltage regulators are commonly used in electronics power supply circuit. DC linear voltage regulator is a LDO regulator that can regulate the output voltage even when the power supply voltage is very near to the output voltage. This paper present a comparison between two of the most admired voltage regulator structures such as feed forward ripple cancellation technique and MOS capacitor compensation technique.The comparison has been carried out considering the output voltage, power consumption, drop-out voltage, load current, quiescent current, line regulation and load regulation. The discussion is supported by practical analysis of both the voltage regulator. The two LDO voltage regulators are taken with power supply voltage, reference voltage, error amplifier, pass transistor. The object of this paper is to compare the all the parameter of the voltage regulator to found best LDO voltage regulator structure. The comparison showed that the voltage regulator circuit with MOS capacitor compensation technique (MCC) is best rather than feed forward ripple cancellation technique (FFRC).All simulation and result of LDO voltage regulator is done at tanner tool 14.1.

Keywords: Low Drop-out(LDO), MOS capacitor, Pass transistor, Error amplifier, summing amplifier and ,feed-forward amplifier.

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1 INTRODUCTION

LDO voltage regulators are necessary building blocks in power-management systems. Power management systems for microprocessors and portable devices often use multiple LDO regulators to offer a regulated supply voltage with minimum
ripple to supply-noise-sensitive blocks [1].To raise battery-life and to achieve better power efficiency, low-dropout regulators are essential. LDO consists of a pass transistor, an error amplifier EA, a feedback network (RF1 and RF2) and a immense off chip capacitor . Various electronic equipments contains circuit which convert AC supply voltage into DC voltage at the preferred level. The DC voltage attained from such circuits must be stable. The DC voltage regulated power supplies are used to acquire the stable DC voltage yet there are variations in load current, temperature and AC line voltage. This power supply attenuates the ripple in the input voltage. The essential function of a voltage regulator is voltage regulation, provides clean, constant, accurate voltage to a circuit.

Regulator benefits:-

1. Accurate supply voltage
2. Active noise filtering
3. Protection from over current faults
4. Generation of multiple output voltages from single source
5. Inter-stage isolation

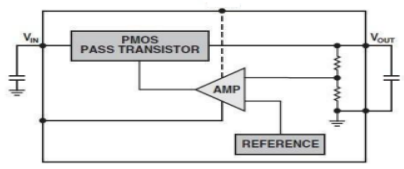

Fig 1: Block diagram of LDO Voltage Regulator [1]

LDO Architecture: - The architecture consists of following four parts:

1. Voltage Reference
2. Error Amplifier
3. Pass Transistor
4. Feedback Resistor

LDO be made of a voltage reference, an error amplifier, a feedback voltage divider and a pass transistor and load circuit. In this circuit, Output current is delivered through the pass device. Its gate voltage is restricted by the error amplifier which compares the reference voltage with the feedback voltage and also amplifying the differences so that reduce the error voltage.

2 IMPLEMENTATION OF LOW DROP-OUT VOLTAGE REGULATOR

2.1 FEED-FORWARD RIPPLE CANCELLATION TECHNIQUE[FFRC]

The Schematic of LDO structure is shown in fig 2. PMOS_1, PMOS_2, PMOS_3, NMOS_1 and NMOS_2 form first stage amplifier i.e. Feed-Forward Amplifier. PMOS_4, PMOS_5,PMOS_6, NMOS_3 and NMOS_4 form second stage amplifier called Summing Amplifier. At the third stage, PMOS_7, PMOS_8, PMOS_9, PMOS_10, NMOS_6 and NMOS_5 form Error Amplifier. PMOS_11 is the Power PMOSFET forming fourth stage. Diode connected transistor PMOS_12 and PMOS_13 form feedback resistive network. Resistor_9,Resistor_10 and Capacitor_4 are the load resistance and capacitance.Capacitor_1,Capacitor_2 and Capacitor_3 are required on-chip active MOS capacitances of LDO structure.

To eliminate input ripples from appearing at the output, a zero transfer gain is necessary from the input to the output. Hence, the gate-overdrive voltage is independent of input ripples, and as a result no ripple appears across the load. Supply ripples, appearing at the source of pass transistor Mp

, are reproduced at the gate of using Mp the feed-forward path.

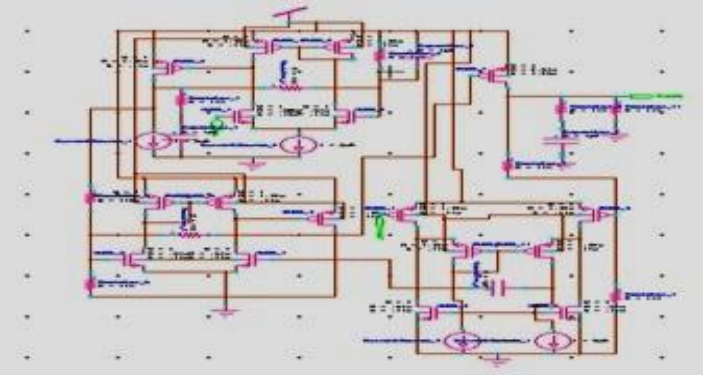

Fig 2: Schematic of LDO regulator using feedforward ripple cancellation technique

2.2 MOS CAPACITOR COMPENSATION TECHNIQUE [MCC]

The solution to control the damping factor and reduce the area of the compensation capacitor on chip, is the NMC technique with active capacitor and resistor; it is called an NMCACR LDO. In this technique, a capacitor is connected between the input differential stage and the output stage.

This LDO is composed of two gain stages, a power PMOS transistor and the feedback resistor network. First stage is the error amplifier (EA), second is a high gain stage. Capacitor_1, Capacitor_2 are the on-chip Active MOS capacitances. Resistor_1 and Resistor_3 construct the feedback resistive network. Resistor_2 and Capacitor_3 the equivalent load resistance and load capacitance at the power PMOS transistor.

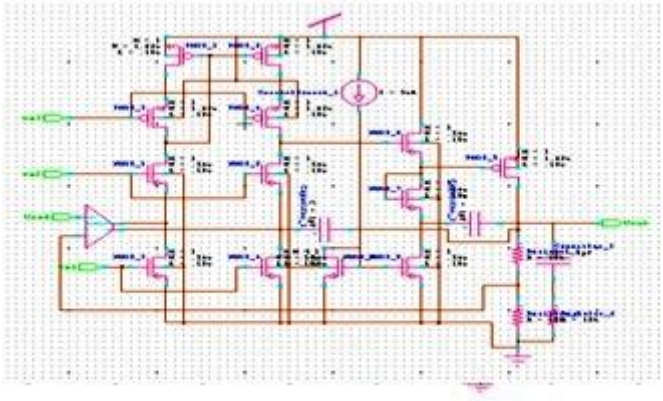

Fig3: Schematic of LDO regulator using MOS capacitor compensation technique

3 ANALYSIS AND COMPARISION OF LDO VOLTAGE REGULATOR

3.1 Feed-Forward Ripple Cancellation Technique

In LDO voltage regulator different types of parameters are consider :-

Load Regulation is the amount that the output voltage changes for a given change in load current. It can be improved by increasing the loop gain of LDO regulator which is constructed by gain of error amplifier and tranconductance of series pass transistor.

Line Regulation means the resistance of LDO against the variation of supply vol

tage.

Line Regulation = ΔVout/ΔVin

Quiescent current that a part draws from the source when idling (either shut down or not delivering significant amounts of load current) can be of critical importance in battery-powered applications.

Load Current is maximum current required in an application must be considered when selecting an IC regulator. The load current specification for an IC regulator be defined as either a single value or a value that is dependent on input-output voltage differential .

In Feed-Forward Ripple Cancellation Technique Voltage regulator at input 1.8V , the output is 1.7V. Therefore the Drop-out voltage is 0.1V which is shown in fig.4.

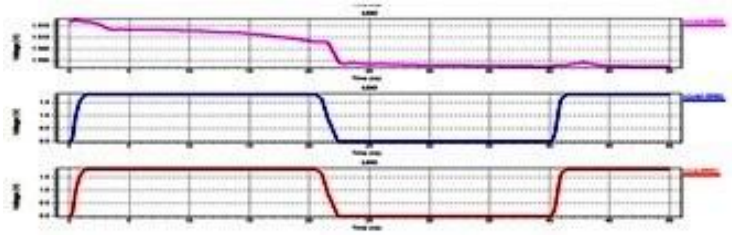

Fig4: Waveform of LDO voltage regulator using feed-forward ripple cancellation

Different types of parameters are calculated and listed below in table 1 & table 2.

TABLE 1.POWER, LOAD CURRENT AND QUIESCENT CURRENT AT DIFFERENT V_{DD}

S. No.	*Input(V)*	*Power Consumption(mw)*	*Load Current(μA)*	*Quiescent current(μA)*
1.	1.5	0.486	52	46
2.	1.8	0.623	72	78
3.	2	0.954	88	92

TABLE 2. OUTPUT, DROP-OUT VOLTAGE AND LOAD REGULATION AT DIFFERENT VDD

S. No.	Input(V)	Output(V)	Drop-out Voltage(V)	Load Regulation (V/mA)
1.	1.5	1.23	0.27	8.01
2.	1.8	1.52	0.28	7.00
3.	2	1.7	0.3	6.34

3.2 Mos Capacitor Compensation Technique

A full on-chip and area efficient low-dropout voltage regulator, which utilize the technique nested miller compensation with active capacitor (NMCAC) to eliminate the external capacitor without compromising the stability of the system in the full output current range.

 ISSN: 2454-4248
59 – 62

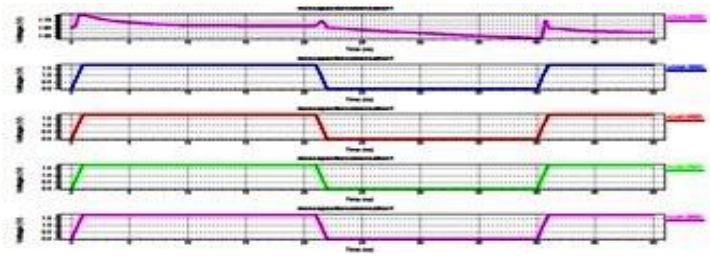

Fig5: waveform of LDO Voltage regulator using MOS Capacitor Compensation Technique

Its different parameters such as Power ,Load current, Quiescent current, Load regulation and Dropout voltage are calculated as listed below in table 3 & table 4.

TABLE 3. POWER, LOAD CURRENT AND QUIESCENT CURRENT AT DIFFERENT VDD

S. No.	Input (V)	Power Consumption (mw)	Load Current(µA)	Quiescent Current(µA)
1.	1.5	0.439	-47	127
2.	1.8	0.615	10	100
3.	2	0.928	20	95

TABLE 4. OUTPUT, DROP-OUT VOLTAGE AND LOAD REGULATION AT DIFFERENT VDD

S. No.	Input(V)	Output(V)	Drop-out Voltage(V)	Load Regulation (V/mA)
1.	1.5	1.45	0.05	3.68
2.	1.8	1.75	0.05	2.93
3.	2	1.95	0.05	1.56

4. COMPARISION OF LDO VOLTAGE REGULATOR USING DIFFERENT TECHNIQUE

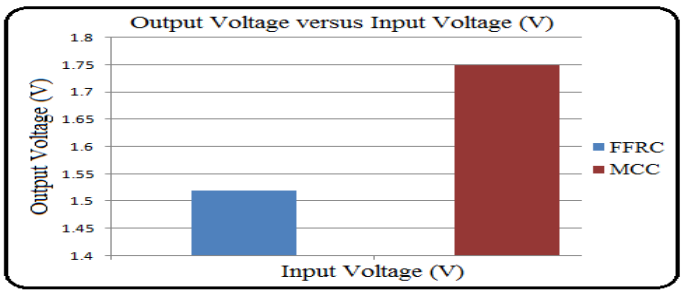

Fig6: Comparision of Output Voltage between FFRC & MCC

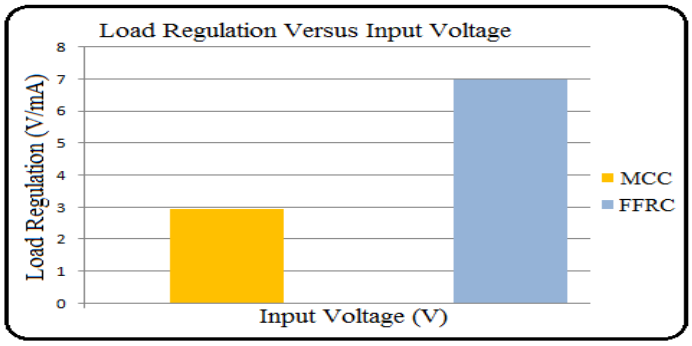

Fig7: Comparision of Load Regulation between FFRC&MCC

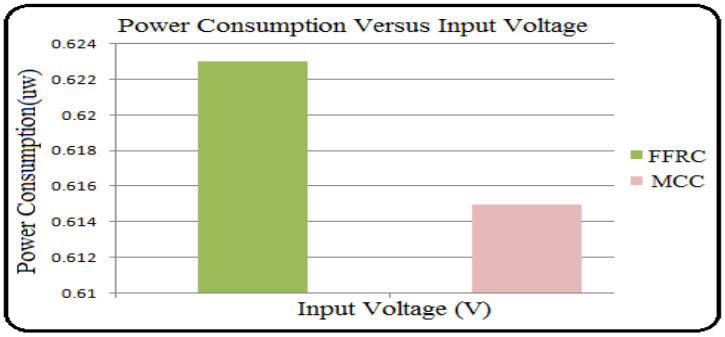

Fig8: Comparision of Power Consumption of FFRC&MCC.

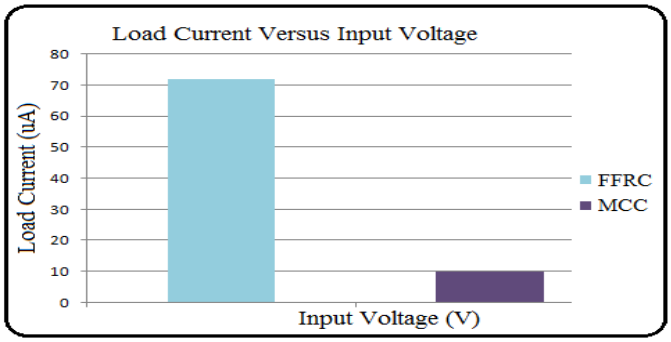

Fig9: Comparision of Load Current between FFRC&MCC.

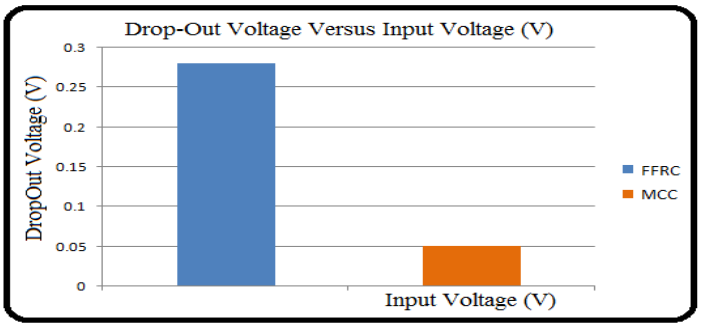

Fig.10: Comparision of Drop-Out Voltage between FFRC&MCC

 ISSN: 2454-4248
59 – 62

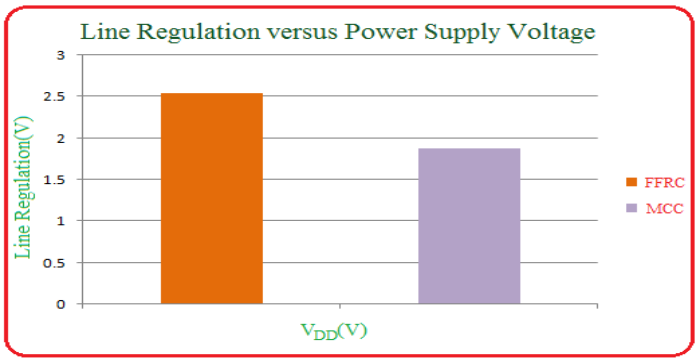

Fig11: Comparision of Line Regulation of FFRC&MCC

The performance comparison of voltage regulator table is shown below

TABLE 5. COMPARISON OF VOLTAGE REGULATOR WITH CONSTANT V_{IN}(1.8V)

S. No.	Parameters	Technique of Regulator	
		FFRC	***MCC***
1.	Output Voltage(V)	1.52	1.75
2.	Power consumption(µw)	0.623	0.615
3.	Load Current(uA)	72	10
4.	DropOut Voltage(V)	0.28	0.05
5.	Line Regulation(V)	2.5	1.8
6.	Load Regulation(V/mA)	7	2.93

5. CONCLUSION

In this work, experimental comparison between two of the low power, low drop-out voltage regulator structures was presented. The analytical description showed that the MOS Capacitor Compensation technique has an output voltage higher than the Feed-Forward Ripple Cancellation technique with power supply voltage 1.8V. The comparison result shows that the LDO voltage regulator with MCC technique provides improvements in terms of output voltage, drop-out voltage, power consumption, quiescent current, line regulation. Therefore we found that performance of LDO voltage regulator with MCC technique is best which provides clean, constant, accurate voltage to a circuit.

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