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Evaluation of Routes from Sources to Destinations in Fault- Free and Fault Scenarios

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INTRODUCTION: In this paper, the design and analysis of the proposed Fault-Tolerant Irregular Dynamic Modified Alpha Network has been presented. This network has been designed by reducing one stage of SEs in the existing Alpha Network. This makes the proposed network cost effective.

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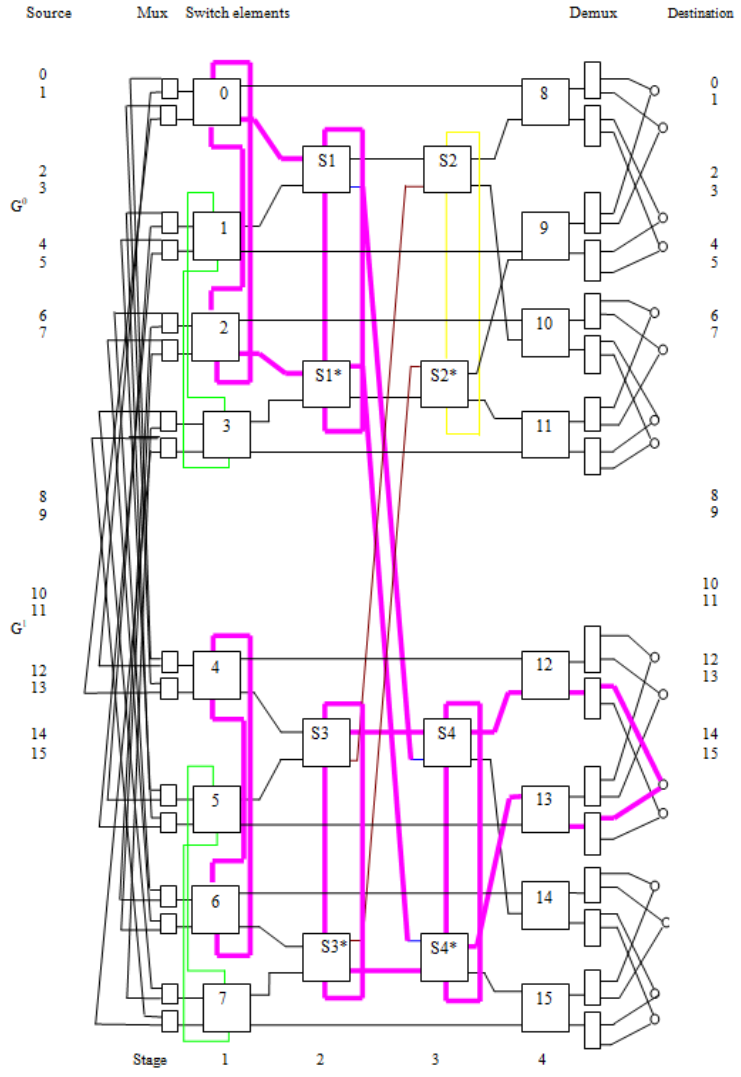
DESIGN OF Multiple Path MALN

The Network is an Irregular Multistage Interconnection Network, of size N*N. It has N sources and N destinations. The network Comprises of two identical groups of SEs, named as G^0 and G^1.Each group incorporates N/2 sources and N/2 destinations. Both the groups are connected to the N inputs through N multiplexers, and to the N outputs through N no. of demultiplexers. The modified Alpha network of size $2^n*2^n[n=\log_2 (N)]$,consists of (2m-2) stages where $m=\log_2 (N/2)$.This network has 2^n no. of switches of size 3*3 and 2^{n-1}no. of switches of size 2*2. Each source is connected to one SE in each group with the help of multiplexers. The switches in all the stages are of size 3*3 except the last one. The switches in the m-2 and m+1 stages have been named as 0,1,2,3----i, i=N-1. The switches in the stage m-1 have been named as S1, S1*,S3 and S3*. The names of the switches used in m stage are S2,S2*,S4 and S4*. The switches in the stages m-2,m-1 and m have been connected to each other through links called as auxiliary links and are called as complimentary switches. These links are used when the SE in the next stage is busy or faulty. This makes the network more Fault-Tolerant and reliable.

The network of size 16*16 is depicted in figure 1



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ROUTES FROM SOURCES TO DESTINATIONS IN FAULT- FREE AND FAULT SCENARIOS

Case 1:No Fault

The Table 1. shows the routes taken in routing the data from source to destination in fault-free condition in MALN.

Table 1: Routes from different source – destination pair in Fault-free MALN

Source-destination pair	Routes followed in the MIN to reach the destination							
(5,0)	5	MUX (5)	2	S1*	S2*	9	DEMUX (2)	0
(8,12)	8	MUX (8)	4	S3	S4	14	DEMUX (12)	12
(3,9)	3	MUX (11)	5	13	DEMUX (10)	9		
(4,10)	4	MUX (12)	6	S3*	S4*	13	DEMUX (11)	10
(0,0)	0	MUX (0)	0	8	DEMUX (0)	0		
(12,6)	12	MUX (4)	2	10	DEMUX (5)	6		
(6,4)	6	MUX (6)	3	11	DEMUX (7)	6		
(7,8)	7	MUX (15)	7	S3*	S4*	13	DEMUX (10)	8
(15,15)	15	MUX (15) MUX (7)	CLASH 3	S1*	S4*	15	DEMUX (15)	15
(1,2)	1	MUX (1)	0	S1	S2	8	DEMUX (1)	2
(11,13)	11	MUX (11) MUX (3)	CLASH 1	S1	S4 S4	14 S4*	CLASH 15	DEMUX (14)
(2,3)	2	MUX (2)	1	9	DEMUX (3)	3		
(9,7)	9	MUX (1) MUX (9)	CLASH 4 4	S3 6	CLASH S3*	S2*	10	DEMUX (5)
(13,11)	13	MUX (13)	6 6	S3 * 4	CLASH S3	S4	12	DEMUX (9)

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Case 2:Faults in switches S1, S2* and S3

The Table 2 shows the routes taken in routing the data from source to destination in MALN, under faults.

Table 2: Routes from different source – destination pair in MALN under faults

Source-destination pair	Routes followed to reach the destination in fault scenario in the MIN								
(2,3)	2	MUX (2)	1	9	DEMUX (3)	3			
(3,11)	3	MUX (11)	5	13	DEMUX (11)	11			
(12,14)	12	MUX (12)	6	14	DEMUX (13)	14			
(6,4)	6	MUX (6)	3	11	DEMUX (6)	4			
(9,3)	9	MUX (1)	0	8	DEMUX (1)	3			
(10,0)	10	MUX (10)	5 5	S3 7	FAULT S3*	S2	8	DEMUX (0)	0
(7,4)	7	MUX (7) MUX (15)	3 7	S1* S1* S3*	S2* S1 S2	FAULT FAULT 10	DEMUX (4)	4	
(5,2)	5	MUX (5)	2	S1*	S2*	CLASH			
			S1*		S1	FAULT			
			REQUEST DROPPED						
			5	MUX (13)	6	S3*	S2*		
FAULT									
						S3*	S3		
FAULT									
					6	4	S3		
FAULT									
(0,7)	0	MUX (0)	0	2	10	3(5)	7		
(8,7)	8	MUX (0) MUX (8)	CLASH 4 4	S3 6	FAULT S3*	S2*	FAULT **REQUEST DROPPED**		

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Conclusion

There are multiple routes available from source to multiple destinations in case of faults. This makes the MALN Fault tolerant Network of course with degraded performance.

References

[1] 1.Shen J. P., August 1982, "Fault-Tolerance Analysis of Several Interconnection Networks", Proceedings International. Conference on Parallel Processing, pp. 102-112

[2] 2. Siegel H. J., 1985, "*Interconnection Networks for Large Scale Parallel Processing: Theory and Case Studies"*, Lexington, M.A.: Lexington Books.

[3] Somani Arun K., Vaidya Nitin H., April 1997, "Understanding Fault-Tolerant and Reliability," IEEE Computer, Theme Issue, **30**.

[4] Tripathi V. S., Tripathi C. B., Tiwari S., July 2006, "Performance evaluation of a Fault-Tolerant Switch for the Next Generation Computer Networks", Proceedings of the 12th International Conference on Parallel and Distributed Systems (ICPADS).