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An Effective Low Power Ring Oscillator Based All Digital Phase Locked Loop

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***Abstract* —** The All digital phase-locked loops (ADPLL) widely employed in the data communication systems including, but not limited to, the implementation of the frequency multiplication and clock synchronization circuits. A phase-interpolator is utilized for power consumption reduction by using TDC in a ring-oscillator in a fractional-N phase-locked loop. A predicted-phase-interpolation method is used to calculate the integer and fractional parts of the frequency-division-ratio and to find two interpolation clocks. The prediction method gives a significant power reduction in the proposed PIFC by enabling the use of low-frequency clocks for phase interpolation

***Keywords* -** *Time to Digital Convertor (TDC), All Digital Phase Locked Loop (ADPLL), Phase –Interpolator based Fractional counter (PIFC), Predicted-Phase- interpolation.*

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I. INTRODUCTION

Phase-locked loops are widely used in advance electronic circuits, Data communication systems as a clock and data recovery, modulation and frequency synthesis, etc... The conventional PLLs consist of analog phase and frequency detector, charge pumps, analog loop filters (LFs) and voltage controlled oscillators (VCOs). Even though, Analog PLLs is giving good locking range and wide operating frequency still it gives problems like PVT variations, redesign problem , more area utilization etc. Due to the technical improvement and new innovation ideas now we have All digital PLL(ADPLL). ADPLL consist of full digital components and it solved the problems occur in DPLL and Analog PLL. The advantages of a digital implementation are the inherent noise immunity of digital circuits, good scalability and easy redesign. Nowadays the designer avoiding the percentage of analog circuitry so that redesign time is improving.

A phase-lock loop is essentially a negative feedback loop in which the phase of the frequency controlled oscillator should lock with that of the incoming signal. Phase error will be created in the Unlock state.

ADPLL have become more attractive because of its wide frequency range, low power consumption, good testability, stability, and portability over difference process. Bang bang phase detector gives good robustness and low power consumption [13]. Frequency locking time is time between initialization of ADPLL and the frequency locking [14].There are two major issues needed to be considered. 1. Design a Digitally-Controlled Oscillator with wide tuning range and high resolution. 2. Design with less lock in time.

The paper is organised as follows Section II covers proposed method of ADPLL and section III covers result analysis and in section IV conclusion is presented.

II. PROPOSED SYSTEM

The proposed ADPLL consist of D-flip flop based phase detector, counter, digital lop filter and Ring based digital oscillator. F_{REF} represents frequency of reference signal and F_{OUT} represents the frequency of ring oscillator frequency.

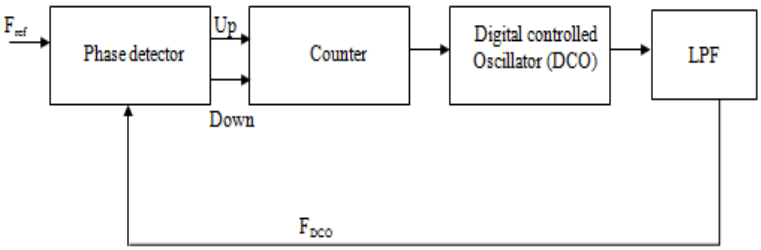

Figure 1. Proposed Block Diagram

Phase detector generates shift right or shift left without considering of the frequency difference between F_{REF} and F_{OUT}. As a result, a frequency divider block is not needed in this ADPLL. The delay element of the detector governs the final phase difference.. Generating shift left or shift right once every two cycles of the reference clock provides stability.

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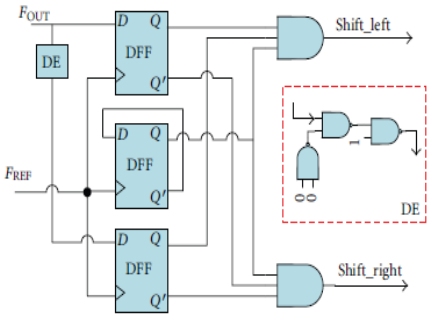

Figure 2. Phase Detector

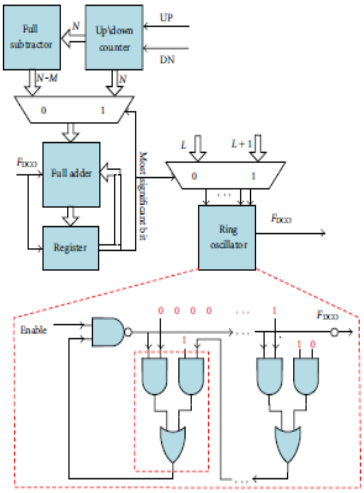

Figure 3. Digitally Controlled Oscillator (DCO)

Digitally Controlled Oscillator (DCO) is the frequency generating block in ADPLL. The frequency of DCO is adjusted for achieving frequency and phase locking. It is used to generate multiples of the frequency. It consists of ring oscillator and fractional divider. The ring oscillator consists of one NAND gate for enabling/disabling the oscillation and a combination of AND OR delay elements. The ring oscillator produces a clock signal (FOSC) whose frequency is proportional to the number of the delay elements in the ring. The FOSC signal must go through each of the delay elements twice to provide one period of oscillation. The number of delay elements and ring oscillator are inversely proportional.

The fractional divider consists of an adder accumulator. The MSB of the accumulator signed register is used to switch the input of the adder between signed integer number N and its two's complement N-M. It is also used to switch between two adjacent ring oscillator chain lengths, (L1) and (L2).

The F_{OSC} is given by

$$F_{osc} = 1/2L\ t_{de} \text{ ----------2/1}$$

where t_{de} is the time delay for each delay element and L is the chain length that is defined by a one-hot coded control word.

Accordingly, switching between two adjacent chain lengths $L1$and$L2$ provides on average fine frequency resolution.

Frequency stability is normally achieved by designing a stable and fast controller based DCO, whereas a high frequency resolution is achieved by increasing the number of bits of the accumulator signed register.

III. RESULTS AND DISCUSSIONS

(a) Schematic Results for Phase Detector

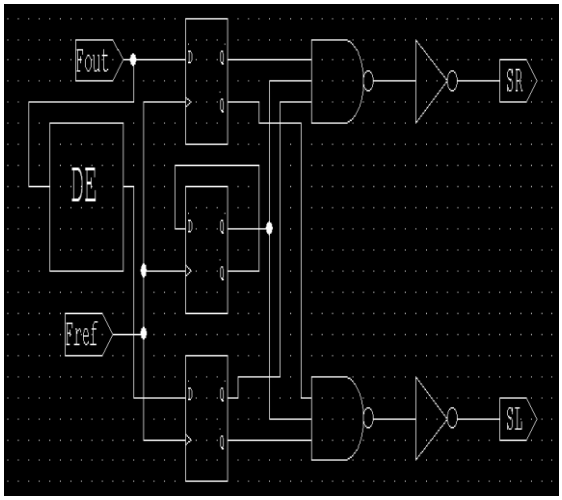

Figure 3.1 Schematic Results for Phase Detector

(b) Simulation Results for Phase Detector

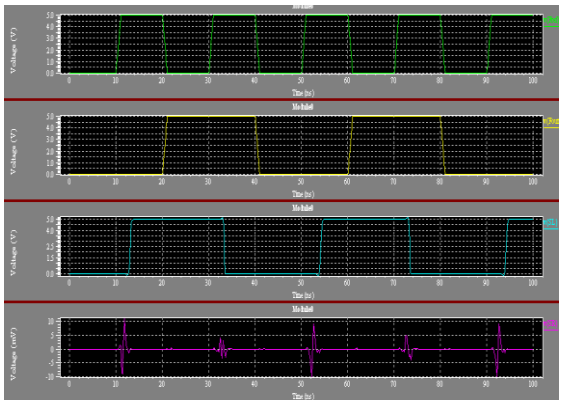

Figure 3.2 Simulation Results for Phase Detector

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(c) Schematic Results for Ring Oscillator

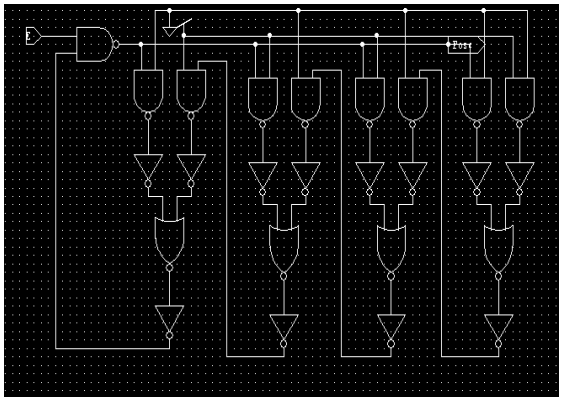

Figure 3.3 Schematic Results for Ring Oscillator

(D) Simulation Results for Ring Oscillator

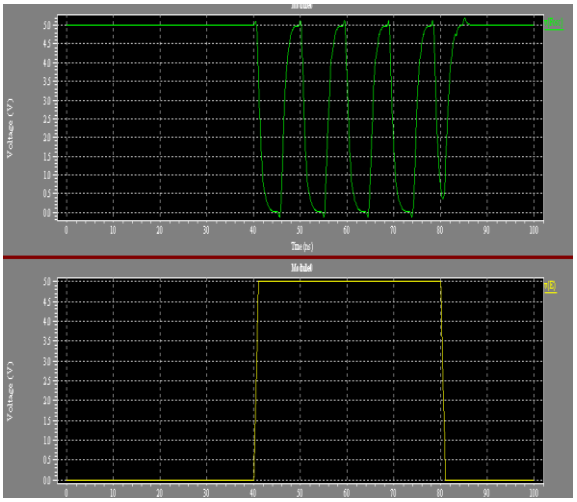

Figure 3.4 Simulation Results for Ring Oscillator

(E) Schematic Results for ADPLL

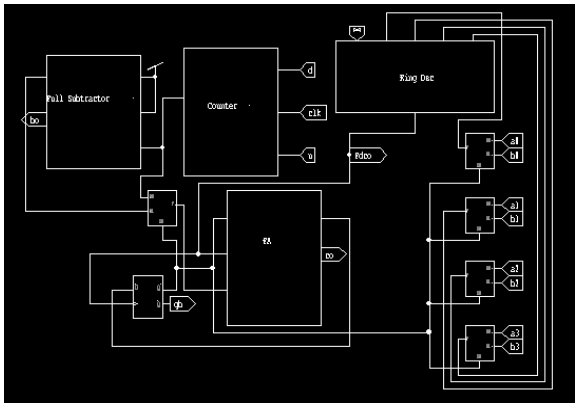

Figure 3.5 Schematic Results for ADPLL

(F) Simulation Result for ADPLL

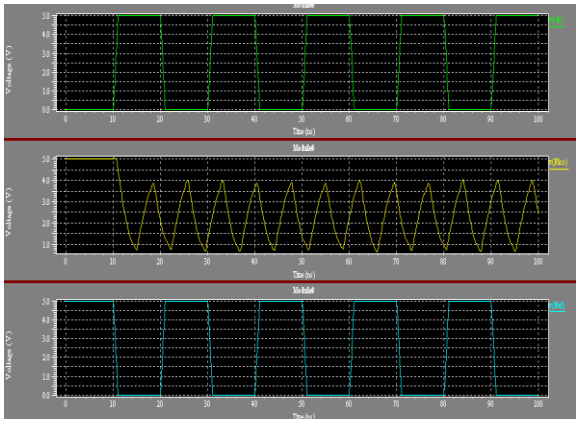

Figure 3.6 Schematic Results for ADPLL

The ADPLL power consumption is 0.31mW and the frequency is 142 MHz

IV. CONCLUSIONS

Thus, the ADPLL designed with D flip flop based phase detector, digital loop filter and ring based DCO. D flipflop based phase detector utilize low power consumption and utilize low area. The ring oscillator is preferred because of its low power consumption and its ability of delay stages extension. Frequency divider is not required in the block The ADPLL is designed with low power utilization, low chip area and the system gives good locking range and frequency resolution.

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