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Energy Efficient Power Management Protocol For Hierarchical Wireless Sensor Network Employing Artificial Intelligence & Dual Stack Sleep Mode

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Abstract—Wireless sensor networks are becoming an integral part of household & industrial technology, & the usage & acceptance expected to rise dramatically with the advent of IOT. Thus we need of the highly energy efficient, wireless sensor network for data collection. Our proposed system is a hierarchical architecture wireless senor network based on tree topology along with dynamic energy saving techniques. In this paper Artificial intelligence based transmitter power variation by estimation of distance is employed to save battery power while data is transmitted. Also, to save energy during sleep circuitry has been devised, dual stack design sleep power consumption are verified using tanner tools, the entire hierarchical WSN is modelled & tested using MATLAB.

Keywords—*Hierarchical WSN, energy efficient WSN, dual sleep, dual stack, artificial intelligence.*

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I. INTRODUCTION

Wireless sensor network (WSN) expressed of three words. Wireless means the communication take place without wires. Sensors are tiny devices that sense any physical quantity and convert that quantity in to electrical signals. The word network means by which sensors can communicate among them. [1]

Wireless sensor network (WSN) can be characterized as a remote system to screen physical or ecological conditions, for example, temperature, sound, vibration, wind speed, moistness and so forth.

Before wireless sensor networks were intended for military applications (front line reconnaissance, question assurance, smart directing, remote sensing and so forth.) however presently it is additionally use in environment condition, wellbeing, home, space investigation, chemical processing and other business regions. [1]

Wireless sensor networks are spatially circulated self-ruling sensors those supervise physical or ecological conditions, for example, temperature, sound, pressure, and so on., and facilitate their information to an essential area over a system. More present day systems are two-way and can likewise control sensor movement. The advancement of wireless sensor networks is driven by military applications, for example, battlefield surveillance; today, such systems are utilized in numerous mechanical and customer applications, for example, industrial process monitoring and control, and machine wellbeing observing. [2]

Till now various techniques were proposed on wireless sensor networks several authors developed different techniques some of them are explained in this section.

T. et al. suggested the energy proficient condition observing station and information gathering system which depended on pervasive wireless sensor networks utilizing solar cell was proposed. Additionally they likewise connected, the progressed WSN and GPRS/3G technology for information gathering, and transmission, various issues of ongoing checking and inclusion zone can be settled and by utilizing sun powered power supply with high limit lead-acid battery, issue of energy consumption has been additionally overcome. [2]

M. et al. described that the energy conservation potential supported analysis with actual device platforms. Introduced two cases wherever authors planned see information gathering in installed, wireless networks as vast information applications. in the first case we habit to see device networks with a large node thickness all together that the blend of the device information gathered by each node is huge. Also, in the second case manages systems with high node complexness, (for example, vehicles) wherever every individual node holds an big number of device data and consequences.[3]

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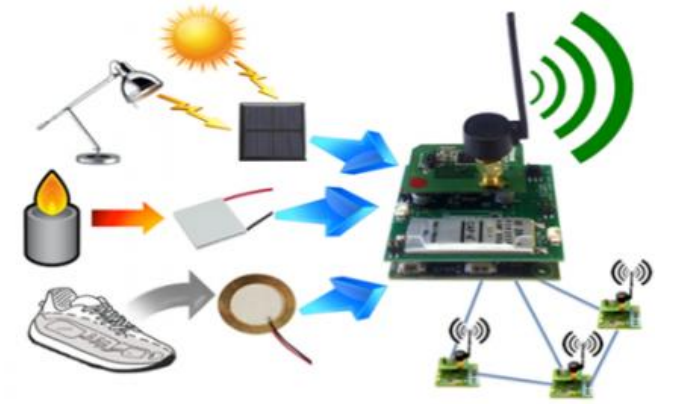

Fig 1.1: Wireless Sensor Network

II. BACKGROUND

The fundamental of the wireless sensor networks that we have used in our research proposal. This section describes the various techniques that are used to save energy.

A. Dual Stack

A dual stack network includes nodes which are fit for handling IPv4 and IPv6traffic at the same time. At the point when a node in a dual stack network gets traffic, it is customized to lean toward the IPv6 over IPv4 traffic. Dual stack operation means using IPv6 side by side the current IPv4 implementation. Dual stack can be used as transition to IPv6 only. Dual stack provides full reachable for both address families.

B. Artificial Neural Networks

In electronics engineering and associated fields, artificial neural networks (ANNs) are numerical or computational models that are roused by a human's focal nervous system (specifically the mind) or, in other words machine learning and also design acknowledgment. Artificial neural networks are exhibited as frameworks of exceptionally interconnected "neurons" which can be process values from the information sources. Neural Network is much the same as a system of interconnected neurons which can be many more. With the assistance of these interconnected neurons all the parallel preparing is being done in body and the best case of Parallel Processing is human or animal's body. Presently, artificial neural networks are the grouping of the basic artificial neurons. [9] This is happens by making layers which are associated with each other. So neural systems, with their more grounded capacity to get significance from convoluted or false information, can be utilized to separate patterns and recognize complex things that are seen by either people or other computer methods.

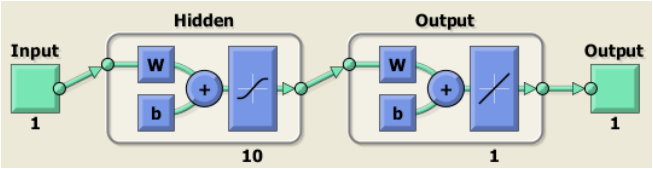

Fig 1.2: Curve Fitting Neural Network

C. Dual Stack Sleep Technique

Technique for leakage strength rebate is the stack approach, which powers a stack affect by utilizing separating a present transistor into two 1/2 length transistors . The partitioned transistor NMOS blast put off altogether. The sleepy stack technique consolidates the sleep and stack approach. The sleepy stack method separates current transistor NMOS into two 1/2 length transistors simply like the stack approach. At that point sleep transistors are included parallel to one of the isolated transistors. Amid sleep mode, sleep transistors are turned off and stacked transistors stifle spillage current while saving state. Each sleep transistor, set in parallel to the one of the stacked transistors, diminishes obstruction of the way, so delay is decreased amid active mode. In any case, territory punishment in NMOS is a noteworthy issue for this methodology. When each transistor is supplanted by three transistors and extra wires are included for S and S', which are sleep Signals. This Technique utilizes the benefit of utilizing the two additional Pull-up and two additional pull-down NMOS and PMOS transistor which works in sleep mode either in OFF state or in ON state.

III. PROPOSED METHODOLOGY

This section discusses the proposed methodology in contrast with existing techniques.

A. wireless Node – General Configuration

Firstly the Environment sensors are coordinated with wireless hardware and wireless hardware is controlled by MSP430 MCU and transmission by CC1120 transceiver. This component is abided by control supply. Fig.1.3 describe the sensor node block diagram. In our existing methodology power supply circuitry is directly connected with sensor nodes due to which in sleep mode these sensors consumed power supply so to overcome this problem we proposed dual stack sleep controller circuit between power supply circuit and sensor nodes. This prevents the power consumption during sleep mode.

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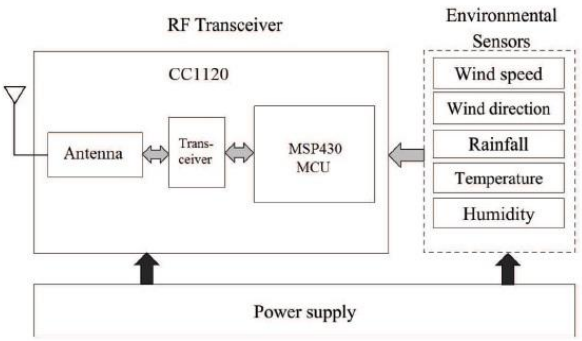

Fig 1.3: wireless Node – General Configuration [2]

B. Wireless Node with dual stack controller

Condition sensors are coordinated with wireless hardware which under the control of MCU and transmission by transceiver. This part is additionally comprises power supply with dual stack sleep controller the sleepy stack procedure separates existing transistor into two half Size transistors like the stack technique. At that point sleep transistors are included parallel to one of the isolated transistors. Amid sleep mode, sleep transistors are turned off and stacked transistors contain leakage current while saving condition. Each sleep transistor, put in parallel to the one of the stacked transistors, lessens obstruction of the way, so delay is diminished amid active mode. When each transistor is supplanted by three transistors and extra wires are included for. Fig.1.4 defines the sensor node block diagram.

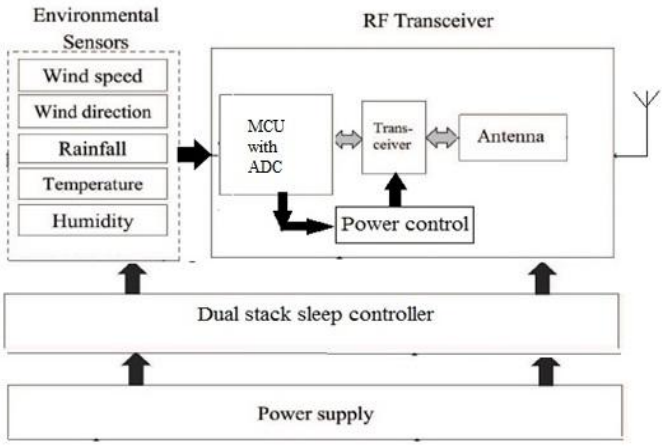

Fig 1.4: wireless Node with dual stack controller

C. Dual Stack Tanner Implementation

- *XOR with Sleep:*

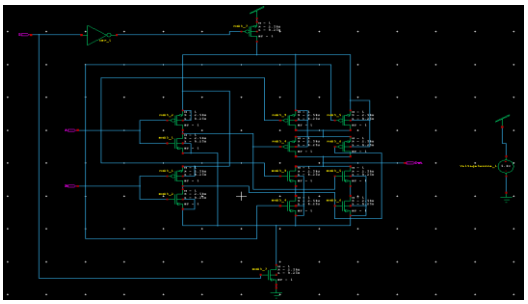

Fig 1.5: XOR with Sleep

- *XOR with Dual Stack:*

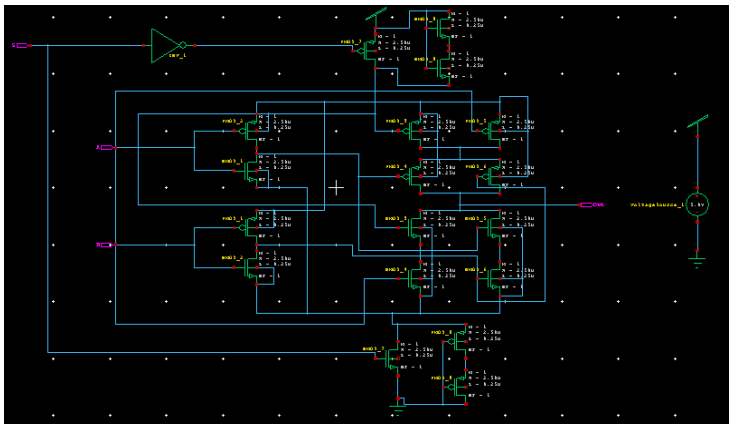

Fig 1.6: XOR with Dual Stack

IV. Experiments and Results

This section discusses the various experimental results and graphs that were carried out during our research. Which includes tanner results, graph with dual stack sleep and without sleep graph.

Tanner Results:

A. Without Sleep Graph:

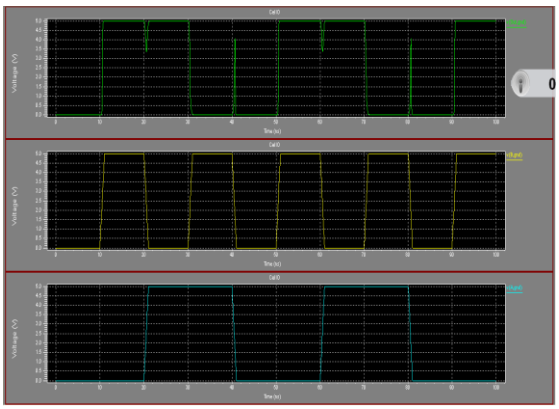

Fig 1.7: Without Sleep Graph

When, calculated the without sleep mode power in non-graphical representation then power consumed by it 4.99 watts around.

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```
* BEGIN NON-GRAPHICAL DATA

Power Results
VVoltageSource_1 from time 0 to 1e-007
Average power consumed -> 4.941021e-004 watts
Max power 1.967737e-002 at time 4.07209e-008
Min power 8.482002e-011 at time 9.825e-009


* END NON-GRAPHICAL DATA
*

* Parsing                          0.02 seconds
* Setup                            0.01 seconds
* DC operating point               0.00 seconds
* Transient Analysis               0.14 seconds
* Overhead                         1.78 seconds
* ----------------------------------------------
* Total                            1.95 seconds

* Simulation completed  with 1 Warning
```

Fig 1.8: Non Graphical Data Presentation

B. With Dual Stack Sleep:

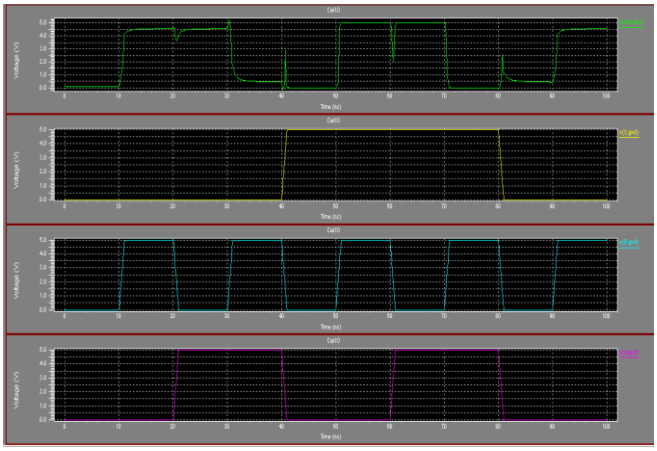

Fig 1.9: Dual Stack Sleep

When, we calculated stack dual sleep in non-graphical mode then power consumed is 2.47 around according to our proposed system.

```
* BEGIN NON-GRAPHICAL DATA

Power Results
VVoltageSource_1 from time 0 to 1e-007
Average power consumed -> 2.472885e-004 watts
Max power 1.659268e-002 at time 8.0556e-008
Min power 6.479430e-010 at time 1e-008


* END NON-GRAPHICAL DATA
*

* Parsing                          0.02 seconds
* Setup                            0.03 seconds
* DC operating point               0.02 seconds
* Transient Analysis               0.28 seconds
* Overhead                         1.56 seconds
* ----------------------------------------------
* Total                            1.91 seconds

* Simulation completed  with 7 Warnings

* End of T-Spice output file
```

Fig 1.10: Graphical Data Presentation

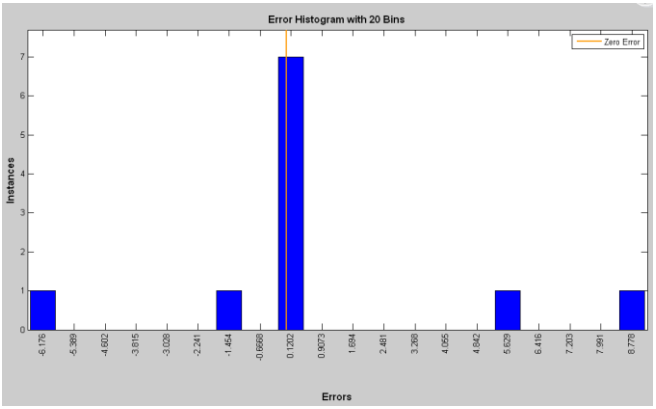

Fig 1.11: Error Histogram Graph

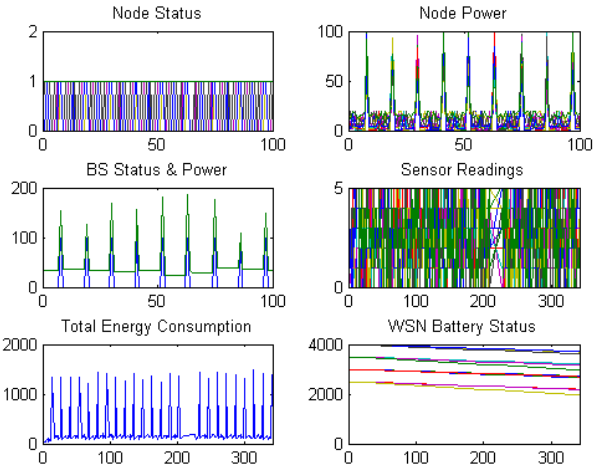

Fig 1.12: Graphical presentation of BS status & power, Node Power, Node Status, Sensor Reading, Total Energy Consumption, WSN Battery Status. With Respect to time

CONCLUSION AND FUTURE SCOPE

In this design, the energy efficient design of a hierarchical WSN is presented. High level energy efficiency is achieved by estimation of transmitter power required for a node by using artificial neural network & node distance as an input, this helps in optimizing the radio power slightly higher than sufficient for reception at that distance, & thus conserved energy by not operating the transmitter at full power, as most of the power consumed by a WSN is in transmit phase, this move, greatly enhance the energy efficiency & thus battery life of the sensor node. Also, apart from maximum power consumption during transmit phase, most of the time i.e. 90% of its deployment, a WSN remains in sleep, & a reduction in sleep leakage power by employing dual stack technique has improved energy efficiency abundantly. Thus the proposed system by employing a hierarchical architecture & amp power management technique via AI based radio power optimization & sleep leakage current reduction using dual stack, proves to be highly energy efficient, & which is demonstrated in the results above. A leakage power reduction of 0.2469 MW and the correspond percentage is

49.96% as compared to normal sleep architecture is a based for a dual stack technique, also total energy consumption reduction of WSN nodes is reduced by 52.495.

The proposed system as depicted has shown improvement in energy efficiency of wireless sensor network to concededly increase the battery life of WSN systems. As wireless sensor nodes & IOT are not in main system commercial implementations, & are the current buzzword, there is a lot to be improvement in exiting technology before real time massive deployment. One of the most sought improvisations is integration of energy harvesting devices with the WSN nodes, so they may catch pure energy from nature to charge energy from nature the charge of the batteries. Another important advancement sought is in improving energy density of batteries & improvement their life span & reducing their cost, one such advancement, WSN may be employment of super capacities instead of batteries in conjunction with energy management & central protocols will need to evolve with this purgation of technology to provides us next generation, battery less self-charging, wireless sensor and central nodes.

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