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Design of Static Segment Adder for Approximating Computing Applications

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***Abstract*—** The digital VLSI design needs to attain high performance with desired reliability range. The high performance involves low power, area efficiency and high speed. This paper proposes a design of High speed energy efficient static segment adder (SSA) to enhance the overall performance based on approximation technique. Static segmentation includes both accurate and inaccurate part. The normal full adder performs accurate part and the carry select adder is used for inaccurate part. By using static segmentation the approximate computation is done. Approximate computing is a computation which generates "good enough" result rather than totally accurate result. Image processing is accomplished using SSA design. In this process 99.4% whole computational accuracy for 16 bit addition and also for 8 bit addition can be achieved.

Keywords- *Static segment adder, Carry select adder (CSLA), Ripple carry adder (RCA), Reconfigurable Error Tolerant Carry Look-Ahead adder (RET-CLA).*

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I. INTRODUCTION

In general power consumption and performance are critical parameters in the design of digital circuit. In digital signal processing the circuit is implemented for filtering, encryption or time to frequency or frequency to time domain transformations. Adders are the major building blocks in Arithmetic and logic unit (ALU).Since addition is often implemented as a main-function within larger systems, its speed becomes a critical factor limiting the overall system performance. Thus, special care must be taken when selecting and designing the adder configuration to be used [1]. In the design of Integrated Circuits, area occupancy plays a vital role because of increasing the necessity of portable systems. Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions [2].

The normal adders are too slow or consume more energy then the implementation of the design will be degraded. In Reconfigurable Error Tolerant Carry Look-Ahead adder (RET-CLA) the LSB Part is designed to produce approximate result [3]. Similarly the most of the DSP blocks implement image and video processing algorithms, where the ultimate output is either an image or a video for human consumption. The limited perception of human vision allows the outputs of these algorithms to be numerically approximate rather than accurate. Approximate addition has been carried out as a means of achieving area, power and speed improvement [4].Many applications are not error tolerable. The incorrect result generated by speculation will result in incorrect final result. For applications where errors cannot be tolerated, a reliable variable latency adder can be built upon the SCSA-based speculative adder by adding error detection and recovery, called variable latency carry selection adder (VLCSA) [5]-[11].

In this work an accuracy improvement static segment approximate technique is used based on the significance probability by invalidating lower order bytes of input information to achieve the required computational accuracy for human perception interfaced application is proposed. The recommended design is incorporated with spatial domain image amplification technique, which operates directly on pixels and gives a quantitative measure for human perception. The rest of the paper is organized as follows. In section II, some of the related works are reviewed and in section III, the proposed system is described. In section IV, the algorithm of static segment adder is explained and in section v, the architecture of static segment adder is detailed. In section VI the accurate and inaccurate part is compared. In section VII the carry select adder is described and in section VIII the ripple carry adder is detailed. The software simulation is explained in section IX and the standard test images are listed in section X. In Section XI the hardware implementation is detailed and the design parameters are discussed in section XII. Finally the paper is concluded in section XIII.

II. EXISTING SYSTEM

An Important problem of computer hardware involves the design of a fast parallel adder to minimize the effect of the worst case carry propagation. To reduce carry propagation the carry skip adder is used [1].The existing modified SQRT CSLA uses Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower delay with slightly increase in area. The basic idea of the proposed architecture is that which replaces the BEC logic by Common Boolean Logic. The proposed architecture generates a duplicate sum and carry-out signal by using NOT and OR gate and select value with the help of multiplexer. The multiplexer is used to select the correct output according to its previously carry-out signal [12]-[15].

The related work consists of full adder which consumes more energy, area, power etc. The image processing application using adders used in wide range of application like image encryption, image mixing, image compressing etc. Full adders are used in this process which consumes less power, too fast, less area and more energy efficient. The traditional ripple carry adder is therefore no longer suitable for large adders because of its low speed performance. Many different types of fast adders, such as the carry skip adder, carry select adder and carry look ahead adder have been developed.

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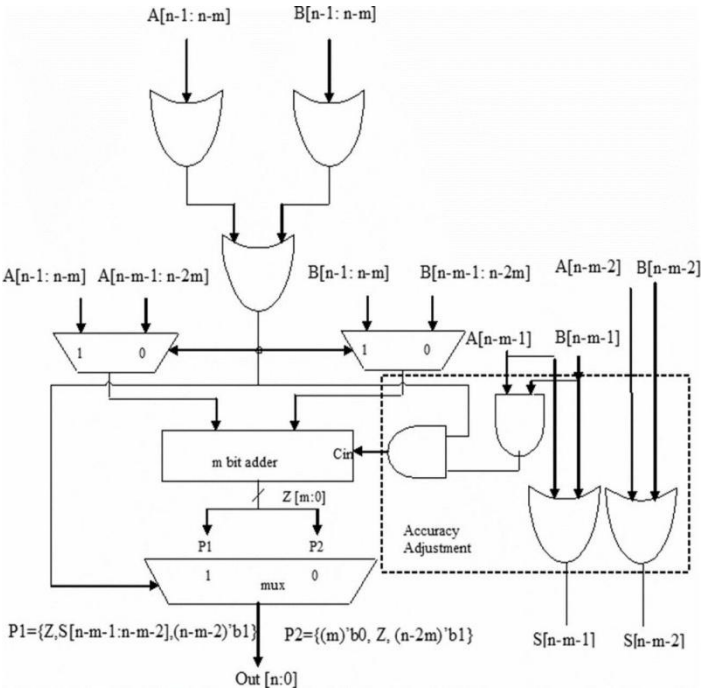

Figure 1 Architecture of static segment adder (SSA)

III. Proposed System

This proposed system includes a design of high speed energy efficient static segment adder which enhance the whole performance based on static segmentation. Accuracy Adjustment logic is incorporated to improve the accuracy derived from invalidating lower order bytes of input operands. To achieve computational Accuracy for error tolerant applications an integration of static segmentation method and Accuracy Adjustment logic is used. The proposed adder design enables to provide high speed and energy efficient through the static segmentation method.

IV. Algorithm of static Segmentation Adder

Step 1: Select m-bit (say8-bit) segment from augend and addend n-bit input (say 16- bit) operands
Step 2: This Segment must contain the leading one bit
Step 3: Select the higher order leading one m-bit position (say8- bit) segment from augend or addend n-bit operands
Step 4: Select the same m-bit position (say 8-bit) segment from augend or addend n-bit operands
Step 5: Add the set of m-bit segments with accuracy adjustment estimator logic carry
Step 6: Expand the m-bit addition to n-it addition

V. Architecture of Static Segment Adder(SSA)

In this architecture (n=2m) the bit-wise OR value of A [n–1: n-m] and B [n–1: n-m] is computed to select the two possible m-bit segments (i.e., (A [n–1: n–m] and B [n–1: n–m]) or (A [n-m–1: n-2 m] and B [n- m–1: n-2 m])). Accuracy adjustment logic is enabled for higher order segment selection of input operands to increase the accuracy by selecting the P1 in the output. When the lower order segment is selected SSA works as a conventional adder to in maintain the accuracy as 100%, the propagation carry from the AAL is zero and P2 is selected the output.

VI. Accurate and Inaccurate Comparison

In the static segmentation adder, the accurate part consists of full adder were carry and sum is as same as normal full adder and in the inaccurate part the sum is complement of carry.

VII. Carry Select Adder

The carry-select adder is the fastest adder and used in many data processing operations. It uses two ripple carry adders and multiplexer Two 4-bit ripple carry adders are multiplexed together, where the resulting carry and sum bits are selected by the carry-in. Since one ripple carry adder assumes a carry-in of 0, and the other assumes a carry-in of 1, selecting which adder had the correct assumption via the

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actual carry-in yields the desired result. The basic block diagram of carry select adder is shown in figure 2.

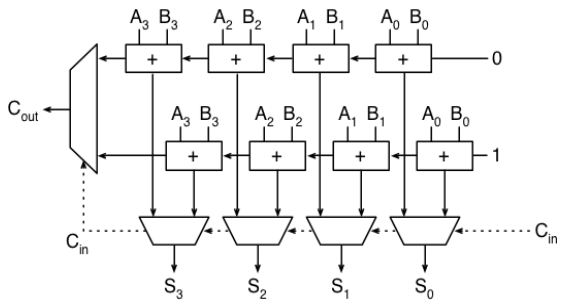

Figure 2 Carry Select Adder

VIII. Ripple Carry Adder

It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry are the reason behind this. Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output. Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder.

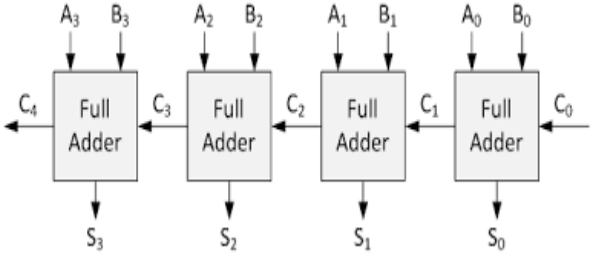

Figure 3 Ripple Carry Adder

Sum out S_0 and carry out C_{out} of the Full Adder 1 is valid only after the propagation delay of Full Adder 1. In the same way, sum out S_3 of the Full Adder 4 is valid only after the joint propagation delays of Full Adder 1 to Full Adder 4. In simple words, the final result of the ripple carry adder is valid only after the joint propagation delays of all full adder circuits inside it. The block diagram is shown in figure 3.

IX. Software Simulation

XilinxISE (Integrated Synthesis Environment) is a software tool produced by Xilinx. It is used for the synthesis and analysis of proposed and existing system. Image enhancement operation is processed using proposed SSA by using the integration of MATLAB Simulink and Xilinx software. The input and output images are shown in figure. The input image has the pixel size of (256 × 256). Verilog code is used to construct user defined Xilinx black box adders and integrated with predefined modules. Normalization operation is performed in MATLAB Simulink using proposed SSA and existing adders by varying multiplication factor to gain the high accuracy images for low contrast and high contrast images. The Xilinx block for overall part is shown in figure 4.

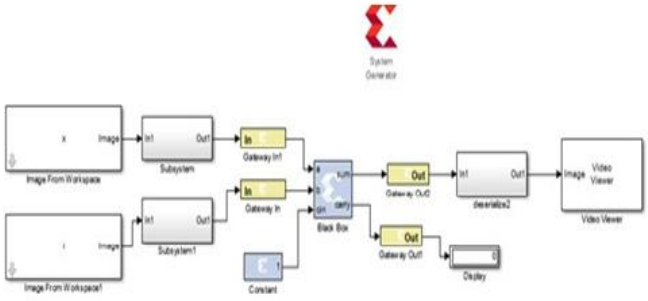

Figure 4 Xilinx block

Figure 5 Input image 1

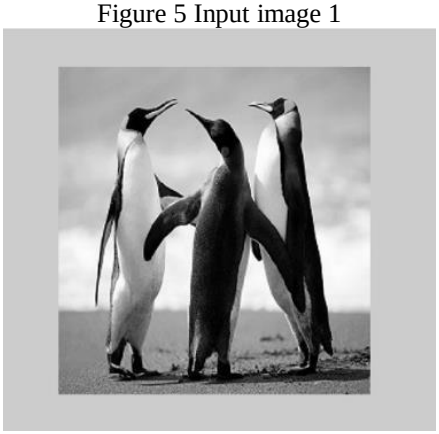

Figure 6 Input image 2

Figure 7 0utput Image

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X. STANDARD TEST IMAGES

The standard test images viz., Lena, pepper, baboon, boat and bridge which are commonly used for evaluating the performance of the de-noising algorithms in the Figure 8.

All test images taken for testing are 8-bit gray scale images of size 512x512, which are commonly used for image denoising.

a)Lena b) Pepper c) Bridge d) cameraman

Figure 8 Standard test images

XI. HARDWARE IMPLEMENTATION

Step 1: The proposed static segment adder is implemented in Atlys Spartan 6 FPGA kit.
Step 2: It is a complete, ready to use digital circuit board and is compatible with all Xilinx CAD tool.
Step 3: The implementation is done for 16 bit addition in which two 16 bit inputs 1 and 2 are given.
Step 4: The different input carry such as 1 or 0 is given and the resultant 16 bit output for static segment adder is seen.
Step 5: The output is verified in the system after processing in the FPGA kit.
Step 6: The performance of both carry select and ripple carry adders are tested. The Xilinx block for hardware simulation is shown in figure 9.

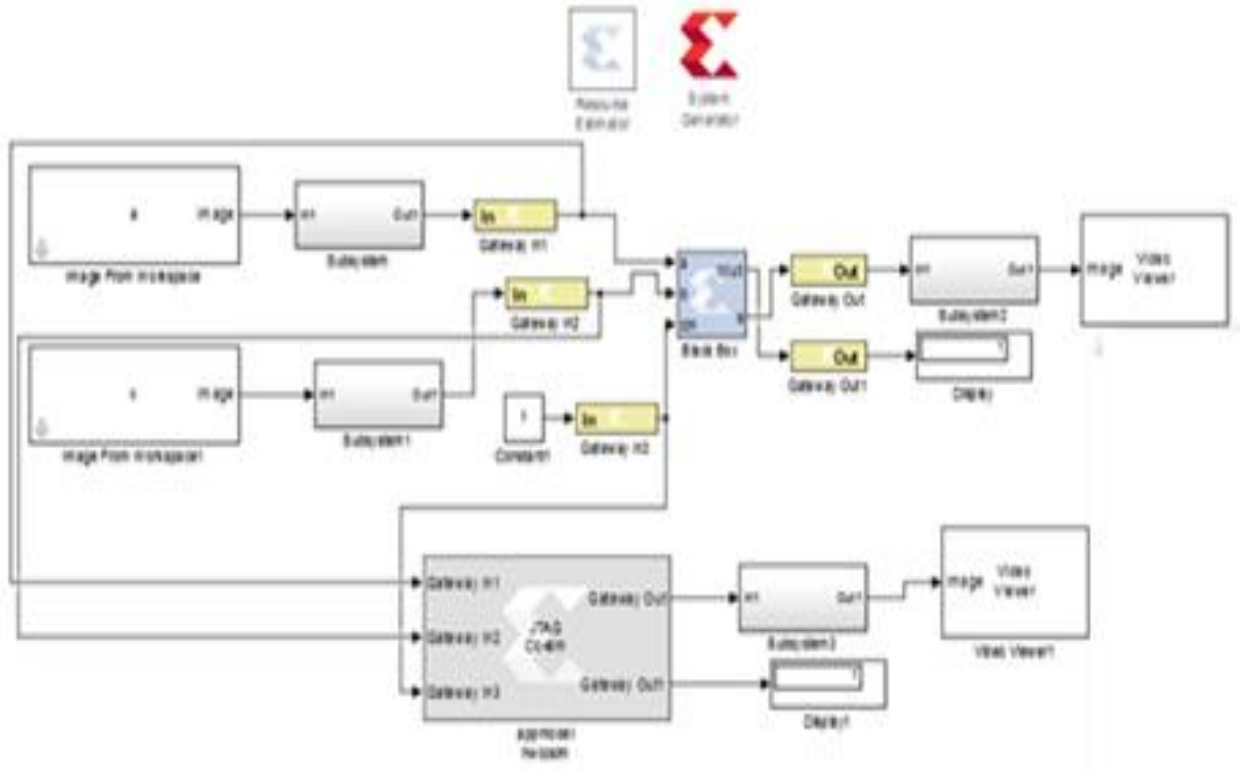

Figure 9 Xilinx Block for Hardware Implementation

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XII. Design Parameter

The result for the slices, LUTs, IOBs of the 16 bit accurate part, inaccurate part and overall part has been reported in table 2. The Overall part gives the approximate result rather than accurate result. Carry select adder is used for inaccurate part and ripple carry adder for accurate part where the inaccurate part is faster than accurate part as it does not wait for carry propagation while comparing to ripple carry adder, the carry select adder has more energy efficient.

Table 1 Comparison of accurate part and inaccurate part

Parameter	Overall part	Accurate part	Inaccurate part
Slices	0	1`	0
Flip flops	0	0	0
BRAM	0	0	0
LUTs	22	37	2
IOBs	50	50	5
Mults/DSP 48s	0	0	0
TBUFs	0	1	0

XIII. Conclusion

The proposed Static Segmentation Adder (SSA) design is found to be capable of producing high accuracy response for low contrast and high contrast images. In the proposed adder, accuracy and speed are increased by accuracy adjustment logic and static segment method. For all possible input combinations, performance analysis is carried out and the worst case error is computed. Carry select adder is faster than ripple carry adder as it does not wait for carry propagation. While comparing to ripple carry adder, carry select adder consumes less power, too fast, less area and more energy efficient. The process takes place in the minimum time. The proposed method of SSA consumes less energy and notably has high speed with average computational error of ~0.6%, when compared to an existing system.

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