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Design of Two Phase Sinusoidal Power Clock using Adiabatic Switching

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Abstract: "Adiabatic" is a term of Greek origin that has spent most of its history associated with classical thermodynamics. It refers to a system in which a transition occurs without energy usually in the form of heat being either lost to or gained from the system. In the context of electronic systems, rather than heat, electronic charge is preserved. Thus, an ideal adiabatic circuit would operate without the loss or gain of electronic charge. Hence, in this work the two phase sinusoidal power clock is designed using Adiabatic switching.

Keywords: *Adiabatic, classical thermodynamics, heat, electronic systems, electronic charge.*

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1. INTRODUCTION TOADIABATIC SWITCHING

The word *ADIABATIC* comes from the Greek word that is used to describe thermodynamic processes that exchange of no energy with the environment and therefore, no energy loss in the form of dissipated heat. In real-life computing, such ideal process cannot be achieved because of presence of dissipative elements like resistance in a circuit. However, one can achieve very low energy engine dissipation by slowing down the speed of operation and only switching transistors under certain conditions[1] . The signal energies stored in the circuit capacitances are recycled instead of being dissipated as heat. The adiabatic logic is also known as *energy recovery CMOS.*

It should be noted that the fully adiabatic operation of the circuit is an ideal condition which may be approached asymptotically as the switching process is slowed down. In most practical cases, the energy dissipation associated with a charge transfer event is usually composed of an adiabatic component and a non-adiabatic component. Therefore, reducing all the energy loss to zero may not possible, regardless of the switching speed. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems.

2. INTEGRATED POWER CLOCK GENERATORS

Our approach to power clock design is to integrate all power-clock switching transistors and associated control circuitry on the same CMOS chip with low-energy logic. Only small resonant-tank inductor(s) are added as external components [2]. The power is supplied from a low-voltage dc power source, a battery for example. Integration of power clock generators with logic has a number of advantages:

- The on-chip active devices are well suited for low-power, low-voltage power conversion, and the device sizes are available for optimization at design time;
- Power-clock distribution is improved because relatively large and detrimental parasitic inductances are removed from the distribution network; bonding-wire and other external parasitic inductances are absorbed by the external resonant-tank inductor(s);
- External discrete component count is minimized;
- On-chip power-clock control circuitry can easily be implemented: sensing of power- clock waveforms for control purposes is void of delays/noise introduced by the chip I/O interface.

2.1 POWER CLOCK GENERATION

In adiabatic circuits, power and clock lines are mixed into a single power clock line, which has both the functions of powering and timing the circuit. A DC to AC converter named power clock generator is needed for the generation of the power clock signal. To evaluate the performance of a power clock generator, the conversion efficiency is defined as the ratio of the dissipated energy in the adiabatic core and the total delivered energy from the DC supply. The LC resonant circuit is suitable for a power clock generator [3]. L is an external inductor and C is the distributed capacitance of the power clock line and it's connected logic circuits all over the chip. To have a stable frequency of oscillation, the equivalent on chip capacitance should be constant and data independent, which is achieved in the adiabatic logic circuit due to its differential nature.

$$C = \frac{\sqrt{2}I_L}{\pi V_{DDfC}}$$

The first step in designing the power clock generator for an adiabatic circuit is circuit modelling to determine the equivalent capacitance. This concept is described in the following Section and illustrated by the example of our adiabatic CLA.

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2.2 ADIABATIC LOGIC MODEL

For each phase, an approximate lumped-element model of the logic includes an equivalent

capacitor C to model energy storage, in series with a resistor *R* to model the losses. The values of the model parameters *R* and *C* can be extracted from the simulation tests where an external ideal sinusoidal voltage source is applied as the power clock. For a given clock frequency f, and a logic activity, the power loss P_L in the logic, and the RMS current I_L supplied to the logic by the power clock can be found from the test. Given P_L and I_L, the model parameters can be found as:

$$R = \frac{P_L}{I_L^2}$$

Where V_{DD} is the peak value of the applied power clock.

As an indication of the logic power loss P_L relative to the maximum loss $CV_{DD}^2 f_c$ that would occur in plain CMOS logic with the same C, we find

$$y_L = \frac{P_L}{CV_{DD}^2 f_c} = \frac{\pi P_L}{\sqrt{2} V_{DD} I_L} = \frac{\pi^2 RCf_c}{2}$$

We have performed this test for our adiabatic CLA and extracted the equivalent *R* and C for each power clock phase for the frequencies 10 MHz,20 MHz, 50 MHz and 100MHz. The results have been summarized in Table 3.1, where the tests were performed for the maximum logic activity of the circuit [4].

3. INTEGRATED RESONANT POWER CLOCK GENERATORS

Various circuit topologies for resonant energy recovery have been proposed for different adiabatic logic styles and for different applications. They can be classified into two main groups: asynchronous and synchronous power clock generators. Asynchronous power clock generators are free running circuits that use feedback loops to self-oscillate without any external timing signals. Fig. 4.1 illustrates two commonly used asynchronous power clock generators: 2N power clock generator. Many problems are associated with asynchronous structures. Their oscillation frequencies are sensitive to their capacitive load variations in different cycles of the system operation resulting in unstable frequency problems. In addition, in large systems, inputs and outputs of each module must be in synchronization with other modules prohibiting the integration of the adiabatic module driven by asynchronous power clock generators into a larger non-adiabatic system. In these cases, the synchronous power clock generators can be utilized as an efficient solution without having any of the above problems [5]. Synchronous power clock generators are synchronized to external time base signals usually available in large systems.

2N synchronous power clock generators, similar to the asynchronous counterparts except that the gate control signals are derived externally are shown. The capacitors CE1 and CE2 in Figure 3.1 and 3.2 are external balancing capacitors to achieve more conversion efficiency. We will show that the synchronous power clock generators are more energy efficient than the asynchronous ones.

3.1 POWER CLOCK DESIGN

We design all two power clock generators for the adiabatic CLA, at 10MHz operating frequency and 3.0V supply voltage, and compare the power dissipation and conversion efficiency. Using the results in Table 2, we design each of the power clock generators by placing simple resistors and capacitors equal to the extracted values instead of the adiabatic adder [6].

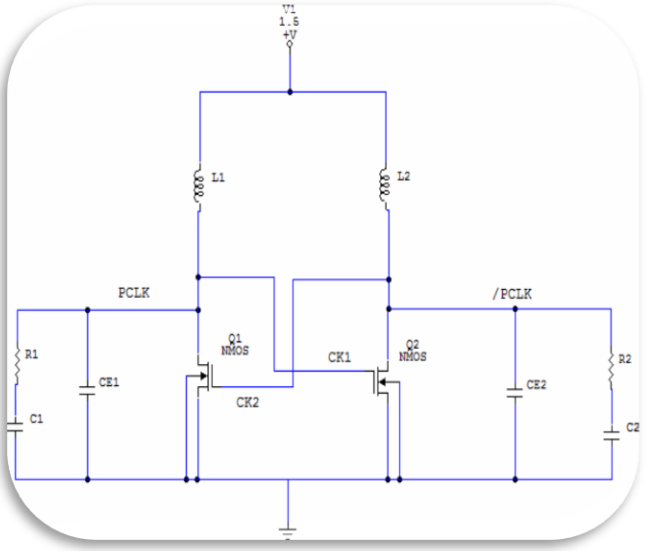

Figure – 3.1 2N Asynchronous two phase power clock generators

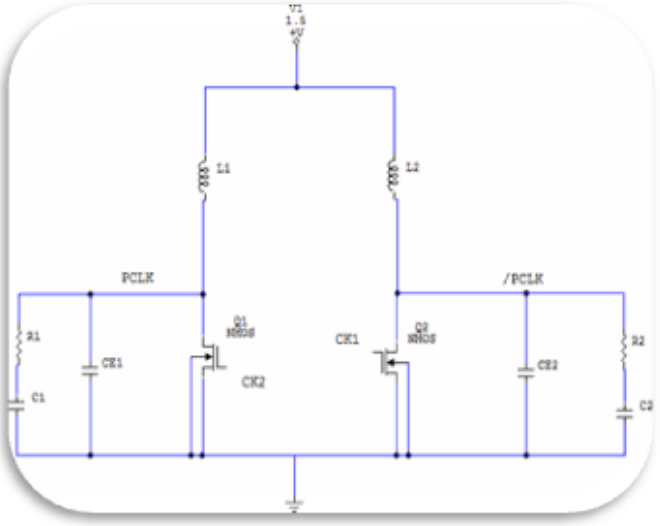

Figure - 3.2 2N Synchronous two phase power clock generators

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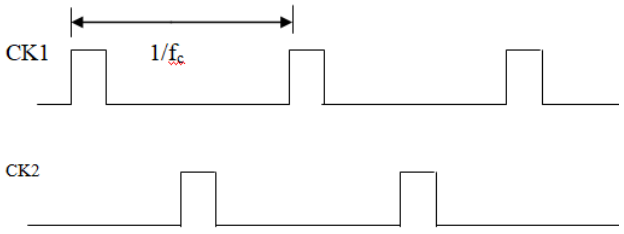

Figure – 3.3 Pulse signals to a synchronous power clock generator.

Then this simple circuit can be quickly designed and simulated to find the optimum design. The value of *L* is determined by the required frequency and the extracted capacitance. The oscillating frequency for the 2N power clock generators is determined by

$$f = \frac{1}{2\pi\sqrt{LC}}$$

Where C is the equivalent capacitance of each phase. After simulating and optimising the power clock generator with the simple RC model, the designed power clock generator is connected to the adiabatic CLA and simulated again. In this stage, slight modifications may be needed to optimise the design for the highest achievable conversion efficiency.

If we talk of only 1-n clock generator circuit, to determine the switch Qrms current, we observe that the switch current during the D/ f_c interval is increasing from zero approximately as a linear function of time. During the switch-on time, energy is added from the dc power source $V_{DD}/2$ to the resonant tank [7].

When the switch Q is turned off, the energy is dissipated during the oscillation. For a sustained steady state oscillation, we have the required energy balance equation given approximately by:

$$\frac{1}{2} L_r \, i_{on}^2 = \frac{P_L}{f_c}$$

Using the above equations, we solve for the switch current i_{on} at the end of the switch on time and the required switch duty ratio D,

$$i_{on} = 4I_L\sqrt{y_L}$$

$$D = \frac{\sqrt{2y_L}}{\pi}$$

The switch rms current I_s is then given by:

For Adiabatic CLA operating at 10 MHz, for phase 1, value of D came out to be 0.01124 and for phase 2, value of D came out to be 0.1118. The waveform for synchronous 2n power generator scheme is as follows

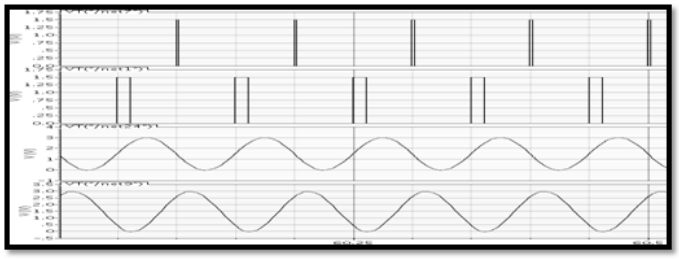

Figure – 3.5 Simulation results of 2N synchronous power clock generators

The results, summarised in Table 3.2, indicate that with synchronous power clock generators, higher conversion efficiencies can be achieved. Between the two synchronous schemes, the 2N power clock generator is simpler, more energy efficient, and resulting in the higher conversion efficiency of 53.26%.

3.0V supply voltage power clock generator	**Synchronous**	**Asynchronous 2N**
Power dissipation of a CLA core	4.54 µW	7.32 µW
Total delivered power	9.5 µW	107.33 µW
Conversion efficiency	52.15%	6.654%

Table 3.2 Power dissipation summary of adiabatic CLA with different power clock generators at 10MHz

operating frequency

3.0V supply voltage power clock generator	Synchronous	Asynchronous 2N
Power dissipation of a CLA core	4.54 µW	7.32 µW
Total delivered power	9.5 µW	107.33 µW
Conversion efficiency	52.15%	6.654%

4. CONCLUSION

From the observation it can be seen that results obtained by using Two-Phase Adiabatic Static Clocked Logic (2PASCL) shows a significant amount of reduction in power dissipation. The comparison of proposed logic with other traditional logics has been proved that power consumption is far less as compared

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to 2padcl based technique. In future these logics can be designed at other technologies to further reduce the power consumption and voltage swing can be improved and further work on minimization of chip area can also be done on various technologies.

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